XDP Hybrid-flyback Controller XDPS2201

Product Overview

Product Highlights

- Digital Hybrid-flyback controller with integrated half-bridge driver in DSO-14 (150mil) package
- 600V high voltage start-up cell for fast charging and low stand-by power
- Peak current mode control for robust and fast line and load control
- Burst mode entry/exit operation based on output current estimation
- Primary side output overvoltage protection
- Supports lowest no-load stand-by power < 75mW
- Wide range of configurable parameters via one pin UART interface
- Lowest necessary bill of material

Features

- Configurable brown-in and brown-out protection
- Configurable built-in soft-start
- Configurable burst mode entry and exit current thresholds with small hysteresis
- Configurable overcurrent protection with two levels for peak and transient load
- Configurable output overvoltage protection
- Configurable frequency reduction with cycle skipping for improved low load efficiency
- Configurable jitter for switching frequency
- Configurable propagation delay compensation for accurate peak current control
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Target Applications

- AC/DC SMPS
- Ultra high power density adapter > 20W/inch^3
- Ultra high efficiency SMPS > 93%

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The XDPS2201 contains a Hybrid-flyback controller that is based on an asymmetrical half-bridge control. The half-bridge is driving a conventional flyback transformer in conjunction with a serial capacitor. The main inductance of the flyback transformer and the serial capacitor are building a resonant tank, which is used for achieving zero voltage switching (ZVS) behavior of the half-bridge power switches and is providing in addition a resonant power transmission during the conventional demagnetization phase of the flyback transformer. During normal operation the charge period and associated power is controlled by direct peak current control, whereas the demagnetization phase is timing controlled to ensure proper negative premagnetization, which is required for ZVS condition at the half-bridge power switches. Beside the continuous resonant mode (CRM) operation the IC also provides an advanced zero voltage resonant valley switching (ZV-RVS) and burst mode to support highest efficiency over the whole load and wide output voltage range.

Sales Code	Package	SP-Ordering Code
XDPS2201	PG-DSO-14	SP005417712

Typical Application

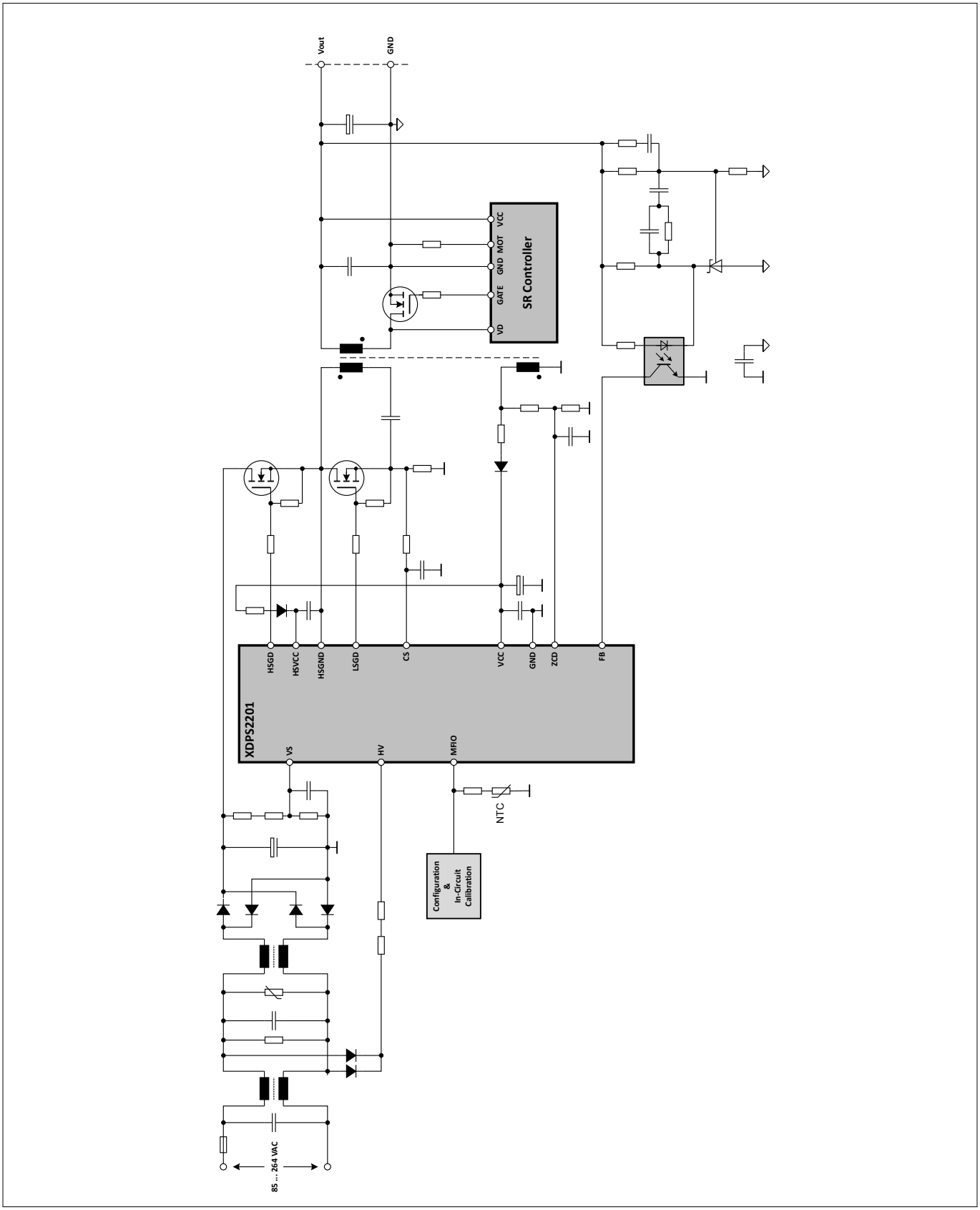


Figure 1 High density adapter < 75W

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1 Pin configuration

The pin configuration is shown in ***Figure 2*** and ***Table 1***. The pin functions are described in the sequel.

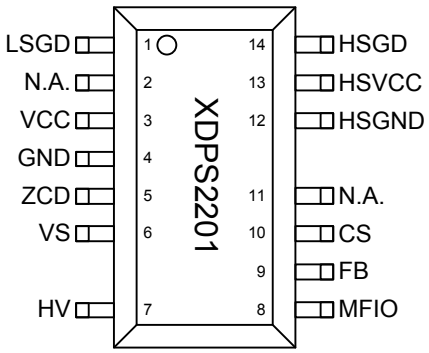


Figure 2 Pin configuration

Table 1 Pin definitions and functions

Symbol	Pin	Type	Function
LSGD	1	O	**Low-side gate driver** Low-side gate driver of half-bridge driver stage
N.A.	2	—	**Not available** This pin is internally connected but not used, and should be connected to GND
VCC	3	I	**Positive voltage supply** IC power supply
GND	4	O	**Ground** Combined power and signal ground
ZCD	5	I	**Zero-crossing detection** *ZCD* pin provides zero-crossing detection after the low-side gate driver is turned off, during pause phase in skip cycle and burst mode. Furthermore, the reflected output voltage at auxiliary winding can be measured during the low-side gate driver turn-on phase
VS	6	I	**Voltage sensing** Low leakage input voltage sensing pin for controlling the negative magnetization and protections. *VS* pin is connected to a resistor divider for measuring the bulk voltage
HV	7	I	**High-voltage input** *HV* pin is connected to the AC line via external resistors and 2 diodes. An internally connected 600 V HV start-up cell is used for the initial VCC charge
MFIO	8	IO	**Multi-functional input-output** UART communication for parameter configuration and failure mode reporting is provided by this pin. In addition, a connected NTC can be measured
FB	9	I	**Feedback** Input pin receiving the feedback control signal from the optocoupler
CS	10	I	**Current sensing**

Pin configuration

Table 1 Pin definitions and functions (continued)

Symbol	Pin	Type	Function
			Input pin for current sensing during the high-side gate driver turn-on phase
N.A.	11	—	**Not available** This pin is internally connected but not used, and should be connected to GND
HSGND	12	O	**High-side ground** Ground reference node for floating driver domain
HSVCC	13	I	**High-side power supply** Power supply input for floating driver domain
HSGD	14	O	**High-side gate driver** Floating high-side gate driver of half-bridge driver stage

2 Block diagram

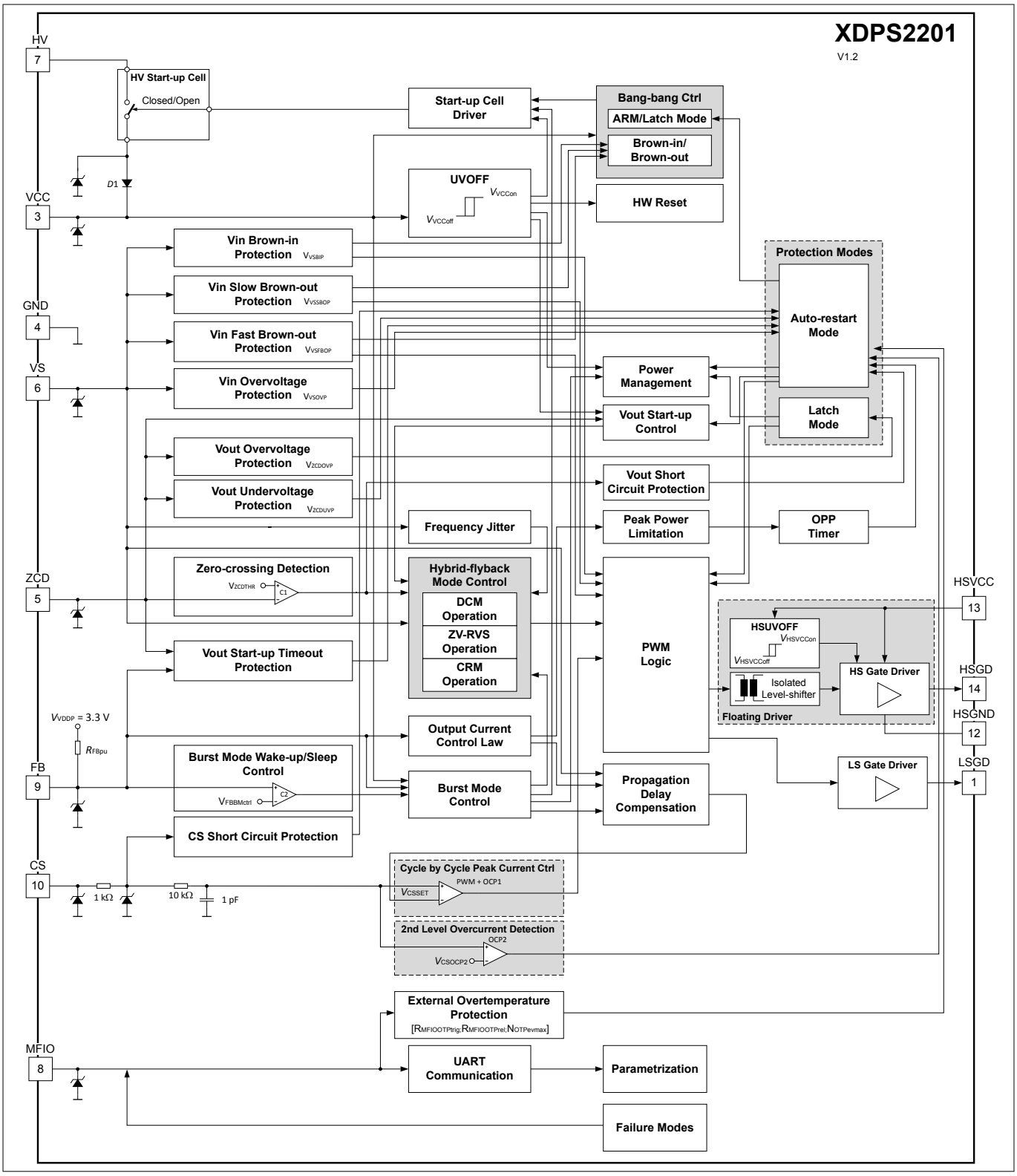


Figure 3 Block diagram

3 Functional description

The functional description gives an overview about the integrated functions and features and their relationship. The mentioned parameters are based on either configurable parameters shown in ***Chapter 4.1*** or fixed parameters shown in ***Chapter 5.5***.

This chapter contains following main descriptions:

- Introduction (***Chapter 3.1***)
- Power supply management (***Chapter 3.2***)
- Control features (***Chapter 3.3***)
- Protection features (***Chapter 3.4***)

3.1 Introduction

In the following a brief introduction is given for the hybrid-flyback converter, which is based on a resonant asymmetrical half-bridge flyback topology shown in ***Figure 4***.

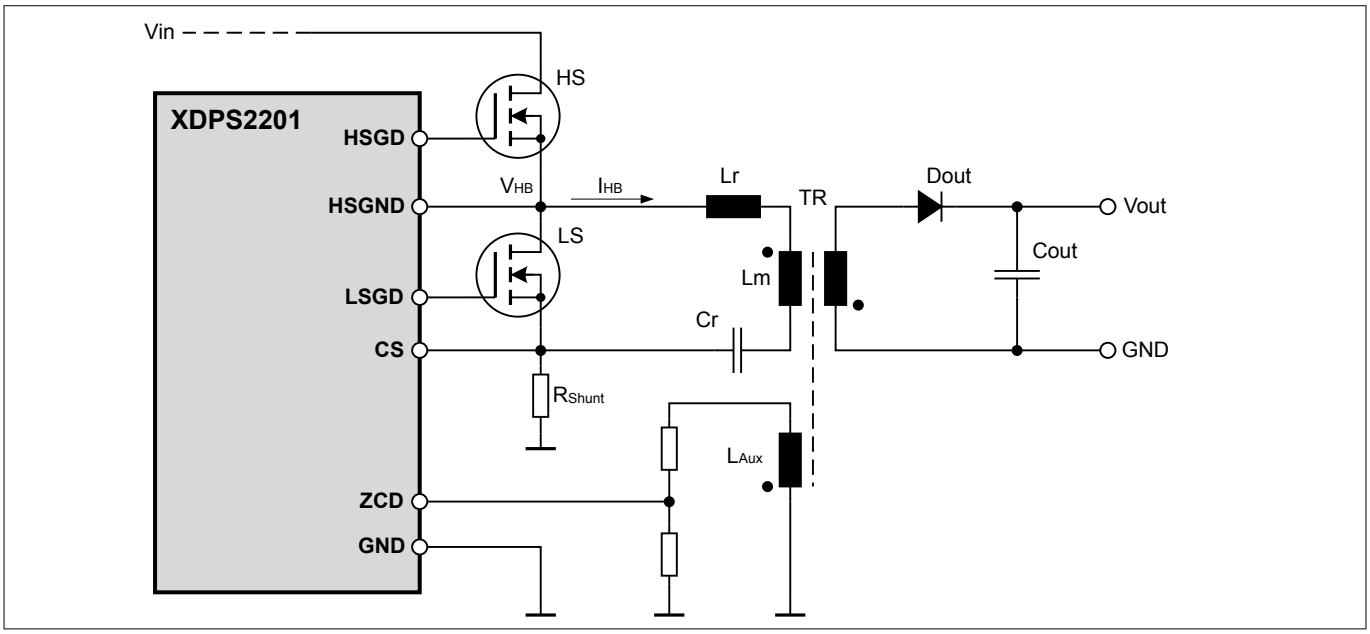


Figure 4 Hybrid-flyback power stage

The main advantage of this hybrid-flyback topology is the extended energy storage approach, which enables the usage of a smaller transformer at the same switching frequency compared to the standard and active clamp flyback topologies. In hybrid-flyback the total energy is not only stored in the transformer. In addition an amount of energy is stored in an external capacitor *Cr*, which is connected in series with the transformer. The proportion of the amount of energy that is stored in transformer and capacitor is depending on the input voltage. For lower input voltage more energy is getting stored in the capacitor. The switching frequency is also depending on the input voltage similar to a critical conduction mode flyback operation (see ***Figure 5***).

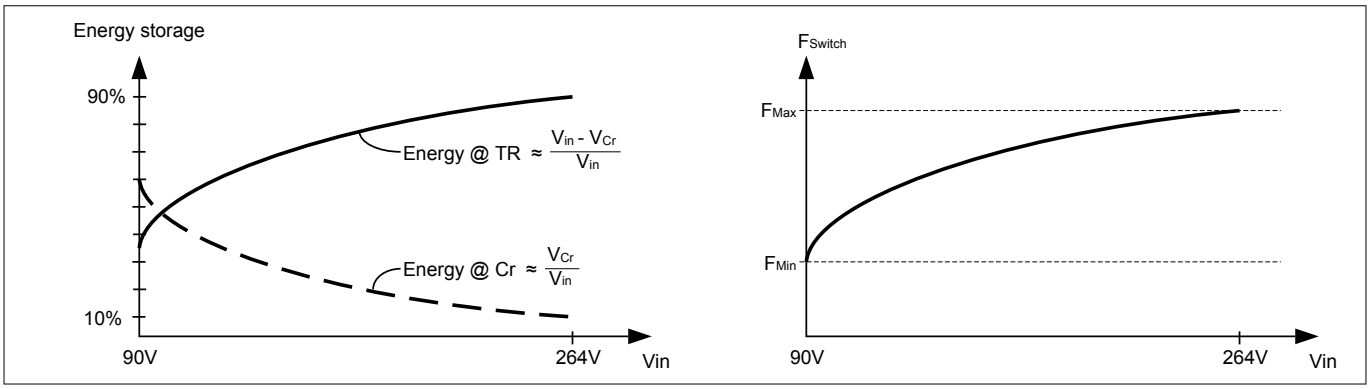


Figure 5 Hybrid-flyback energy storage sharing and switching frequency dependency

The resonant asymmetrical half-bridge flyback power stage can achieve zero voltage switching (ZVS) operation on primary side and zero current switching (ZCS) operation on secondary side under all conditions of input voltage *Vin* and output voltage *Vout*. The power circuit in the primary side is realized by an LC tank, built by the resonant inductor *Lr* and resonant capacitor *Cr*, which is driven by a half-bridge similar to an LLC converter. *Lr* represents the series inductance, being *Lr* either only the transformer leakage inductance or the leakage inductance plus an optional external inductor. With this configuration the transformer leakage energy is recycled avoiding the switching losses of traditional single switch flyback converter.

In order to achieve lowest switching losses by means of ZVS operation over the whole load range, two control methods are implemented to support maximum efficiency over wide *Vin*, wide *Vout* and whole output load ranges. The control methods are based on measured current signal V_{CS} at shunt resistor R_{Shunt}, voltage signal V_{ZCD} and valley detection N_{RVSval} at auxiliary winding L_{Aux} and input voltage *Vin*.

Following operating modes are supported by the two control methods for ensuring ZVS operation:

- Continuous resonant mode (CRM) operation (see ***Chapter 3.1.1***)
- Zero voltage resonant valley switching (ZV-RVS) operation (see ***Chapter 3.1.3***)

3.1.1 Continuous resonant mode (CRM)

The operation phases of the resonant asymmetrical flyback duty cycle can be divided into 6 phases as shown in ***Figure 6*** and ***Figure 7***. In continuous resonant mode (CRM) the switching of high-side switch *HS* and low-side switch *LS* is done in an alternating manner without blanking phases. Only short dead-times t_{deadHS} for the high-side switch turn-on and t_{deadLS} for the *LS* switch turn-on apply during the soft resonant switch-over of the half-bridge middle node.

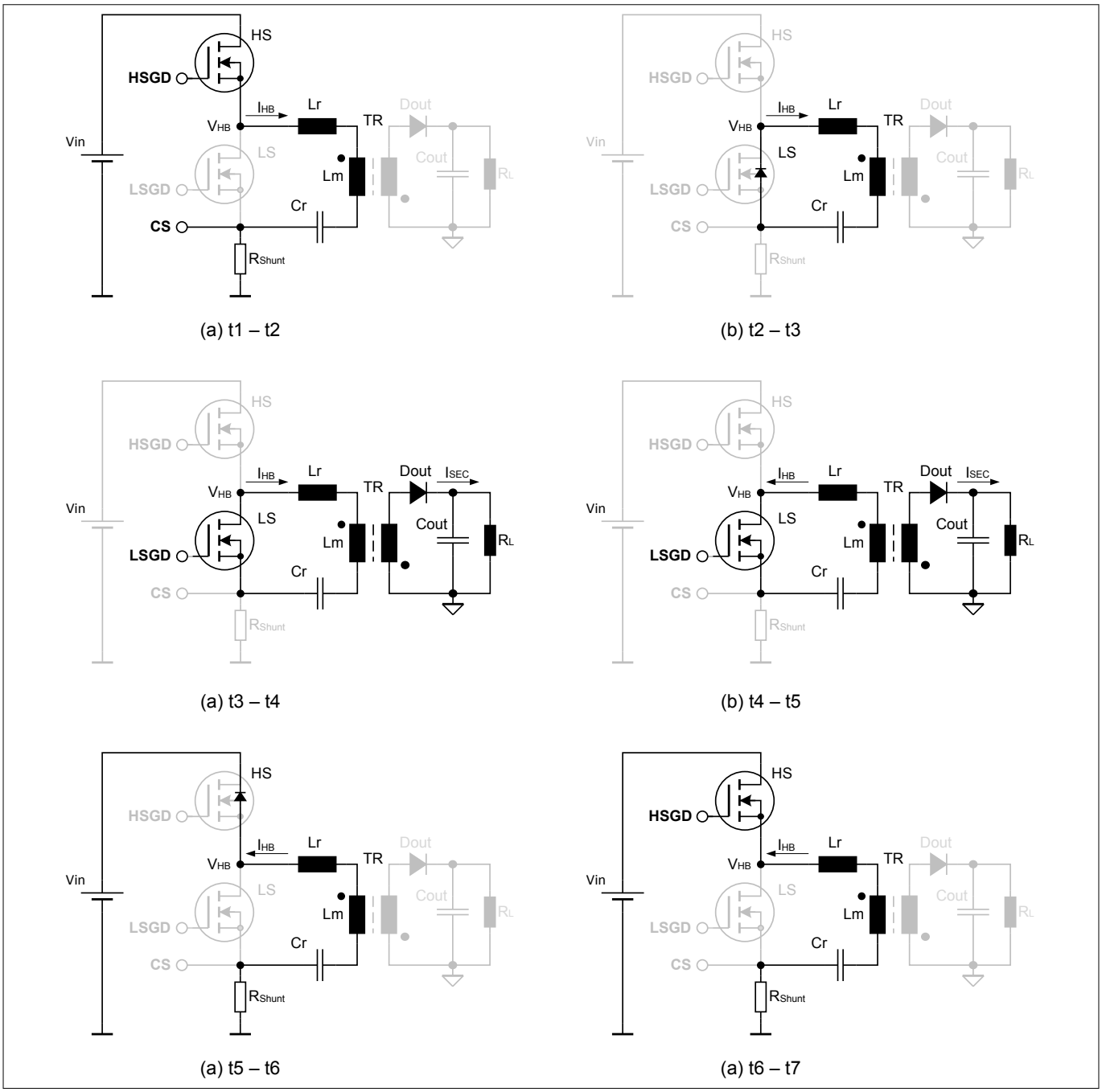


Figure 6 Hybrid-flyback converter operation phases in CRM

Phase 1, t1 to t2:

Phase 1 starts when the half-bridge current I_{HB} is changing in direction to a positive value. In this phase *HS* switch is turned on and *LS* switch is turned off since time *t0*. The increasing positive current I_{HB} is magnetizing the transformer *TR* and charging the resonant capacitor *Cr*. The output diode *Dout* is biased inversely blocking any energy transfer to the secondary side. The magnitude of I_{HB} is measured via the shunt resistor R_{Shunt}. Phase 1 is finished once I_{HB} exceeds an internal peak current set-point, which turns off the *HS* switch.

Phase 2, t2 to t3:

At time *t2 HS* switch is also turned off, which disconnects the charging path from *Vin*. The magnetizing current I_{HB} in the transformer *TR* keeps flowing and forces the voltage at the half-bridge node V_{HB} to drop until the body diode of *LS* switch starts to conduct. At this time *t3* the primary side of the transformer *TR* has the same voltage level as capacitor *Cr*.

Phase 3, t3 to t4:

During phase 3 *HS* switch is kept turned off. At time *t3 LS* switch is turned on under zero voltage (ZVS) condition. The voltage at secondary winding of transformer *TR* is now equal to the voltage across the resonant capacitor *Cr*, divided by the transformer turns ratio. The secondary side current I_{SEC} starts flowing through output diode *Dout*. The resonant sine wave shape and period of I_{SEC} is determined by the resonant tank formed by the transformer leakage inductance *Lr* and *Cr*. The primary half-bridge current I_{HB} is the sum of the transformer *TR* magnetizing current I_{MAG} plus the reflected secondary side current I_{SEC}. The current in the resonant *LrCr* tank is still positive and mainly driven by the transformer magnetizing inductance *Lm*, which charges further the resonant capacitor *Cr*. In this manner the energy stored in the transformer and *Cr* is transferred to the output.

Phase 4, t4 to t5:

Phase 4 starts when the primary side half-bridge current I_{HB} inverts its direction, which is driven by the resonant *LrCr* tank. During this time period the energy is still being transferred to the secondary side. At the same time also bringing down the transformer magnetizing current I_{MAG} to a negative level equivalent with I_{MAGneg} is supported as long *LS* switch is kept turned on.

Phase 5, t5 to t6:

At the beginning of phase 5 *LS* switch is also getting turned off. The negative current I_{MAGneg} in the transformer *TR* induced during the previous phase 4 is forcing the half-bridge bridge voltage V_{HB} to rise until clamping is taking place by the body diode of *HS* switch.

Phase 6, t6 to t7:

Phase 6 starts with turning on *HS* switch at ZVS condition. As the transformer resonant tank *LmCr* current I_{MAG} is still negative the excess of energy in the tank is sent back to the input.

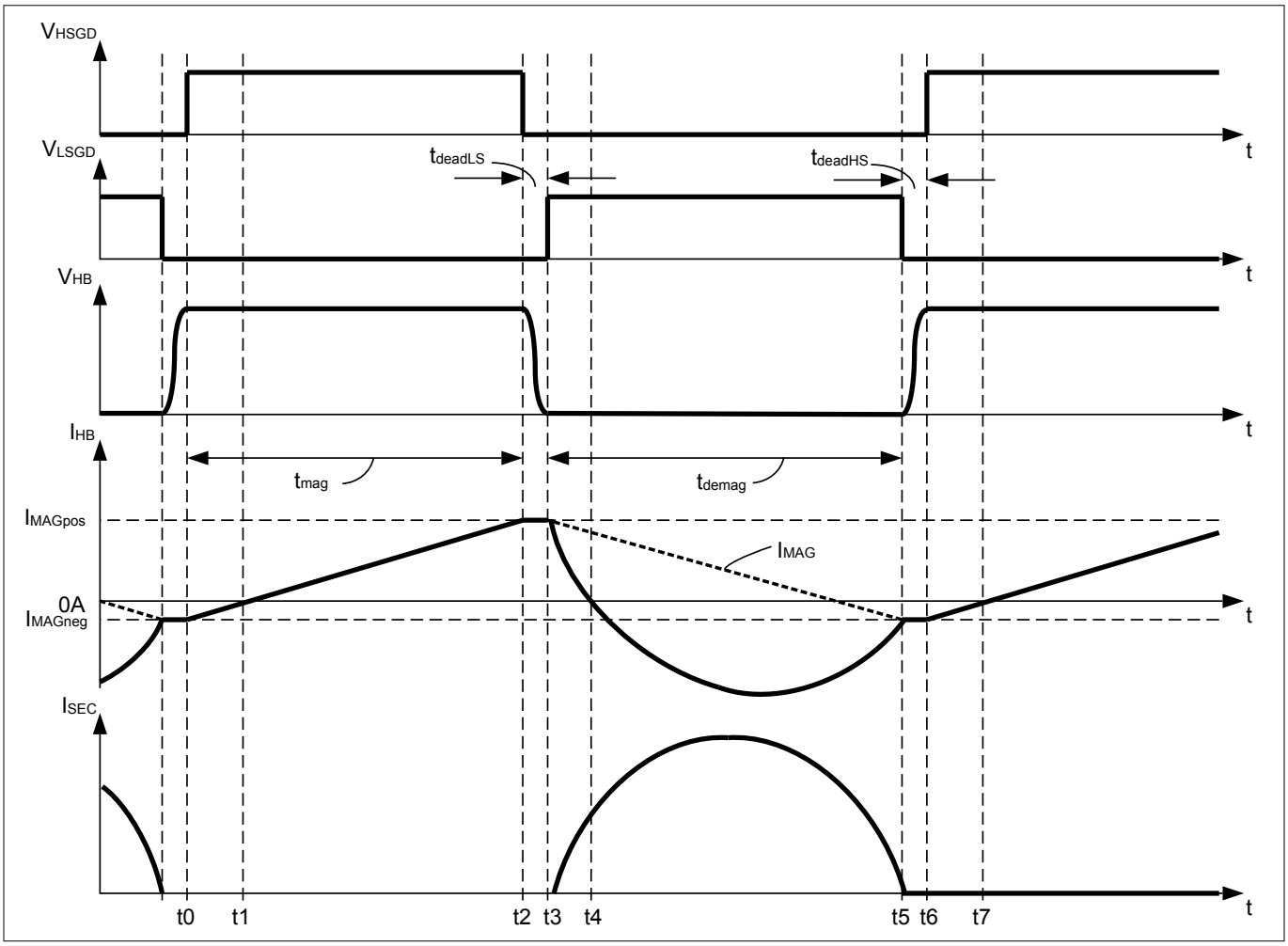


Figure 7 Hybrid-flyback converter signals

3.1.2 Boundary conditions for ZVS operation

Achieving a zero voltage switching (ZVS) turn-on condition for both *HS* and *LS* switches requires the right polarity of the resonant tank *LmCr* current I_{MAG}. Furthermore a sufficient energy level in the resonant tank *LmCr* is needed to switch-over the half-bridge voltage V_{HB} during the dead-times t_{deadLS} and t_{deadHS}. By ensuring ZVS operation, hard switching with undesired oscillations and, in worst case, body diode cross conduction can be properly avoided.

Switching over from *HS* switch to *LS* switch under ZVS condition is properly supported by the positive magnetization level (see ***Figure 7***) . Forcing ZVS condition for switch-over from *LS* switch to *HS* switch is covered by regulating the negative magnetization level depending on the input voltage *Vin*.

Wide Vout voltage range operation

When operating with variable output voltage there is an application requirement for adapting the switching phase between HS switch turn-on phases to ensure ZVS condition. ***Figure 8*** shows an example for a potential body diode cross conduction when output voltage is reduced and the timings for *LS* switch turn-on phase t_{LSon} and start of *HS* turn-on are not adapted. At time t3 the slope of demagnetization current I_{MAG} is flatter compared to time period before t0 due to lower *Vout* level. This leads to a larger demagnetization period t_{demag} of the transformer (see ***Equation 7***). Keeping the pulse pattern for t_{LSon} and dead-time t_{deadHS} for turning on the *HS* switch constant would result in a body diode cross conduction of *LS* switch at time t5 (see ***Figure 8***). Here I_{MAG} is still positive and therefore not switching-over the half-bridge node and not finishing the conduction of the *LS* switch body diode. By adapting the pulse pattern depending on *Vout* ZVS condition is reached for all output voltage and load conditions (see ***Chapter 3.3.1.2.1***).

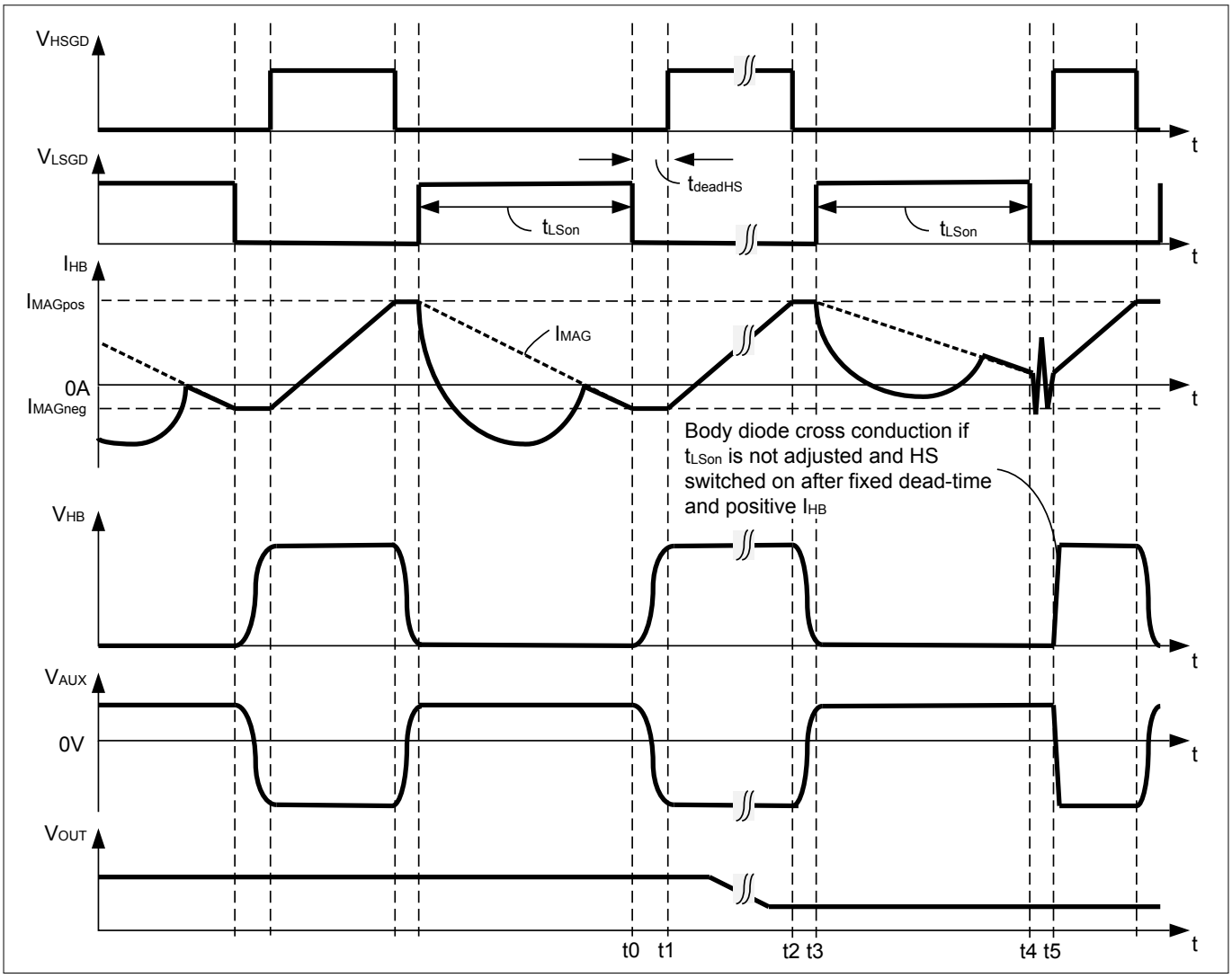


Figure 8 Body diode cross condunction at low Vout and fixed *LS* switch on-time

3.1.3 Zero voltage resonant valley switching mode (ZV-RVS)

When decreasing the load the amount of circulating magnetization energy is proportionally increasing compared to the transmitted energy in CRM operation. When decreasing *Vout* the demagnetization time is becoming longer than half of the resonant period of the *LrCr* tank, which can lead to further resonant half-bridge oscillations. Turning off the *LS* switch during an ongoing I_{HB} oscillation can lead to oscillations on the secondary side due to the secondary side leakage inductance.

The higher circulation half-bridge current at low output load is limiting the achievable efficiency in CRM operation.

To overcome the mentioned issues the zero voltage resonant valley switching (ZV-RVS) mode is implemented to fix the peak to peak magnetization current and support a frequency foldback operation to reduce the average amount of circulating magnetization current.

ZV-RVS mode is based on valley detection of the signal at auxiliary winding L_{AUX} via *ZCD* pin zero-crossing detection. The free-wheeling oscillation, which is observed after demagnetization of transformer has finished, is the same as seen in the standard flyback topology. ***Figure 4*** shows the auxiliary winding L_{AUX} used for zero-crossing detection, the falling edge indicating a rising half-bridge voltage V_{HB} and vice versa.

For optimum operation a waiting time gap $t_{waitgap}$ is introduced after a *HS* and *LS* switching cycle, which increases the associated half-bridge switching period. The time period $t_{waitgap}$ is depending on the set number

for skipping valley detection before the next zero-crossing rising edge detection leads to a dedicated ZVS pulse. The number of skipped valleys is increasing with decreasing output load. After the ZVS pulse only one *HS* and *LS* half-bridge switching cycle with subsequent $t_{waitgap}$ is performed. The ZVS pulse is generated by turning on *LS* switch under ZVS condition and forcing a negative half-bridge current level I_{MAGneg} to create a negative magnetization of the transformer. This leads to the same ZVS condition for turning on *HS* switch similar to CRM operation (see ***Chapter 3.1.1***).

The operation can be divided into 8 phases as shown in ***Figure 9***.

Phase 1, t0 to t1:

Phase 1 starts with finishing the demagnetization of the transformer. In this phase both switches are kept turned off and the half-bridge current I_{HB} is only determined by the free-wheeling oscillation due to parasitic capacities and inductivities connected to the half-bridge node. Phase 1 ends with a zero-crossing rising edge detection, which is depending on the set valley skipping number. A zero-crossing rising edge detection via *ZCD* pin indicates that V_{HB} is dropping to 0V as base for reaching ZVS condition for turning on *LS* switch.

Phase 2, t1 to t2:

Phase 2 is a predefined delay time for turning on *LS* switch after the zero-crossing rising edge detection at time t1. The predefined delay time is depending on the free-wheeling oscillation period and provides ZVS condition for V_{HB}.

Phase 3, t2 to t3:

At time t2 *LS* switch is turned on under ZVS condition. *HS* switch is still kept turned off. The voltage on the resonant capacitor *Cr* is applied to the primary winding of the transformer forcing a negative flowing half-bridge current level I_{HBneg}, which magnetizes the transformer in the negative direction. The injected current during ZVS pulse on-time t_{ZVS} needs to provide the right amount of energy for switching over the half-bridge node voltage V_{HB}.

*Note: Depending on the voltage of the resonant capacitor Cr and the output capacitor Cout, a secondary side synchronous controller (SR) may get triggered at the same time when ZVS pulse is generated. To avoid a shoot-through with SR controller being turned on when subsequently turning on HS switch, the minimum on-time of the SR controller must be shorter than the minimum pulse width of ZVS pulse t_{ZVS} (see **Figure 29**).*

Phase 4, t3 to t4:

At time t3 *LS* switch is turned off. The negative half-bridge current keeps flowing and pulls up the half-bridge node. Once the half-bridge voltage V_{HB} is clamped by the body diode in *HS* switch ZVS condition is reached for turning on *HS* switch. Phase 4 is similar to the phase 5 in ***Chapter 3.1.1***.

Phase 5, t4 to t5:

At time t4 *HS* switch is turned on. Once the half-bridge current I_{HB} changes in polarity, energy is taken from the input capacitor and stored in the transformer and the resonant capacitor *Cr*. I_{HB} is rising and increasing the voltage at *Cr*. During this phase the secondary diode is inversely polarized and blocking a flowing current.

Phase 6, t5 to t6:

At time t5 *HS* switch is turned off. The half-bridge current I_{HB} keeps flowing and decreases the half-bridge voltage V_{HB} down to 0V, leading to ZVS condition for *LS* switch.

Phase 7, t6 to t7:

In phase 7 the main energy transmission to the secondary side is taking place. Once the half-bridge current I_{HB} starts to decrease, the secondary side diode *Dout* is getting forward polarized and charging the output capacitor *Cout*. I_{MAG} is then demagnetizing the transformer. In addition a resonant current is superimposed, which is generated by the transformer leakage inductance and the resonant capacitor acting as resonant tank *LrCr*. As *Lr* is significant smaller than *Lm* the resonant period of *LrCr* tank is much shorter and can be seen as an oscillation. The very large resonant period of *LmCr* tank can be seen as a linear decrease of magnetizing current in this relative short time phase.

Phase 8, t7 to t8:

Phase 8 shows an example of the half-bridge current signal when the *LrCr* tank half resonant period is shorter than the demagnetization phase at *LS* switch turn-off. This shape of current is depending on the operation conditions determining the demagnetization period and low-side on-time. At time t8 the demagnetization of the transformer is finished. The secondary side diode *Dout* is again inversely polarized and the free-wheeling oscillation at the half-bridge node is starting.

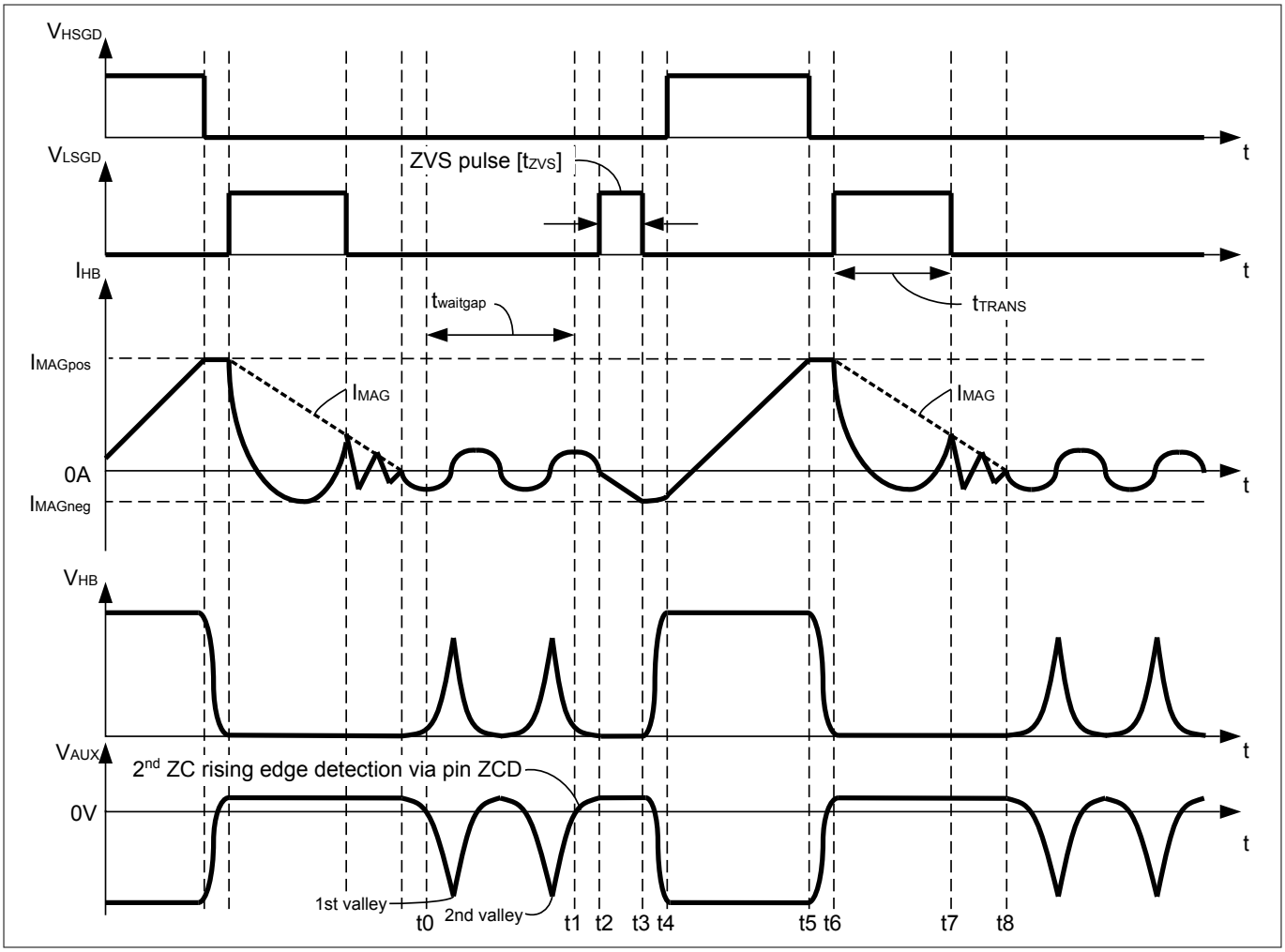


Figure 9 Hybrid-flyback operating in zero voltage resonant valley switching mode (ZV-RVS)

3.1.4 Output control methods

Output current control in CRM

The hybrid-flyback topology can be controlled either by duty cycle control or a combination of peak current control for *HS* switch and on-time control for *LS* switch. When looking on duty cycle control for *HS* switch a relationship between output voltage V_{out} and input voltage V_{in} is given as shown in the following equation. All equations in the sequel are based on considering ideal lossless components and neglecting any dead-times.

$$V_{\text{out}} = D \times \frac{V_{\text{in}}}{N} \times \frac{L_m}{L_m + L_r}$$

Equation 1

The duty cycle *D* is determined by

$$D = \frac{t_{\mathrm{HSon}}}{t_{\mathrm{HSon}} + t_{\mathrm{LSon}}}$$

Equation 2

with t_{HSon} and t_{LSon} being the on-times for *HS* and *LS* switches. *N* represents the winding turns ratio between primary and secondary side of the transformer.

Equation 1 shows that V_{out} is independent of the output current I_{out}.

Same as for standard flyback controllers primary peak current control is implemented to support a 1st order system for easier control loop compensation. The taken input power per half-bridge switching cycle is depending on the voltage at the resonant capacitor *Cr* that is charged by the half-bridge current I_{HB} during the on-time t_{HSon}. The input power can be calculated as shown in the following equation.

$$P_{\mathrm{in}} = \frac{1}{2} \times V_{\mathrm{Cr_avg}} \times \left(I_{\mathrm{MAGpos}} + I_{\mathrm{MAGneg}}\right)$$

Equation 3

$V_{\mathrm{Cr_avg}}$ is the average voltage on the resonant capacitor *Cr*, which is the reflected output voltage V_{out} multiplied with the transformer turns ratio. The output voltage is reflected at winding L_{AUX} during the on-time period of *LS* switch.

$$V_{\mathrm{Cr_avg}} = N \times V_{\mathrm{out}}$$

Equation 4

Assuming an ideal system with no losses, the taken output power P_{out} can be seen as the transferred input power $P_{\mathrm{in}} = P_{\mathrm{out}}$. Both leads to a direct correlation between input half-bridge current I_{HB} and average output current I_{out} as shown following.

$$I_{\mathrm{out}} = \frac{P_{\mathrm{out}}}{V_{\mathrm{out}}} = \frac{1}{2} \times N \times \left(I_{\mathrm{MAGpos}} + I_{\mathrm{MAGneg}}\right)$$

Equation 5

Equation 5 shows that I_{out} can be controlled only by controlling I_{MAG} and can then be independent of *Vin* and *Vout*. This is different compared to a standard flyback controller, where by means of peak current control the output power P_{out} is controlled independent on output voltage.

The hybrid-flyback is controlling the magnetization time t_{mag} and demagnetization time t_{demag} (see ***Figure 7***) in 2 different ways. t_{mag} is mainly controlled by the positive half-bridge current level I_{MAGpos} by means of peak current control at shunt resistor R_{shunt} via *CS* pin. Whereas t_{demag} is controlled by adjusting the on-time t_{LSon}. Increasing t_{demag} increases the negative magnetizing current level I_{MAGneg} when keeping I_{MAGpos} level constant. During output overcurrent condition t_{demag} can be temporarily longer than t_{LSon} due to waiting for the zerocrossing detection before turning on the *HS* switch. The correlations between t_{mag}, t_{demag} and I_{MAGpos}, I_{MAGneg} are shown in following equations:

$$t_{\mathrm{mag}} = \frac{L_m \times \left(I_{\mathrm{MAGpos}} - I_{\mathrm{MAGneg}}\right)}{V_{\mathrm{in}} - V_{\mathrm{Cr_avg}}}$$

Equation 6

$$t_{\mathrm{demag}} = \frac{L_m \times \left(I_{\mathrm{MAGpos}} - I_{\mathrm{MAGneg}}\right)}{N \times V_{\mathrm{out}}}$$

Equation 7

Output current control in ZV-RVS mode

Compared to CRM operation the ZV-RVS mode is adding waiting time gaps $t_{waitgap}$, where no energy is either taken from the input nor energy is transferred to the output. This extends the minimum off-time, which is determined by the on-time of the *LS* switch. The average output current I_{out} is decreasing with increasing $t_{waitgap}$ derived by following equation from ***Figure 10***. This provides 2 degree of freedom to control the output current by means of half-bridge current I_{HB} and extended half-bridge switching period $t_{HBperiodex}$ adjustment.

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{t_{HBperiod}}{t_{HBperiodex}} \times \frac{1}{2} \times N \times \left(I_{MAGpos} + I_{MAGneg}\right)$$

Equation 8

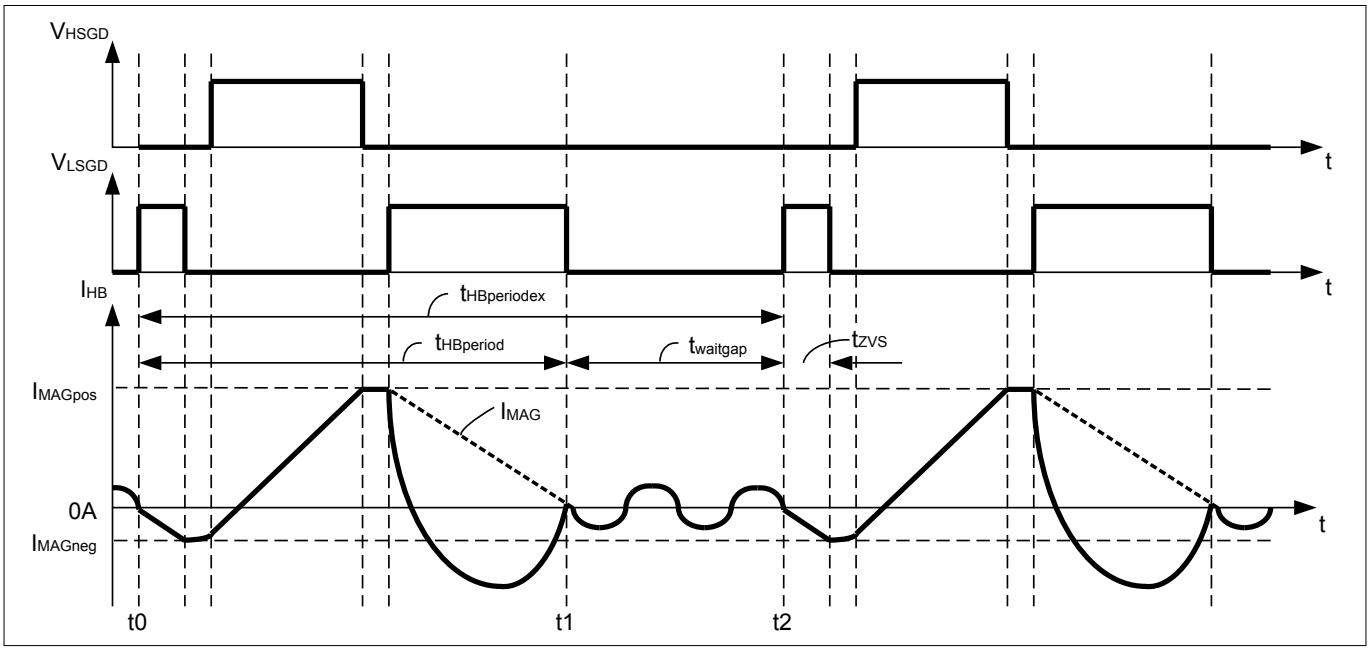


Figure 10 ***LrCr* tank and I_{MAG} currents during ZV-RVS mode operation**

3.2 Power supply management

The power supply management ensures a reliable and robust IC operation. Depending on the operation mode of the control IC, the power supply management unit runs in different ways for VCC supply, which are described as in the sequel.

- VCC capacitor charge-up and start-up sequence (***Chapter 3.2.1***)
- Bang-bang mode operation during brown-in phase (***Chapter 3.2.1***)
- Bang-bang mode operation during protection mode (***Chapter 3.2.3***)
- VCC supply during burst mode (BM) operation (***Chapter 3.2.4***)

3.2.1 VCC capacitor charge-up and start-up sequence

At VCC start-up the capacitor C_{VCC} is being charged by the internal HV start-up cell via *HV* pin (see ***Figure 11***). The high voltage *HV* pin is connected to an external resistor R_{HV}, which is in series with 2 diodes connected to *VAC*. The internal HV start-up cell is turned on for V_{VCC} lower than the IC deactivation voltage threshold V_{VCCoff} (see ***Chapter 3.4.2***). Once the voltage at *VCC* pin exceeds the threshold V_{VCCon} at time *t0* the HV start-up cell is turned off and the IC is starting the internal hardware initialization procedure (see ***Figure 12***). Subsequently the IC starts with half-bridge gate driver operation after brown-in condition is reached at time *t2* (see ***Chapter***

3.4.4.1). During this period of time the VCC capacitor is discharging until the external VCC self-supply takes over at time *t3* and start regulating the voltage at *VCC* pin for V_{VCCss}.

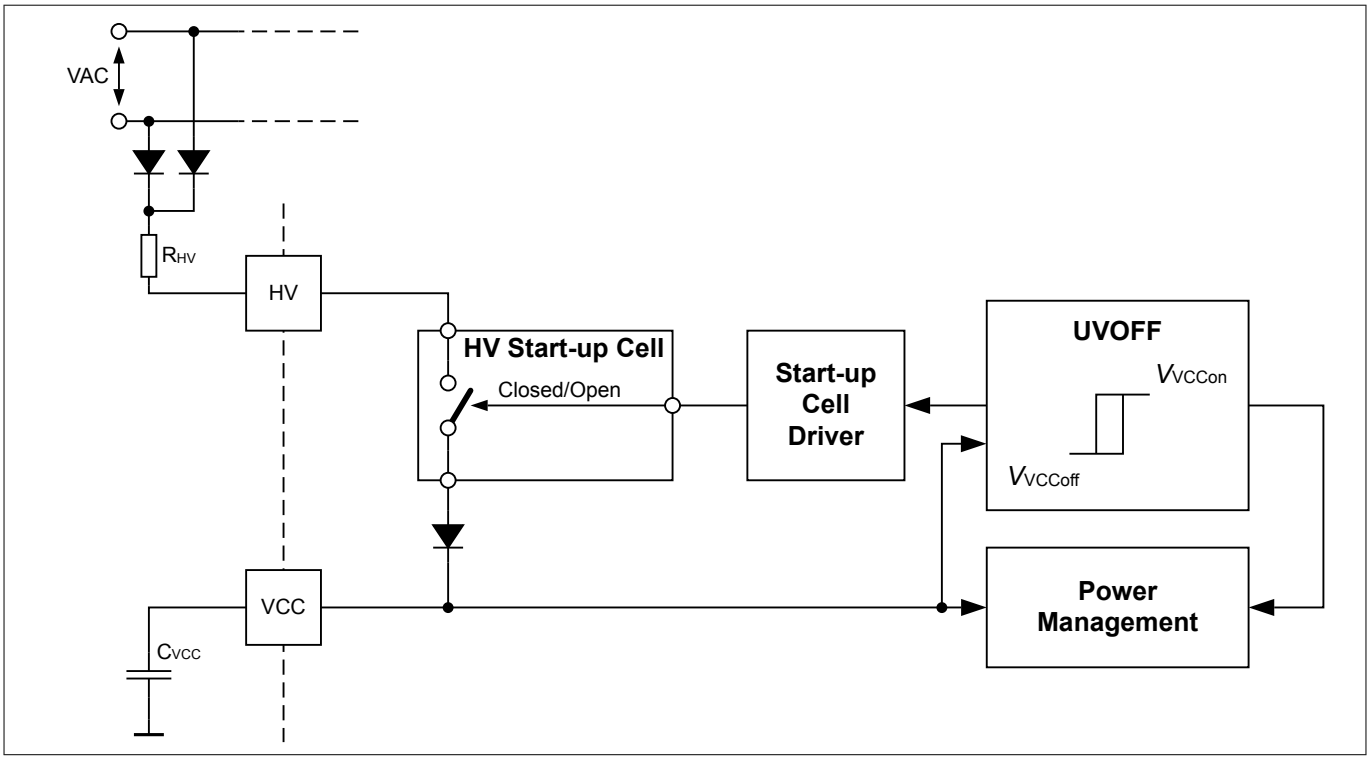


Figure 11 VCC capacitor charge-up control

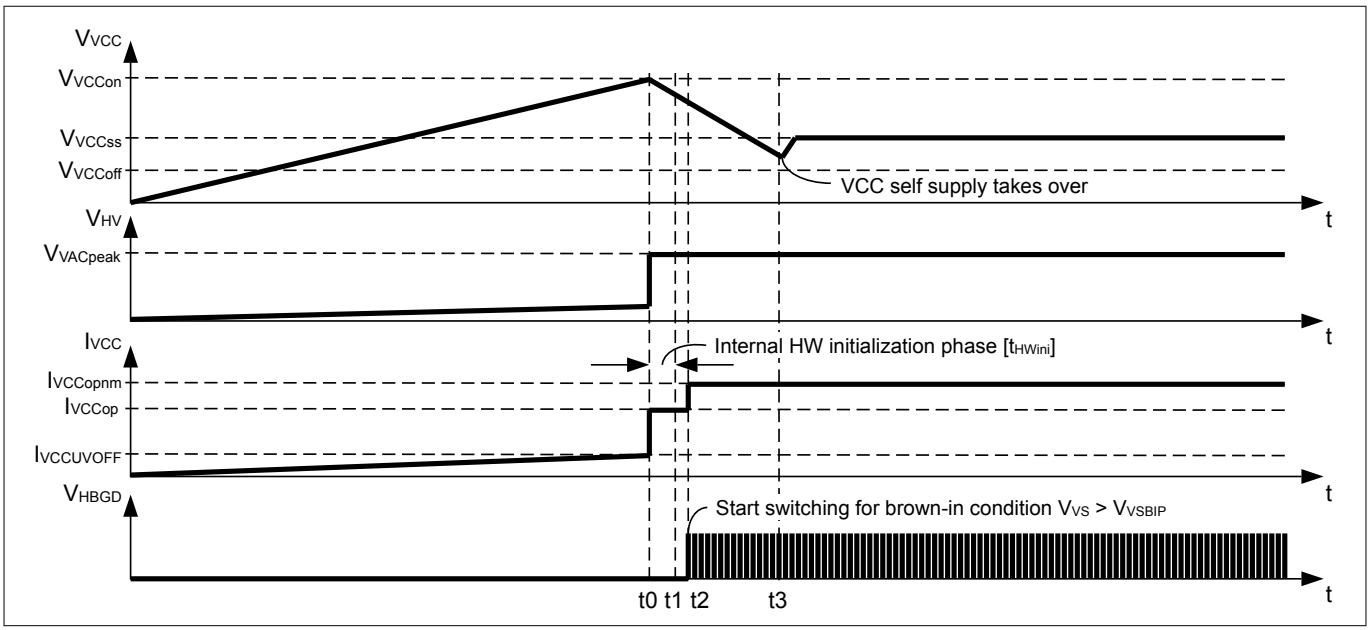


Figure 12 Typical start-up sequence

3.2.2 Bang-bang mode operation during brown-in phase

During brown-in phase the IC is observing the voltage at *VS* pin for reaching *Vin* brown-in condition. During this time VCC is not yet self-supplied via the transformer. To support a fast activation of switching operation when *Vin* brown-in condition is getting reached, the VCC voltage needs to be kept at a high level to support immediate operation with having enough time for take-over by VCC self-supply. A bang-bang mode operation

for *Vin* brown-in phase is ensuring a high VCC level, which can be either triggered by *Vin* brown-in protection or the fast and slow *Vin* brown-out protection (see ***Figure 13*** and ***Chapter 3.4.4***).

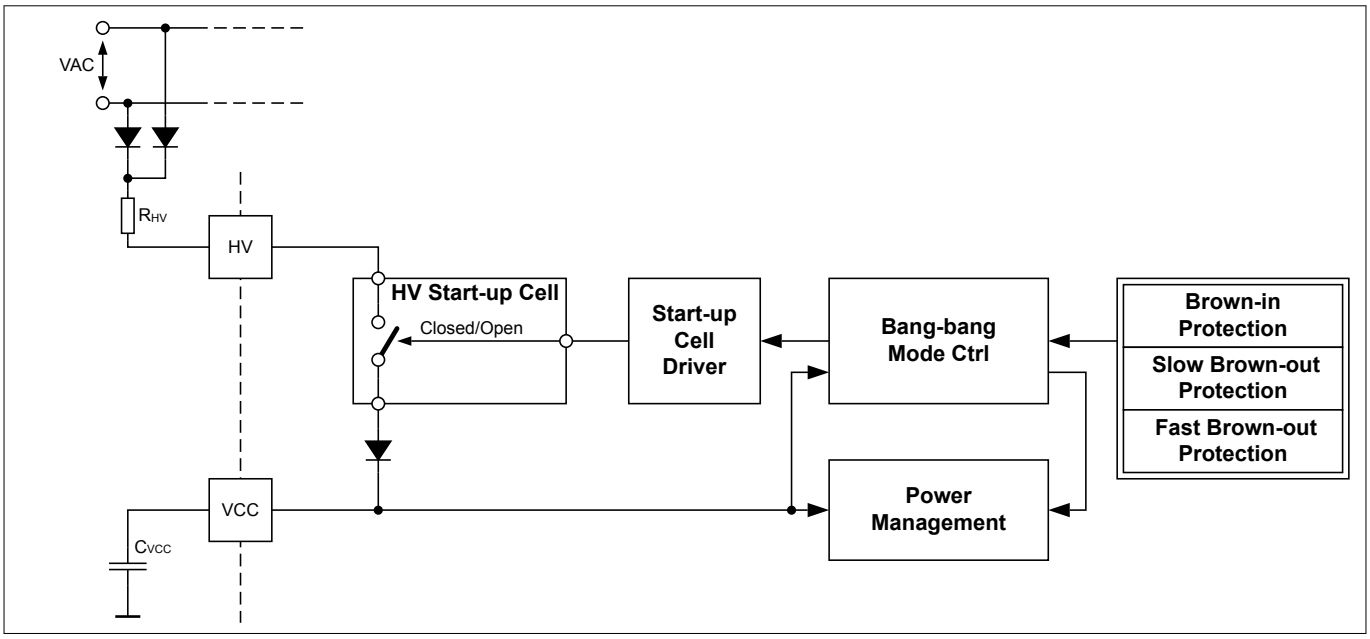


Figure 13 Bang-bang mode triggered by brown-in and brown-out

Figure 14 shows the bang-bang mode operation after a brown-out detection event. Once brown-out is detected at time t0 the IC enters immediately a sleep mode with reduced current consumption I_{VCCBB}. The HV start-up cell turns on and charges up the VCC voltage until the threshold V_{VCCon}. Then the IC is activated for a time period $t_{VSBIdet}$ in order to detect a *Vin* brown-in condition. Subsequently the IC is entering again the sleep mode. At time t1 *Vin* brown-in condition is reached but the IC is still inactive. The IC is detecting the *Vin* brown-in condition after being activated with VCC exceeding V_{VCCon} at time t2.

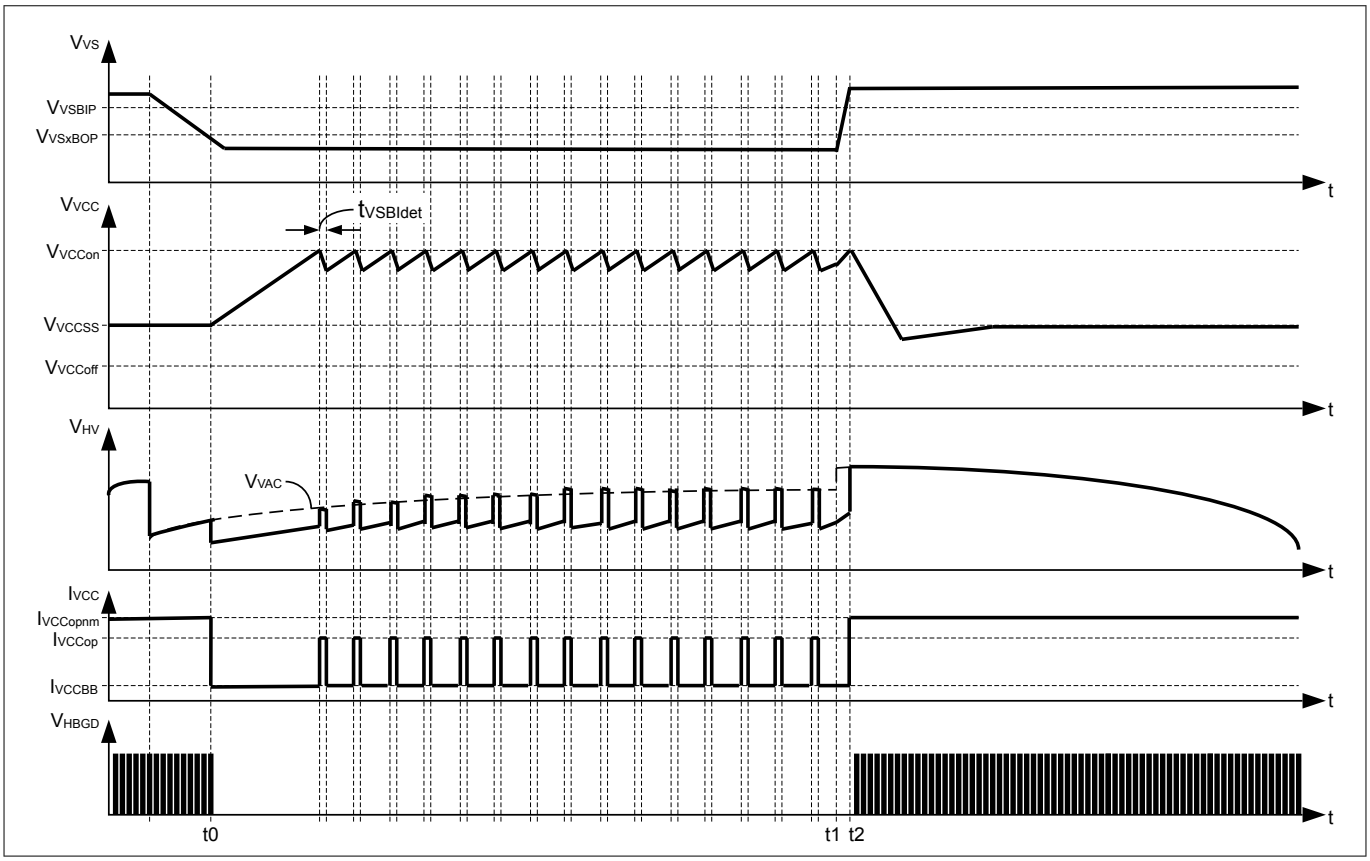


Figure 14 Bang-bang mode operation during brown-in phase

3.2.3 Bang-bang mode during protection mode operation

The bang-bang mode triggered by auto-restart mode or latch mode supports an IC operation without external VCC supply during the latched and auto-restart operation (see ***Chapter 3.4.1***). It directly controls the HV start-up cell by turning off at *VCC* pin threshold V_{VCCon} and turning on after a time period $t_{ARMbase}$ (see ***Figure 15***). During this bang-bang mode operation the VCC is kept at a high voltage level in order to support a proper restart, once triggered. The VCC current consumption is reduced to I_{VCCBB}.

In auto-restart mode, there is also in addition a counter activated, which initiates a restart after a set number of $N_{ARMstep}$ HV start-up cell charge cycles (see ***Figure 16***).

In latched operation a mode reset can only be achieved by disconnecting the AC line. A HW reset is taking place once the VCC voltage drops below the threshold V_{VCCoff}.

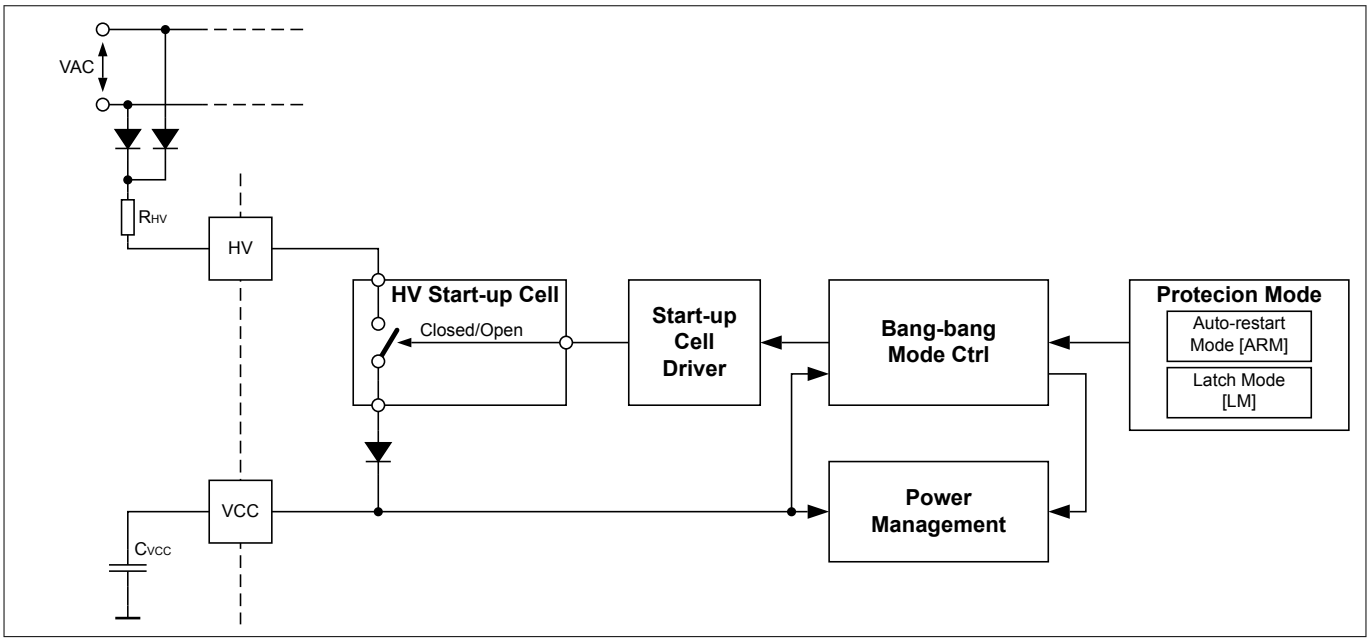


Figure 15 Bang-bang mode during protection mode

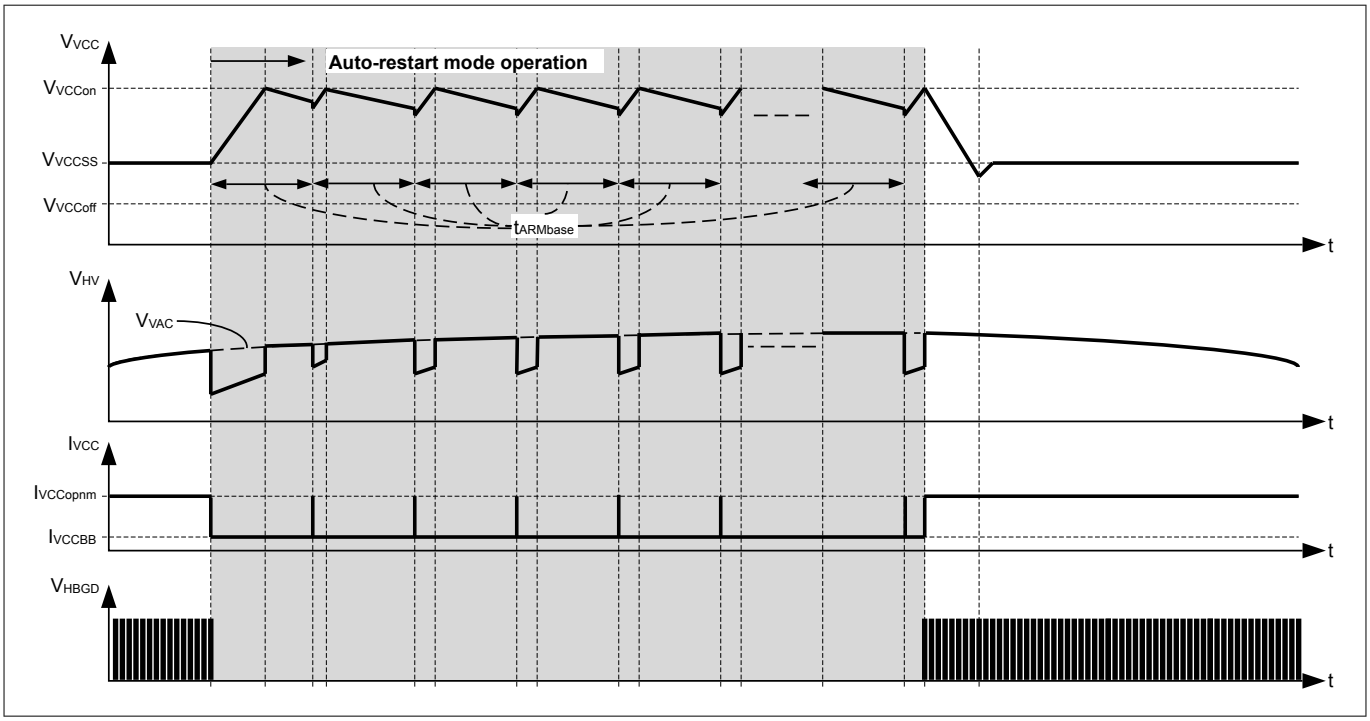


Figure 16 Auto-restart mode operation

3.2.4 VCC supply during burst mode (BM) operation

During burst mode operation the IC enters repeatedly a power saving mode, in which the IC current consumption is reduced to $I_{VCCBMpsm}$. Waking up from and entering this power saving mode is controlled by the feedback voltage at *FB* pin by comparing the voltage level with the wake-up and sleep control threshold $V_{FBBMctrl}$ (see ***Chapter 3.3.4.2***). In addition a wake-up threshold $V_{VCCslpHVon}$ is enabled at *VCC* pin, which turns-on the HV start-up cell once V_{VCC} drops below $V_{VCCslpHVon}$. This shall support a higher voltage level at *HSVCC* pin than the threshold $V_{HSVCCon}$. The HV start-up cell is turned off when either the IC is waked up via *FB* pin or

V_{VCC} is exceeding the threshold V_{VCCon}. In addition there is always only one HV start-up cell VCC charge up cycle initiated once entering the burst mode.

Note: The system dimensioning should ensure that during steady state burst mode operation V_{VCC} stays always well above the VCC wake-up threshold $V_{VCCslpHVon}$ in order to avoid increasing bias losses due to charging the VCC capacitor from input high voltage.

Figure 17 shows a typical burst mode operation signal for V_{VCC} and correlated current consumption I_{VCC} during steady state burst mode operation once feedback voltage has dropped below the burst mode entry threshold V_{FBBMen}. A large decrease of V_{VCC} can occur for a large output load drop at time *t0*, when optocoupler feedback network is entering saturation due to *Vout* overshoot. This can lead to a significant longer rising time period of feedback voltage V_{FB} until time *t2*. At time *t1* the VCC voltage is dropping below the threshold $V_{VCCslpHVon}$ and turning on the HV start-up cell. The average current $I_{HV(avg)}$ flowing into pin *HV* is depending on *VAC* and charging via *VCC* pin with $I_{VCCchrg(avg)}$ the capacitor at VCC. At time *t2* the IC is waked up via *FB* pin and the HV start-up cell is turned off. When feedback voltage is dropping below $V_{FBBMctrl}$ at time *t3* the IC is entering the power saving mode.

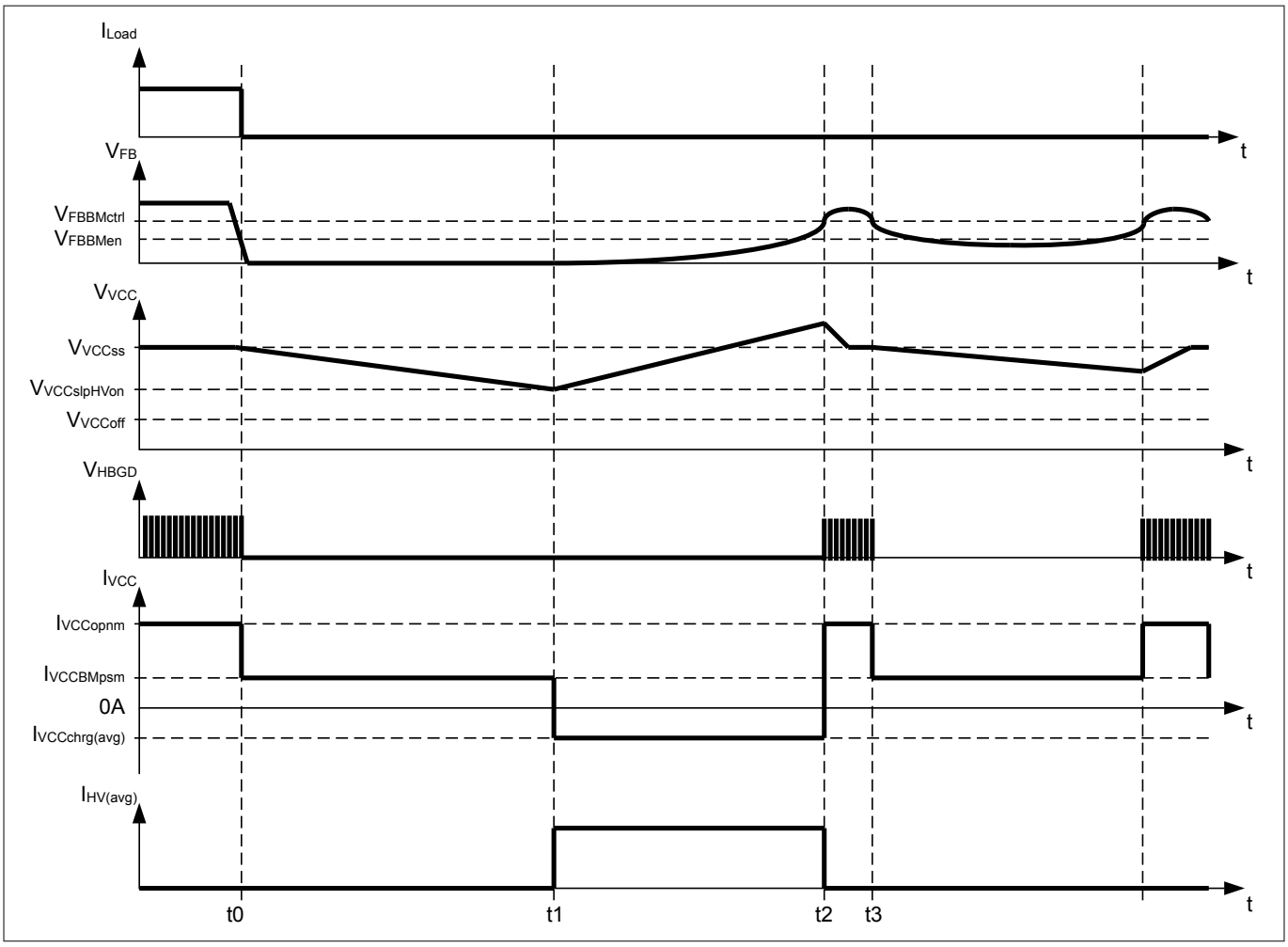


Figure 17 Burst mode operation

3.3 Control features

The control features chapter contains all functions for the hybrid-flyback PWM generation and the half-bridge gate driver listed in ***Table 2***. The hybrid-flyback PWM generation consists mainly of the mode control and output current control. The output current control is determining that part of the PWM control, which is taking place during high-side switch on-time t_{HSon} by means of peak current control (see ***Figure 18***) for the positive magnetization level I_{MAGpos}. Furthermore it provides the decision for changing the valley number in ZV-RVS operation. The PWM control ensures cycle by cycle ZVS switching operation. The mode control feature focus on controlling directly the timings of the half-bridge PWM scheme associated with the dead-times t_{deadLS}, t_{deadHS} and the low-side switch on-time t_{LSon} to determine the negative magnetization level I_{MAGneg} for the different operation modes like CRM, ZV-RVS and DCM.

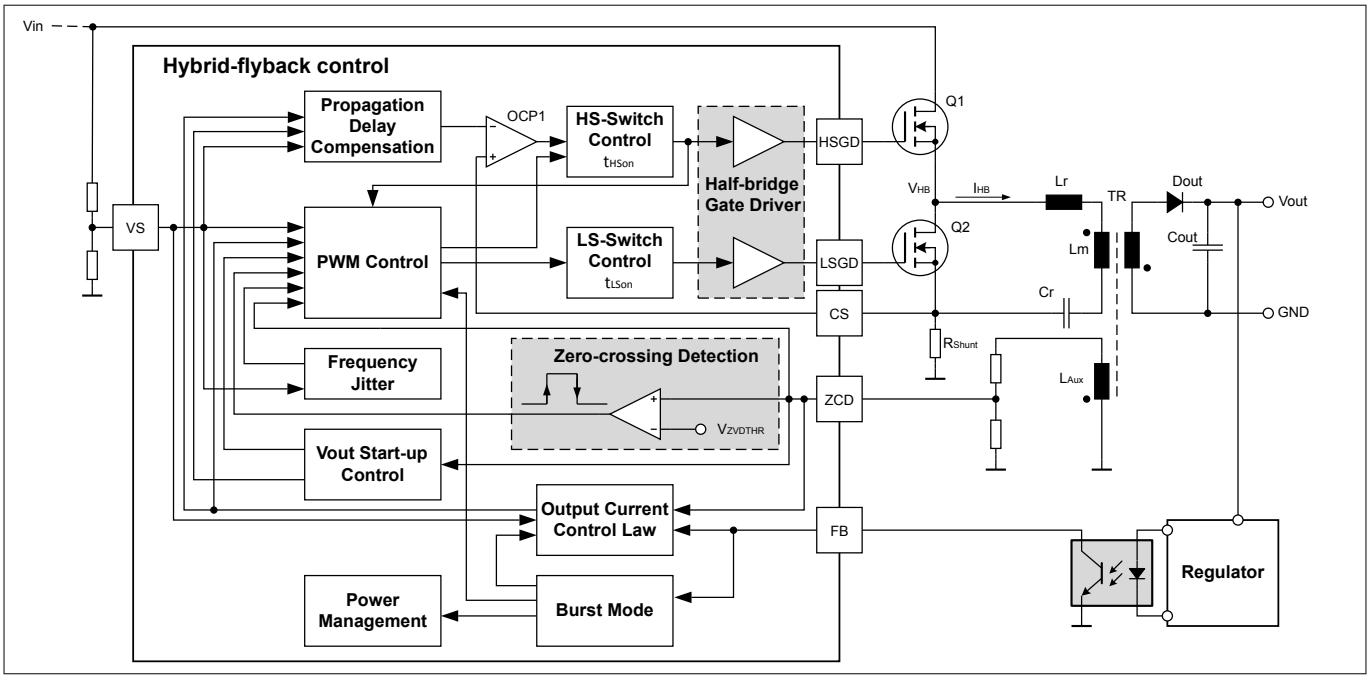


Figure 18 Hybrid-flyback control structure

Table 2 Control features

Feature	Chapter
Output control	***Chapter 3.3.1***
Mode control	***Chapter 3.3.2***
Burst mode control	***Chapter 3.3.4***
Vout start-up control	***Chapter 3.3.3***
Frequency jitter	***Chapter 3.3.5***
Half-bridge gate driver	***Chapter 3.3.6***

3.3.1 Output control

During continuous switching operation the output current is only controlled by means of the positive and negative magnetization current levels I_{MAGpos} and I_{MAGneg} following ***Equation 5***. During continuous operation the output current I_{out} is controlled by means of a linear relationship between the feedback voltage at *FB* pin and the associated internal current set-point I_{SET}, which is described in ***Chapter 3.3.1.3***. The linear relationship is achieved by adjusting I_{MAGneg} cycle by cycle via the turn-on time of *LS* switch t_{LSon} depending on the input

voltage *Vin* (see ***Chapter 3.3.1.1***) and the output voltage *Vout* (see ***Chapter 3.3.1.2***). The positive magnetization level I_{MAGpos} equals the positive half-bridge peak current that is controlled via *CS* pin at the shunt resistor R_{Shunt} (see ***Figure 19***):

$$V_{CSpeak} = I_{HBpeak} \times R_{Shunt} = I_{MAGpos} \times R_{Shunt}$$

Equation 9

The output voltage is measured via *ZCD* pin at the auxiliary winding and taken for protection features (see ***Chapter 3.4.8***) and for compensating the peak to peak magnetizing current I_{MAGpp} to ensure ZVS operation over wide output voltage range (see ***Chapter 3.3.1.2***).

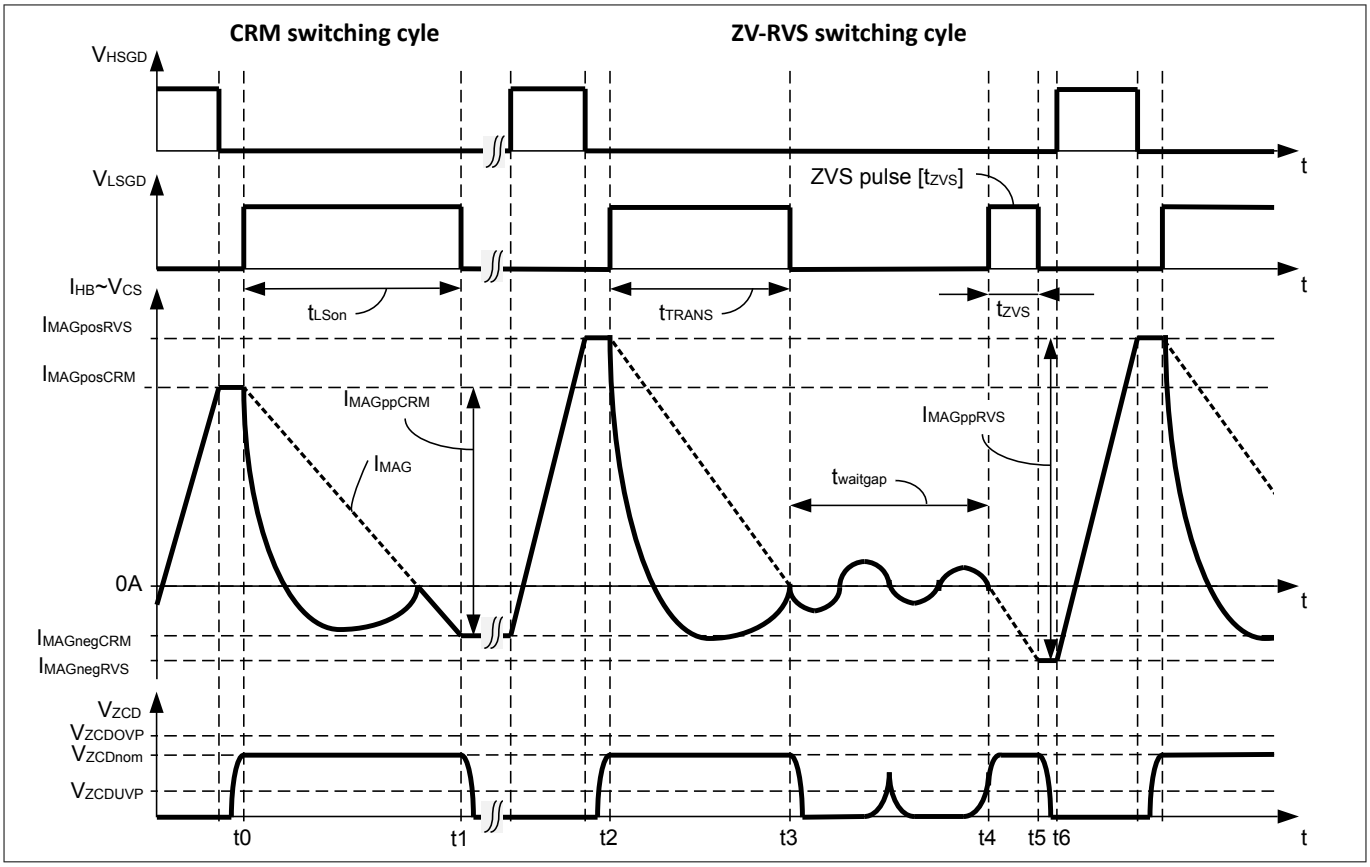


Figure 19 Negative magnetization controlled by low-side gate driver

3.3.1.1 Keeping ZVS operation for wide input voltage range

ZVS operation for wide input voltage range is achieved by *Vin* feed-forward compensation of negative magnetization level I_{MAGneg} during the different operation modes (see ***Chapter 3.3.2***). This is supported by several configurable parameters introduced in the sequel.

The implemented output current control is based on the dimensioning for the nominal output current level I_{outnom}[1)] following ***Equation 5***:

$$I_{outnom} = \frac{N}{2} \times \left(I_{MAGposnom}(\mathrm{Vin};\mathrm{Vout};\mathrm{Mode}) + I_{MAGneg}(\mathrm{Vin};\mathrm{Mode})\right)$$

Equation 10

The peak current control at *CS* pin for adjusting I_{MAGpos} is therefore depending on the input, output voltage and the mode operation that are directly impacting the negative magnetization level I_{MAGneg}.

1 configurable, see ***Table 5***

I_{MAGneg} is compensated for a changing output voltage (see ***Chapter 3.3.1.2***). Therefore the compensation for input voltage requires only set-points for minimum and maximum *Vin* (see ***Figure 20***).

Minimum *Vin*

For minimum *Vin* the natural freewheeling oscillation caused by $I_{MAGnegnom}$[2)] (see ***Figure 19***) shall support the complete switch-over of the half-bridge node.

Maximum *Vin*

For maximum *Vin* the additional required negative magnetization is set for CRM with $I_{MAGnegmaxCRM}$[2)] and for ZV-RVS with $I_{MAGnegmaxRVS}$[2)], which might be different.

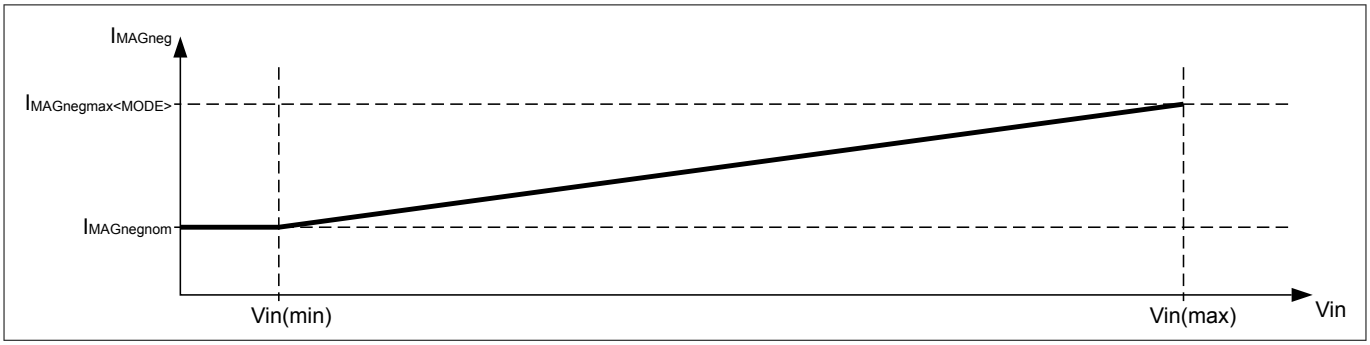


Figure 20 ***Vin* feed-forward compensation for I_{MAGneg}**

3.3.1.2 Keeping ZVS operation for wide output voltage range

When output voltage *Vout* is decreasing the demagnetization time of the transformer t_{demag} is prolonging, which leads to a longer time period t_{TRANS}. ZVS operation is ensured by adjusting the turn-on time of the *LS* switch t_{LSon} to match with the changed time period for t_{TRANS} in order to keep the same negative magnetization level I_{MAGneg} for a constant output load (see ***Figure 21***). $t_{TRANSRVS0V}$ means the time period for *Vout* = 0V and is derived from $t_{TRANSRVS0V\%}$[3)] by the following equation:

$$t_{TRANSRVS0V} = t_{TRANSRVS0V\,\%} \times t_{TRANSnom}$$

Equation 11

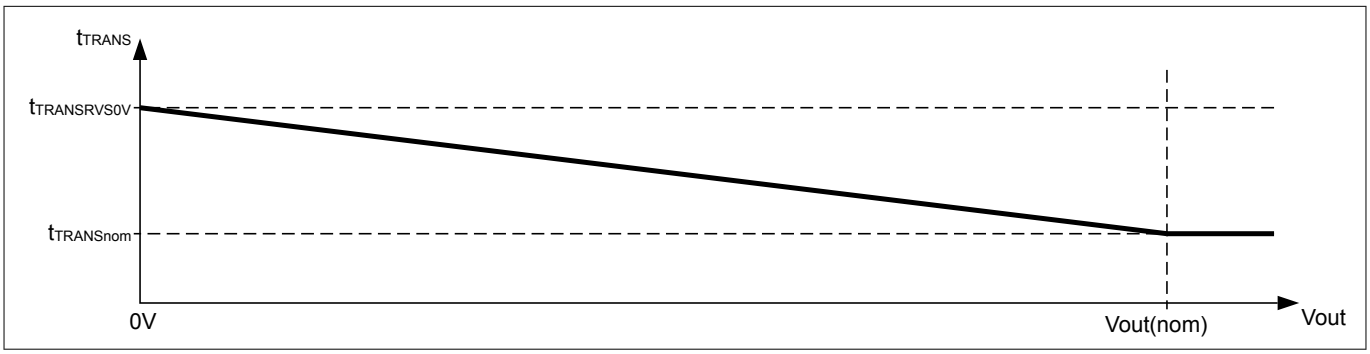


Figure 21 ***Vout* compensation for t_{TRANS}**

3.3.1.2.1 Cycle by cyle ZVS operation during CRM operation

When fast decreasing the output voltage *Vout* (see ***Figure 8***) or fast increasing the positive magnetization level I_{MAGpos} (see ***Chapter 3.3.2.5***) the demagnetization time t_{demag} of the transformer can be too short when operating with fixed *LS* switch on-time period. This can cause hard switching or even body diode cross conduction if transformer is still positive magnetized.

2 configurable, see ***Table 6***

3 configurable, see ***Table 6***

To ensure a cycle by cycle ZVS switching condition, the controller only activates the *HS* switch when the voltage signal at *ZCD* pin (see ***Figure 18***) indicates a changing half-bridge voltage V_{HB}. By this body diode cross conduction is properly avoided. This is achieved by regulating I_{MAGneg} for a target delay time t_{LS2ZCD} between falling edge of *LS* switch and subsequently occurring falling edge at *ZCD* pin (see ***Figure 22***).

The polarity of the transformer auxiliary winding L_{AUX} has to be considered in such a way that a rising V_{HB} is leading to a falling V_{ZCD}. The time between turning off the *LS* switch until zero-crossing detection for turning on the high-side switch t_{LS2ZCD} is observed and determining a prolongation of next turn-on phase for *LS* switch if required to ensure reliable ZVS operation.

An example is shown with phase t2-t3 in comparison to phase t6-t7. The dead-time $t_{deadHS1}$ is determined by the negative half-bridge current level $I_{MAGneg1}$. The small level of $I_{MAGneg1}$ leads to a rather slow rising slope of V_{HB}. The detection of zero-crossing at *ZCD* pin is delayed and turn-on of *HS* switch is not taking place under full ZVS condition at time t3. The increased delay of zero-crossing after having turned off *LS* switch is taken as input for increasing indirectly the negative half-bridge current level to $I_{MAGneg2}$ by extending the turn-on time of *LS* switch in phase t5-t6. ZVS condition for turning on the *LS* switch are reached by properly dimensioning the dead-time t_{deadLS} (see ***Chapter 3.3.2.1***).

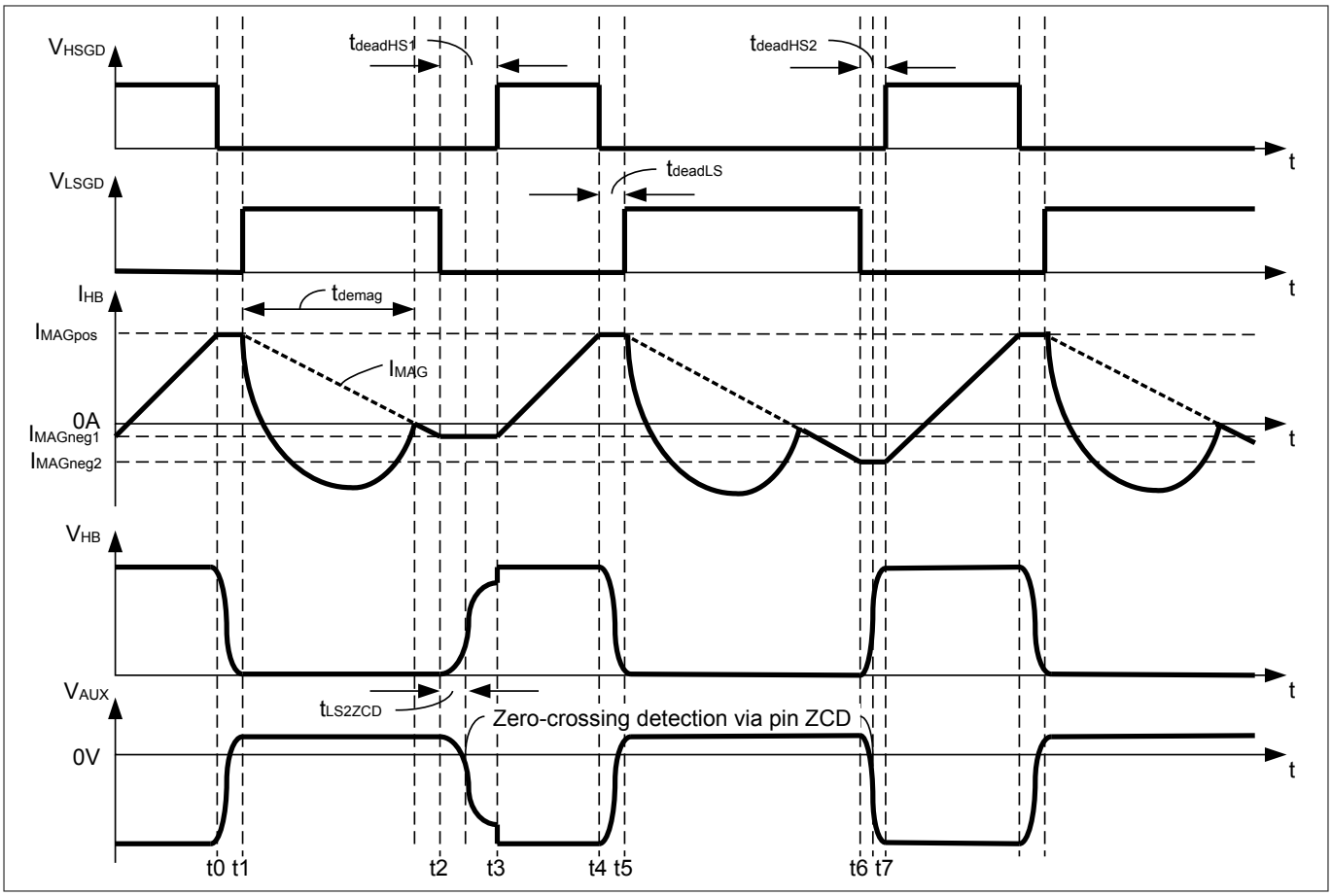


Figure 22 Using zero-crossing detection at L_{AUX} to ensure ZVS operation

Only in DCM operation at very light-load partial hard switching can occur for the first *LS* switching cycle turn-on. This is only taking place after a long waiting period when demagnetization of the transformer is finished not causing a body diode conduction issue (see ***Chapter 3.3.2.3***).

3.3.1.3 Output current control law

Figure 23 shows the control path from feedback signal input at *FB* pin to peak current setting at *CS* pin. The requested output current equals to the internal I_{SET} for the corresponding feedback signal. The required peak current setting is then calculated based on *Vin* measurement and mode operation.

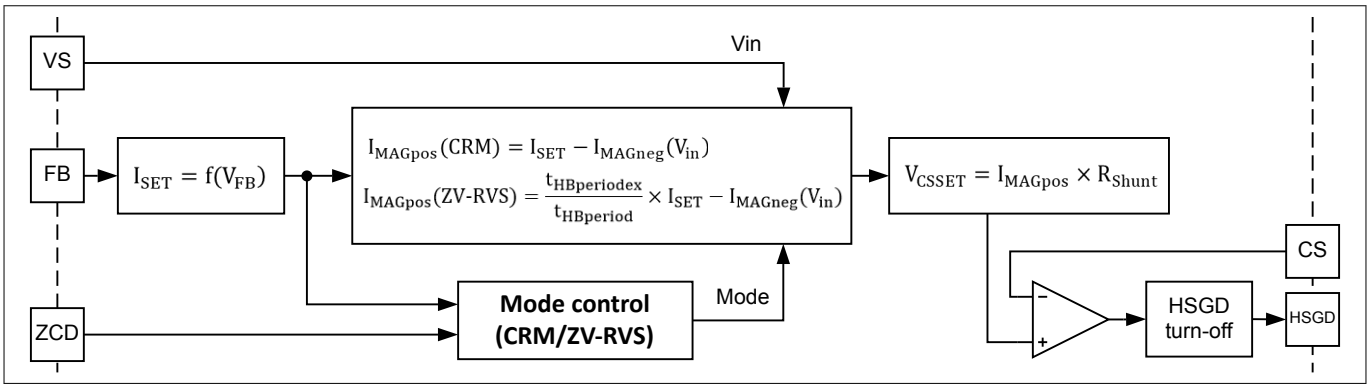


Figure 23 Control path from feedback input to peak current setting

The feedback voltage V_{FB} has a linear correlation with the output current I_{out} between the boarders for maximum output current $I_{outOCP1max}$ and burst mode entry current level $I_{outBMen}$. ***Figure 24*** is showing output current levels for various functions.

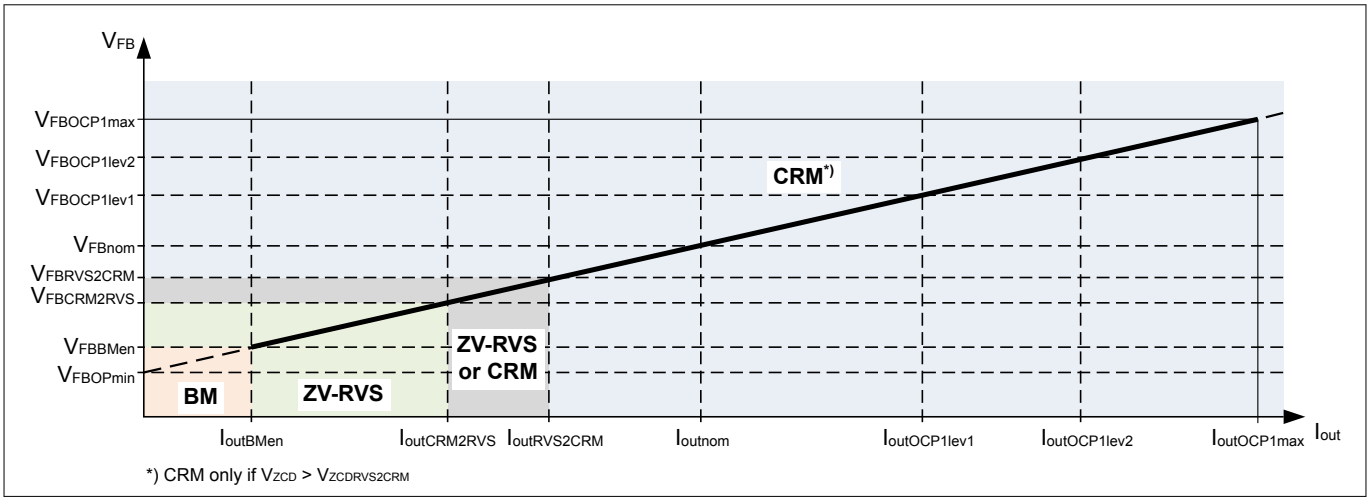


Figure 24 Control law for feedback voltage at *FB* pin

Controlling the output current I_{out} is determined by the equivalent internal current set-point I_{SET}, which is then taken for the peak current setting at *CS* pin to adjust the positive magnetization level I_{MAGpos}. The correlation between I_{SET} and I_{MAGpos} is different for CRM (see ***Chapter 3.3.1.3.1***) and ZV-RVS mode (see ***Chapter 3.3.1.3.2***) in order to ensure a smooth transition between the CRM and ZV-RVS mode. ***Figure 25*** shows the configurable current set-points for various functions and their correlation with the feedback voltage.

The configurable current set-points $I_{SETxxx\%}$ are defined in percentage with respect to the nominal current set-point $I_{SETnom\%}$ that determines in percentage of the *FB* pin operating voltage range $V_{FBOPmax}$ the associated voltage level V_{FBnom}. Here $I_{SETnom\%}$ is set to 50% used as a factor without unit.

$$V_{FBnom} = (I_{SETnom\,\%} \times V_{FBOPmax}) + V_{FBOPmin}$$

Equation 12

*Note: The current set-point for burst mode exit threshold $I_{SETBMex\%}$ is only active during burst mode operation and only used as an internal parameter for comparison, which is not associated with a feedback voltage level (see **Chapter 3.3.4.4.1**). The same applies for $I_{SETstmax\%}$ that is only active during Vout start-up control (see **Chapter 3.3.3**) to provide additional output charge current.*

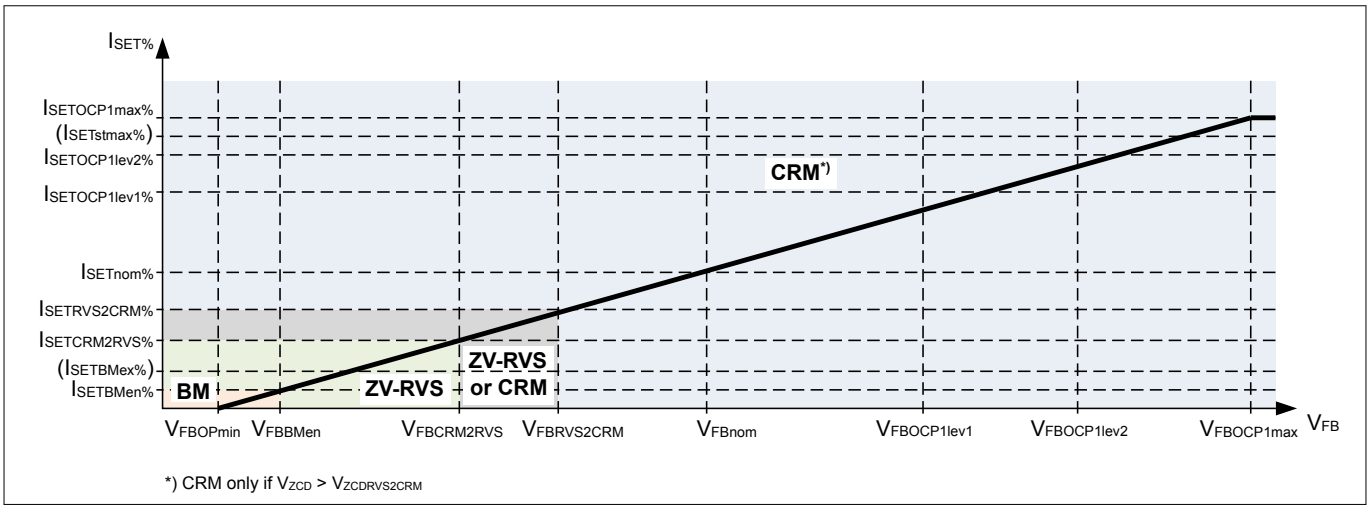


Figure 25 Configurable internal current set-points $I_{SETxxx\%}$ and correlation with V_{FB}

For all other current set-points $I_{SETxxx\%}$ the correlated feedback voltage V_{FBxxx} can be calculated as following:

$$V_{FBxxx} = (I_{SETxxx\,\%} \times I_{SETnom\,\%} \times V_{FBOPmax}) + V_{FBOPmin}$$

Equation 13

The offset $V_{FBOPmin}$ considers the minimum operating voltage level of the opto-coupler output before entering saturation.

The peak current setting at *CS* pin is done by comparing the voltage at the shunt resistor R_{Shunt} with the internally derived threshold V_{CSxxx}:

$$I_{MAGxxx} = \frac{V_{CSxxx}}{R_{Shunt}}$$

Equation 14

V_{CSxxx} is beside $I_{SET\%}$ also depending on *Vin* and the mode operation (see ***Chapter 3.3.1.1***) shown by following relationship:

CRM operation

$$V_{CSxxx} = (I_{SETxxx\,\%} \times I_{SETnom\,\%} \times V_{CSOPmax}) + \left(I_{MAGneg}(\mathrm{Vin}) \times R_{Shunt}\right)$$

Equation 15

ZV-RVS operation

$$V_{CSxxx} = \frac{t_{HBperiodex}}{t_{HBperiod}} \times \left[(I_{SETxxx\,\%} \times I_{SETnom\,\%} \times V_{CSOPmax}) + \left(I_{MAGneg}(\mathrm{Vin}) \times R_{Shunt}\right)\right]$$

Equation 16

Hereby $V_{CSOPmax}$ is the maximum operating voltage range at *CS* pin. R_{Shunt} dimensioning is based on nominal output current I_{outnom} at nominal current set-point $I_{SETnom\%}$, where $I_{SETnom\%}$ also determines in percentage of $V_{CSOPmax}$ at *CS* pin the associated voltage level $V_{CSOPnom}$.

$$R_{Shunt} = \frac{N}{2} \times \frac{I_{SETnom\,\%} \times V_{CSOPmax}}{I_{Outnom}}$$

Equation 17

At the corners for *Vin(min)* and *Vin(max)* the expected peak current setting for nominal current set-point $I_{SETnom\%}$ can be calculated with:

Minimum peak current setting V_{CSnom}*(min)* for nominal load at *Vin(min)*

CRM operation

$$V_{CSnom(min)} = (I_{SETnom\,\%} \times V_{CSOPmax}) + \left(\left(I_{MAGnegnom\,\%} \times \frac{2 \times I_{Outnom}}{N}\right) \times R_{Shunt}\right)$$

Equation 18

ZV-RVS operation

$$V_{CSnom(min)} = \frac{t_{HBperiodex}}{t_{HBperiod}} \times \left(\left(I_{SETnom\,\%} \times V_{CSOPmax}\right) + \left(\left(I_{MAGnegnom\,\%} \times \frac{2 \times I_{Outnom}}{N}\right) \times R_{Shunt}\right)\right)$$

Equation 19

Maximum peak current setting V_{CSnom}*(max)* for nominal load at *Vin(max)*

CRM operation

$$V_{CSnom(max)} = (I_{SETnom\,\%} \times V_{CSOPmax}) + \left(\left(I_{MAGnegmaxCRM\,\%} \times \frac{2 \times I_{Outnom}}{N}\right) \times R_{Shunt}\right)$$

Equation 20

ZV-RVS operation

$$V_{CSnom(max)} = \frac{t_{HBperiodex}}{t_{HBperiod}} \times \left(\left(I_{SETnom\,\%} \times V_{CSOPmax}\right) + \left(\left(I_{MAGnegmaxRVS\,\%} \times \frac{2 \times I_{Outnom}}{N}\right) \times R_{Shunt}\right)\right)$$

Equation 21

3.3.1.3.1 Current control during CRM

During CRM operation the negative magnetization I_{MAGneg} is controlled for a target value only depending on input voltage *Vin* (see ***Chapter 3.3.1.1***). Here the negative magnetization I_{MAGneg} is controlled by adjusting the on-time t_{LSon}, which leads to a linear correlation between I_{out} and the set positive magnetization level I_{MAGpos}:

$$I_{out} = \frac{N}{2} \times \left(I_{MAGpos}(\mathrm{Vin}) + I_{MAGneg}(\mathrm{Vin})\right)$$

Equation 22

I_{MAGpos} is then controlled by the peak current control at *CS* pin based on the correlation with the internal target current set-point I_{SET}, which is a proportional representation of the output current I_{out}:

$$I_{SET} = \frac{2}{N} \times I_{out}$$

Equation 23

$$I_{MAGpos}(I_{SET}; \mathrm{Vin}) = I_{SET} - I_{MAGneg}(\mathrm{Vin})$$

Equation 24

When reducing the load the on-time of *LS* switch is getting reduced until the minimum time period $t_{TRANSnom}$. For further reduction in load the on-time of *LS* is kept constant, which results in a constant peak to peak magnetization I_{MAGpp} (see ***Figure 19***):

$$I_{MAGpp} = I_{MAGpos} - I_{MAGneg}$$

Equation 25

3.3.1.3.2 Current control during ZV-RVS mode

As in ZV-RVS mode the peak current control for I_{MAGpos} shall be kept almost constant (see ***Chapter 3.3.2.2.1***) to ensure that the demagnetization time is longer than half of the resonant period of the *LrCr* tank, a waiting time gap $t_{waitgap}$ is introduced directly after the end of $t_{TRANSnom}$ period (see ***Figure 19***), which is extending the half-bridge period to $t_{HBperiodex}$. This results in a reduced output current I_{out} that can be expressed as:

$$I_{out} = \frac{t_{HBperiod}}{t_{HBperiodex}} \times \frac{N}{2} \times \left(I_{MAGpos} + I_{MAGneg}\right)$$

Equation 26

The control for $t_{HBperiodex}$ is performed by means of valley skipping control (see ***Chapter 3.3.2.2.1***) depending on I_{SET} and *Vin*:

$$t_{HBperiodex}(I_{SET}; \mathrm{Vin}) = t_{HBperiod} \times \frac{\left(I_{MAGpos} + I_{MAGneg}(\mathrm{Vin})\right)}{I_{SET}}$$

Equation 27

3.3.1.4 Propagation delay compensation (PDC)

During peak current control a propagation delay is impacting the resulting peak current limitation (see ***Figure 26***). The higher reached peak current is then compensated to a lower level by the closed application control loop via the feedback signal at *FB* pin. The magnitude of $I_{MAG\ pos}$ overshoot is depending on the voltage at the transformer input winding *Lm*, which is depending on input voltage *Vin* and reflected output voltage at resonant capacitor V_{Cr}. A higher voltage amplitude at the transformer input winding leads to a steeper rising slope of I_{MAGpos} and vice versa. A total delay of $t_{PDCOPC1}$ leads then to a delta overshoot of $\Delta I_{MAGposcomp}$:

$$\Delta \mathrm{I}_{MAGposcomp} = \frac{(\mathrm{Vin} - V_{Cr})}{\mathrm{Lm}} \times t_{PDCOPC1}$$

Equation 28

$t_{PDCOPC1}$ consists of an internal delay t_{PDint} caused by the OCP1 comparator, gate driver and an external delay t_{PDext} caused by the power switch turn-off and parasitic capacitance connected to the half-bridge node.

$$t_{PDCOCP1} = t_{PDint} + t_{PDext}$$

Equation 29

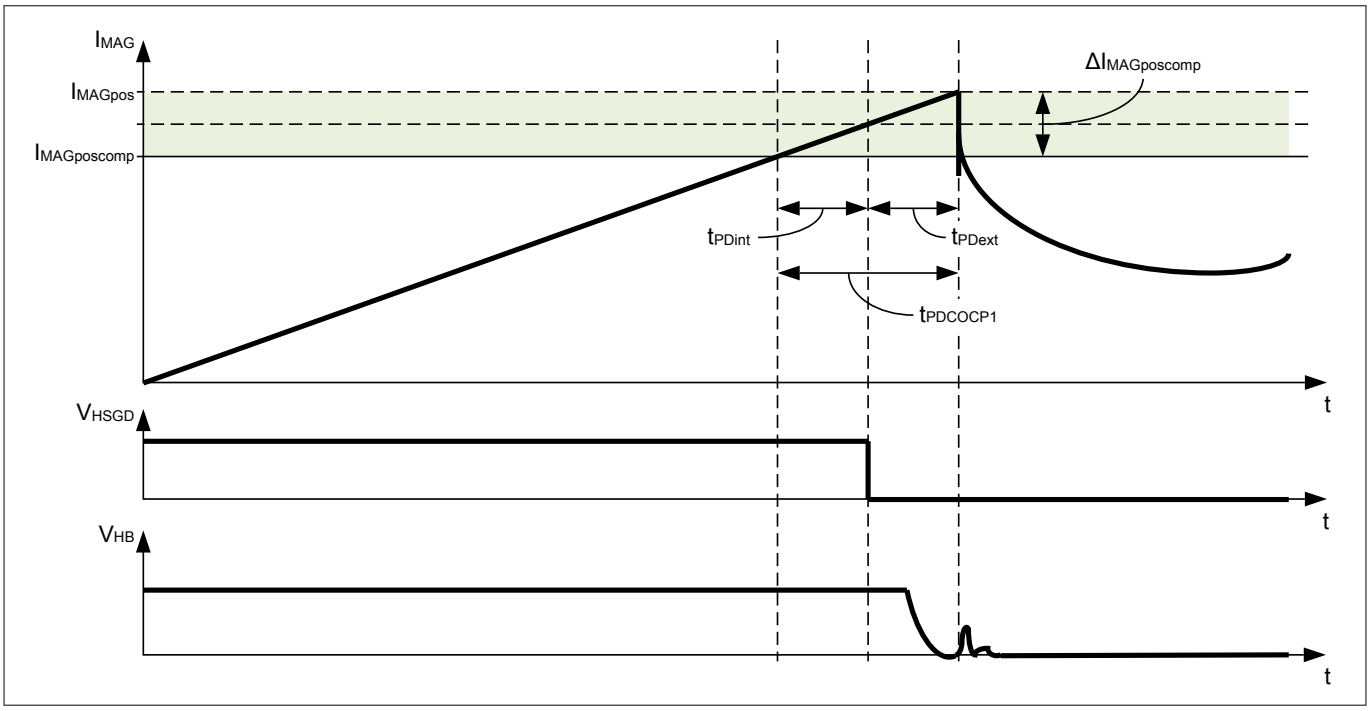


Figure 26 Propagation delay compensation of peak current control for I_{MAGpos}

This dependency on *Vin* and V_{Cr} impacts the current set-point threshold accuracy seen in the application and is therefore compensated to avoid errors on the feedback signal V_{FB}.

The propagation delay compensation uses ***Equation 28*** to calculate $\Delta I_{MAGposcomp}$ based on the parameter $t_{PDCOPC1}$[4], the measured input voltage at *VS* pin and measured reflected output voltage at *ZCD* pin. *Lm* is extracted from other configurable parameters as following:

$$\mathrm{Lm} = \frac{V_{\mathrm{VSVCRnom}} \times t_{\mathrm{TRANSnom}}}{I_{\mathrm{MAGpp}}}$$

Equation 30

The peak current setting is then compensated by reducing the internal target peak current set-point I_{MAGpos} with $\Delta I_{MAGposcomp}$:

$$I_{\mathrm{MAGposcomp}} = I_{\mathrm{MAGpos}} - \Delta I_{\mathrm{MAGposcomp}}$$

Equation 31

3.3.2 PWM control schemes

Table 3 shows the list of features that describes the pulse width modulation (PWM) control methods for the different control modes and the associated mode transition. Depending on load, output voltage, and input voltage (see ***Chapter 3.3.1***) the control scheme is adjusted to ensure ZVS operation for both low-side and high-side switches.

4 configurable, see ***Table 21***

Table 3 PWM control

Feature	Chapter
CRM control scheme	***Chapter 3.3.2.1***
ZV-RVS mode control scheme	***Chapter 3.3.2.2***
DCM control scheme	***Chapter 3.3.2.3***
Mode transition control	***Chapter 3.3.2.4***
Overcurrent control	***Chapter 3.3.2.5***

3.3.2.1 CRM control scheme

The PWM control targets a ZVS operation for every half-bridge switching cycle by cycle by tuning the negative current level I_{MAGneg} (see ***Figure 27***) . The dead-time t_{deadLS}[5)] between *HS* and *LS* switch is fixed as the peak current is high enough to provide proper ZVS operation for *LS* switch.

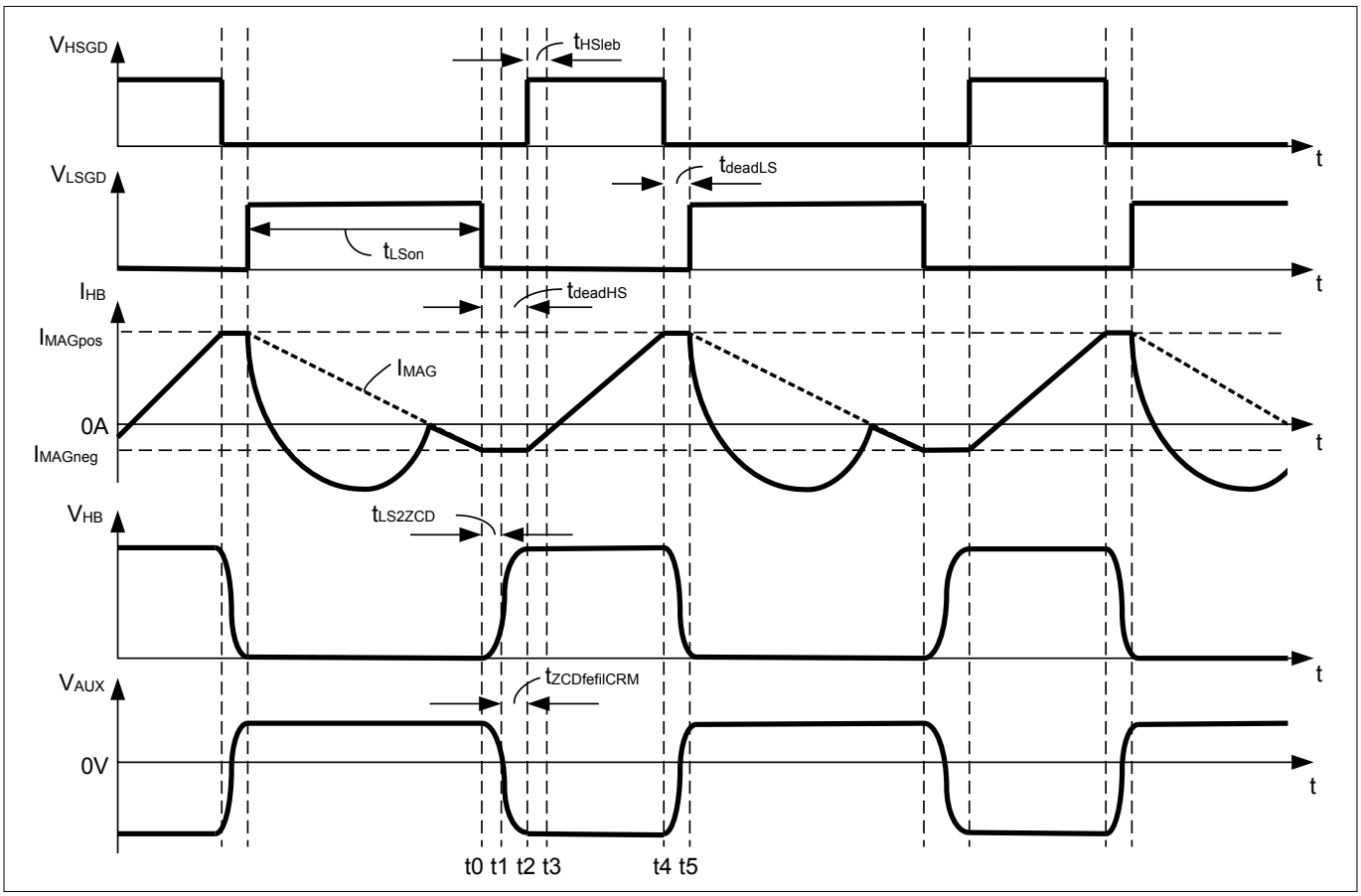


Figure 27 Half-bridge timings for CRM operation

The dead-time t_{deadHS} is depending on input voltage and mode operation. In CRM operation it consists of 2 time periods:

5 configurable, see ***Table 7***

$$t_{\text{deadHS}}(\text{Vin};\text{CRM}) = t_{\text{LS2ZCD}}(\text{Vin}) + t_{\text{ZCDfefilCRM}}$$

Equation 32

The time period t_{LS2ZCD} is captured after turning off *LS* switch at time t0 until zero-crossing detection at time t1 and compared with a target value based on *Vin*. The shortest time period $t_{\text{LS2ZCDmin}}$[5] occurs at maximum input voltage, whereas the longest time period $t_{\text{LS2ZCDnom}}$[5] is correlated with minimum input voltage (see ***Figure 28***).

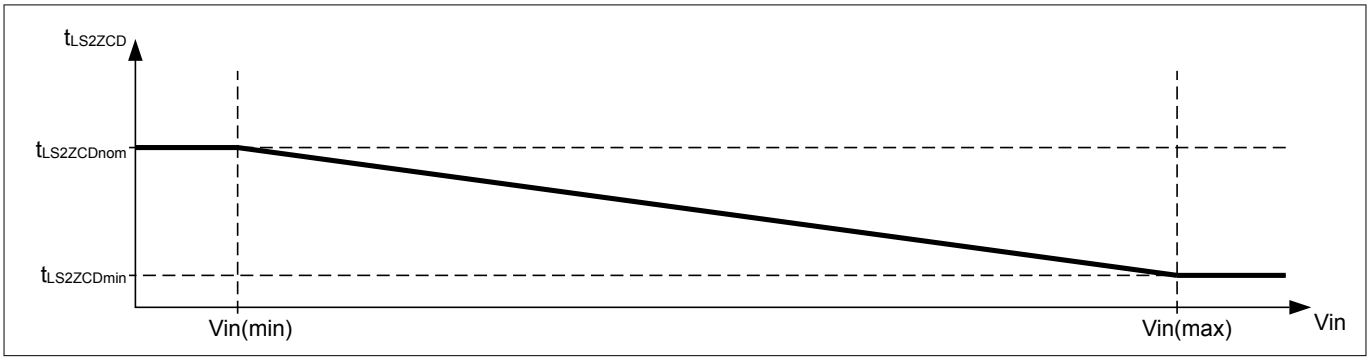


Figure 28 Adaptive target time period for t_{LS2ZCD}

In the subsequent half-bridge switching cycle the *LS* switch on-time t_{LSon} is adjusted by Δt_{LSon}

$$\Delta t_{\text{LSon}} = t_{\text{LS2ZCD}}(\text{Vin}) - t_{\text{LS2ZCDcap}}$$

Equation 33

with $t_{\text{LS2ZCDcap}}$ being the captured time period.

Extending t_{LSon} increases the negative magnetization level I_{MAGneg}, which then reduces the time for switching-over the half-bridge node. In this way the negative magnetization is being self-adjusted to the defined target value as shown in ***Chapter 3.3.1.1*** and supporting an internal accurate output current estimation for peak current setting at *CS* pin.

When reducing t_{LSon} the minimum is determined by t_{TRANSnom}[5] at maximum output voltage level.

The 2nd part of t_{deadHS} is defined by the fixed time period $t_{\text{ZCDfefilCRM}}$[5], which is delaying the *HS* switch turn-on at time t2 after zero-crossing detection at time t1 (see ***Figure 27***).

After *HS* switch is turned on the peak current limitation only takes place after a leading edge spike blanking period t_{HSleb}[5], which determines also the minimum on-time of *HS* switch operation.

3.3.2.2 ZV-RVS control scheme

The relevant timings for ZV-RVS mode operation with ZVS pulse generation are shown in ***Figure 29***). During ZV-RVS mode a waiting time gap t_{waitgap} is inserted at time t0 after a *HS* and *LS* switch half-bridge cycle to control the output current (see ***Chapter 3.3.1.3.2***). The ZVS pulse t_{ZVS} is initiated by turning on the *LS* switch after the rising edge zero-crossing detection target number at time t1 and a delay time period $t_{\text{ZCDrefilRVS}}$[6]. The dead-time for turning on the *HS* switch after the ZVS pulse is fixed with $t_{\text{deadHSRVS}}$[6]. The subsequent dead-time t_{deadLS} is same as in CRM operation.

The required ZVS pulse length t_{ZVS} is determined by the target negative magnetization level I_{MAGneg}, the transformer magnetizing inductance *Lm* and depending on output voltage *Vout*:

5 configurable, see ***Table 7***
6 configurable, see ***Table 8***

$$t_{ZVS} = \frac{I_{MAGneg} \times Lm}{N \times V_{OUT}}$$

Equation 34

I_{MAGneg} is adapted for changes in input voltage (see ***Chapter 3.3.1.1***). The minimum ZVS pulse length occurs when both lowest input voltage and highest output voltage applies. Here the parameter t_{ZVSmin} [7] is limiting the minimum adjustable ZVS pulse length.

Note: The minimum t_{ZVSmin} shall be equal or longer than the minimum on-time of the SR controller for proper operation.

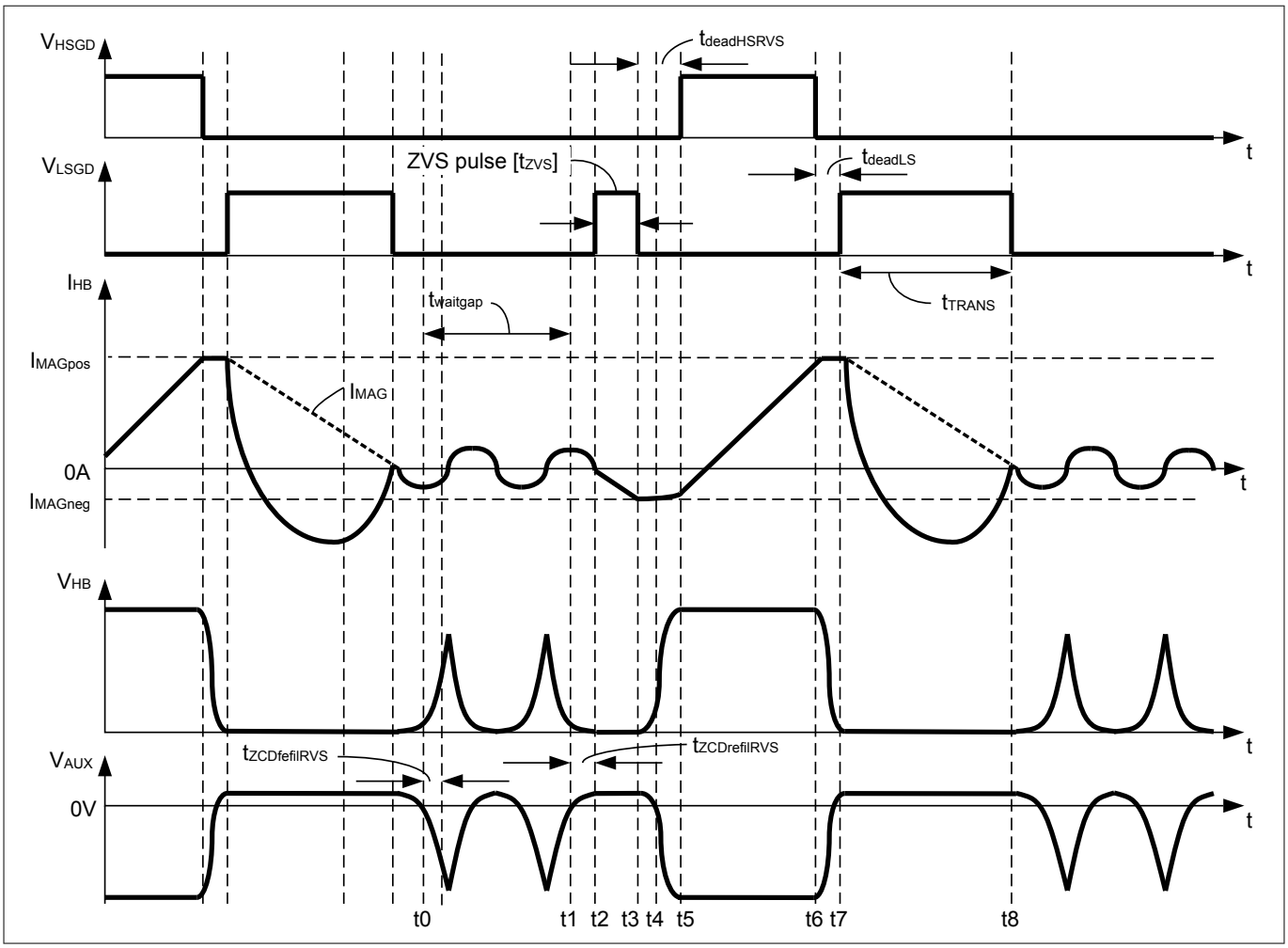


Figure 29 Half-bridge timings for ZV-RVS mode operation

3.3.2.2.1 Valley skipping control

When operating in ZV-RVS mode, valley detection is taking place to determine the time for turning on the ZVS pulse (see ***Figure 29***). The waiting time after transformer demagnetization $t_{waitgap}$ is controlled based on the target number of detected valleys. A valley is counted once a falling edge of the ZCD signal is detected after a filter $t_{ZCDfefilRVS}$ [8]. The target number for valley detection is adjusted every half-bridge switching cycle depending on exceeding the thresholds $I_{MAGposRVS(+)}$ or $I_{MAGposRVS(-)}$. The target valley number is increased once

7 configurable, see ***Table 8***

8 configurable, see ***Table 8***

the internally derived peak current setting I_{MAGpos} is dropping below $I_{MAGposRVS(+)}$ and decreased when exceeding $I_{MAGposRVS(-)}$. Hence a hysteresis is built in order to avoid value jumping during steady state operation. The hysteresis magnitude can be calculated with:

$$I_{MAGposRVShys} = \frac{1}{3} \times I_{MAGposnom}$$

Equation 35

Both thresholds are depending on the output voltage measured via *ZCD* pin. The value is decreasing with decreasing output voltage as shown in ***Figure 30***. As a result the peak current setting at *CS* pin is kept almost constant between the two thresholds $I_{MAGposRVS(-)}$ and $I_{MAGposRVS(+)}$ for a given output voltage. The threshold $I_{MAGposRVS(+)}$ is determined by the two points for $I_{MAGposnom}$ at nominal output voltage and $I_{MAGposRVS0V}$ for *Vout* = 0V. $I_{MAGposRVS0V}$ is defined by $I_{MAGposRVS0V\%}$[9] with following equation:

$$I_{MAGposRVS0V} = I_{MAGposRVS0V\,\%} \times I_{MAGposnom}$$

Equation 36

The maximum number of requested target valleys is limited and leads to a mode change to DCM (see ***Chapter 3.3.2.4***).

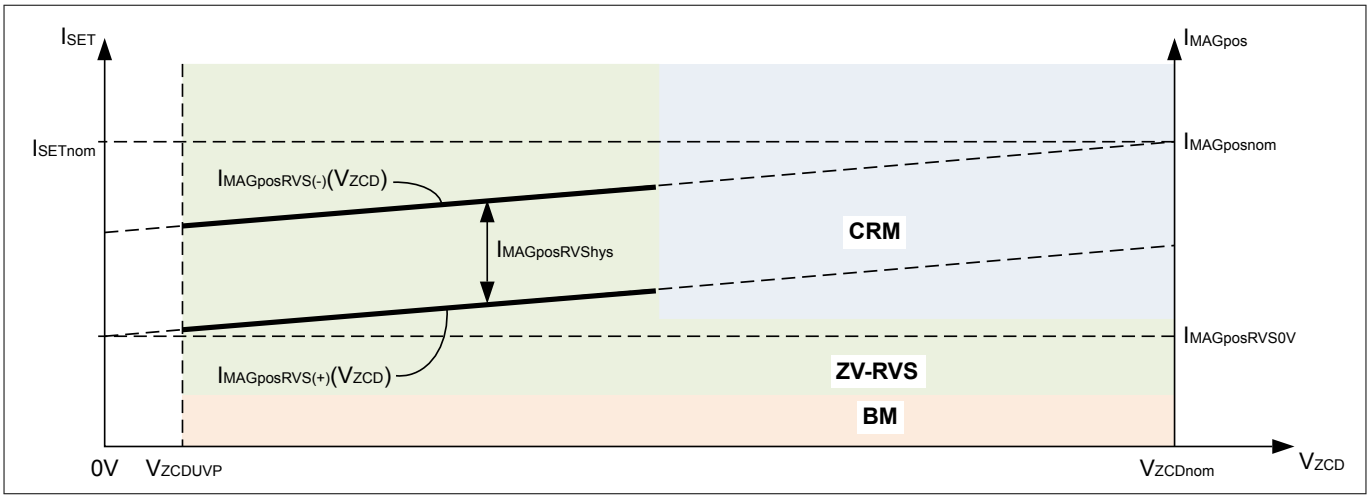


Figure 30 Valley skipping control for adjusting $t_{waitgap}$

3.3.2.3 DCM control scheme

The DCM control is associated with triggering the ZVS pulse in ZV-RVS mode operation. ZV-RVS mode operation at light-load is limited by the maximum number of detectable zero-crossings at *ZCD* due to decreasing oscillation magnitude with prolongation of the inserted waiting time gap $t_{waitgap}$ (see ***Figure 10***). When further reducing the output current the waiting time gap $t_{waitgap}$ is further increased until the ZVS pulse is initiated without zero-crossing detection. The subsequent half-bridge cycle is then again performed under ZVS condition (see ***Chapter 3.3.2.2***).

Increasing $t_{waitgap}$ takes only place until the extended half-bridge period $t_{HBperiodex}$ (see ***Chapter 3.3.2.2***) reaches the associated minimum half-bridge switching frequency F_{DCMmin}[10]. When output current is further decreased, the feedback voltage V_{FB} drops until it exceeds the burst mode entry threshold (see ***Chapter 3.3.4.1***).

The DCM operation can be disabled by means of EN_{DCM}[10].

9 configurable, see ***Table 6***
10 configurable, see ***Table 9***

3.3.2.4 Mode transition control

Mode transition between CRM and ZV-RVS mode

The mode transition control observes the signal levels at *FB* and *ZCD* pins for exceeding thresholds that define the changeover from CRM to ZV-RVS mode and vice versa. The feedback signal V_{FB} is determining the internal current set-point $I_{SET\%}$ and compared with the current set-point thresholds (see ***Chapter 3.3.1.3***). During operating in CRM the thresholds $I_{SETCRM2RVS\%}$[11)] and $V_{ZCDCRM2RVS}$[11)] at *ZCD* pin are determining the switchover to ZV-RVS mode. Operating in ZV-RVS mode the thresholds $I_{SETRVS2CRM\%}$[11)] and $V_{ZCDRVS2CRM}$[11)] at *ZCD* pin are determining the switchover to CRM.

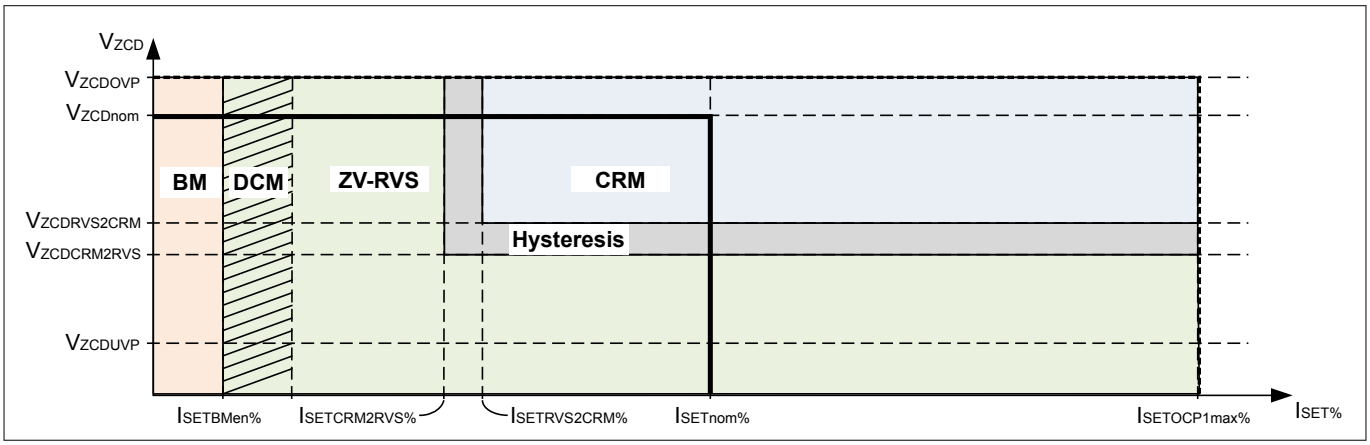


Figure 31 Mode transition between CRM and ZV-RVS mode

Mode transition between ZV-RVS mode and DCM

The DCM operation takes place once the control loop requests for operating beyond the maximum number of valley switching $N_{RVSvalmax}$[12)] (see ***Chapter 3.3.2.2.1***). After entering DCM operation the peak current setting is slightly increased by adding an offset of 25% of the set $I_{MAGposRVS(+)}$. During DCM operation the number of occurring valleys is observed. When ZVS pulse is initiated within a time period with lower number of valleys than $N_{RVSvalmax}$ a switch-over to valley synchronized ZV-RVS mode operation is taking place. After leaving the DCM operation the 25% offset is removed again. This ensures a hysteresis between entering and leaving DCM.

3.3.2.5 Overcurrent control

The hybrid-flyback topology supports high level overcurrent operation with high efficiency. In such case CRM operation is taking place based on the equations shown in ***Chapter 3.3.1.3.1***. The additionally required circulating current is achieved by increasing the peak current setting for current set-points higher than I_{SETnom}, as requested by the feedback signal at *FB* pin. Hereby the energy transmission time t_{TRANS} is extended to provide increased negative magnetization level I_{MAGneg} to reach ZVS condition for turning on the *HS* switch (see ***Chapter 3.3.1.2.1***). If the estimated overcurrent is exceeding overcurrent set-points for a defined time period, a protection mode is entered (see ***Chapter 3.4.7***).

3.3.3 Vout start-up control

The IC contains a *Vout* start-up control by observing the output voltage via the reflected voltage at *ZCD* pin, which is shown in ***Figure 34***.

11 configurable, see ***Table 19***

12 configurable, see ***Table 9***

A start-up request takes place after an IC HW reset or entered auto-restart mode when VCC is charged up and exceeded the threshold V_{VCCon} (see ***Chapter 3.2.1***). At that moment following 4 conditions are checked to be valid:

1. Brown-in condition with $V_{VS} > V_{VSBIP}$ (see ***Chapter 3.4.4.1***)
2. No Input overvoltage with $V_{VS} < V_{VSOVP}$ (see ***Chapter 3.4.4.4***)
3. Feedback signal out of regulation range $V_{FB} > V_{FBBMctrl}$
4. No overtemperature condition with $R_{MFIO} > R_{MFIOOTPrel}$ (see ***Chapter 3.4.9***)

The conditions 1-3 needs to be valid within the time period $t_{stupcheck}$. Once conditions 1-3 are valid condition 4 is checked.

In case one of those conditions is not met the IC enters bang-bang during brown-in phase (see ***Chapter 3.2.2***).

After all 4 conditions are valid the IC prepares for the first *HS* switch pulse. Here a maximum on-time $t_{HSonmax}$ is calculated based on *Vin* to check for a R_{Shunt} short circuit at *CS* pin (CSSCP, see ***Chapter 3.4.6***), when turning on the *HS* switch. But before turning on the *HS* switch a first initial *LS* switch pulse is generated with $t_{ZVSst1st}$[13] to precharge the bootstrap capacitor at *HSVCC* pin. Afterwards the length of ZVS pulse is fixed to the time period $t_{ZVSstup}$ until the voltage at *ZCD* pin exceeds the threshold $V_{ZCDtZVSstup}$.

$$t_{ZVSstup} = \frac{I_{MAGneg} \times L_m}{k \times V_{ZCDtZVSstup}}$$

Equation 37

Then t_{ZVS} is decreased depending on increasing V_{ZCD} (see ***Figure 32***).

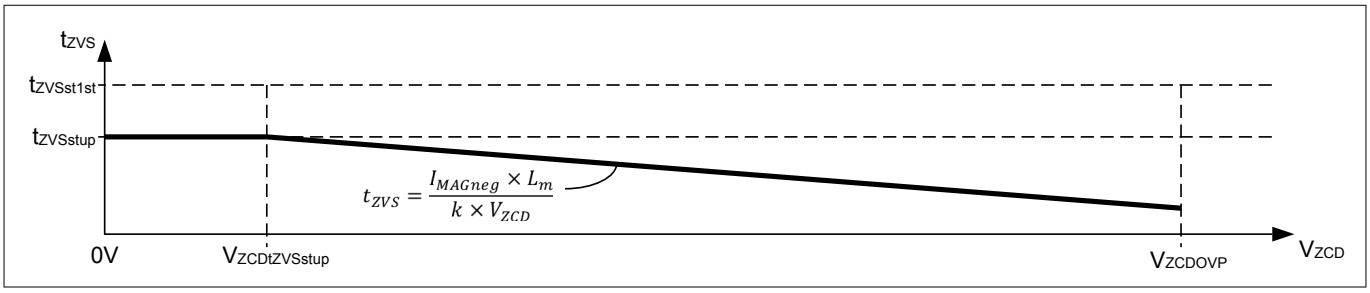


Figure 32 Adaptive t_{ZVS} depending on V_{ZCD}

During ZCD search phase the number of generated half-bridge switching cycles is counted. If no zero-crossing detection is taking place after the *HS* switch is turned off, a next ZVS pulse is generated after a time period $t_{startzcdto}$[13]. When ZCD signal is missing, the counted number of half-bridge switching cycles is exceeding $N_{HBcyclemax}$[13] a protection mode for *Vout* short circuit detection (VoutSCP, see ***Chapter 3.4.8.3***) is entered.

With entering the ZCD search phase the very first peak current setting at *CS* pin is starting based on overcurrent set-point $I_{SETOCP1lev1\%}$. The further peak current setting is kept constant until V_{ZCD} is exceeding the threshold $V_{ZCDtZVSstup}$. Then Vout start-up control is determining the peak current control setting based on comparing the measured voltage at *ZCD* pin with target voltage set-point $V_{ZCDtarget}$. The peak current control is cycle by cycle linearly increasing V_{CS} until target voltage level at *ZCD* pin is reached or linearly decreasing V_{CS} if V_{ZCD} is over the target voltage level for *ZCD* pin. Here the IC increases step by step after a time period $t_{SLWTASK}$ the incremental target value $V_{ZVDtarget}$ (see ***Figure 33***). During start-up the current set-point maximum control range is limited by $I_{SETstmax\%}$[13].

The incremental voltage step $\Delta V_{ZCDstinc}$ is determined by the ramp-up time period $t_{startramp}$[13]:

13 configurable, see ***Table 11***

$$\Delta V_{ZCDstinc} = \frac{V_{ZCDnom} \times t_{SLWTASK}}{t_{startramp}}$$

Equation 38

By this the IC ramps up the output voltage in a primary side controlled manner. When the voltage at *ZCD* pin exceeds the threshold $V_{ZCDRVS2CRM}$ the PWM operation is switched over to CRM scheme.

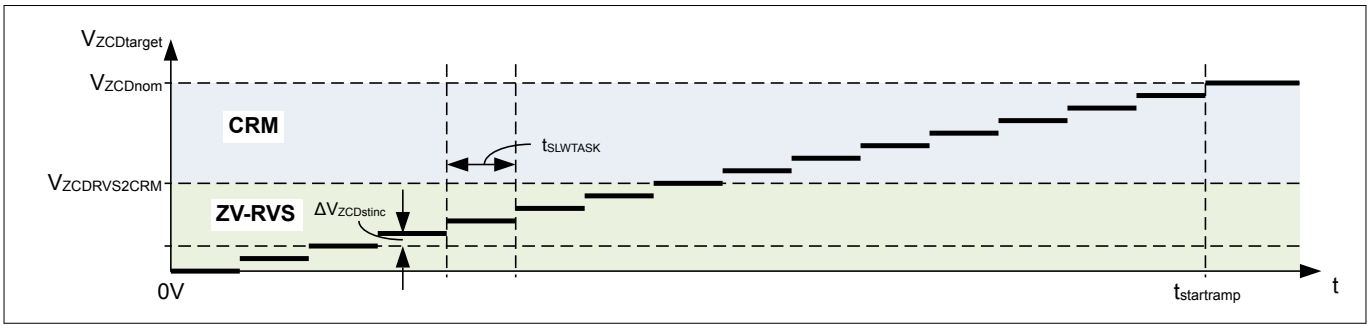


Figure 33 $V_{ZCDtarget}$ control during start-up phase

The start-up phase is finished once the feedback loop at *FB* pin takes over the peak current control. This takes place when the peak current setting at *CS* pin determined by V_{FB} is dropping below the peak current setting determined by V_{ZCD} ramp-up control. The maximum time period for the start-up phase is limited by a timer when exceeding $t_{startto}$, which leads to a start-up timeout (STTOP, see ***Chapter 3.4.5***).

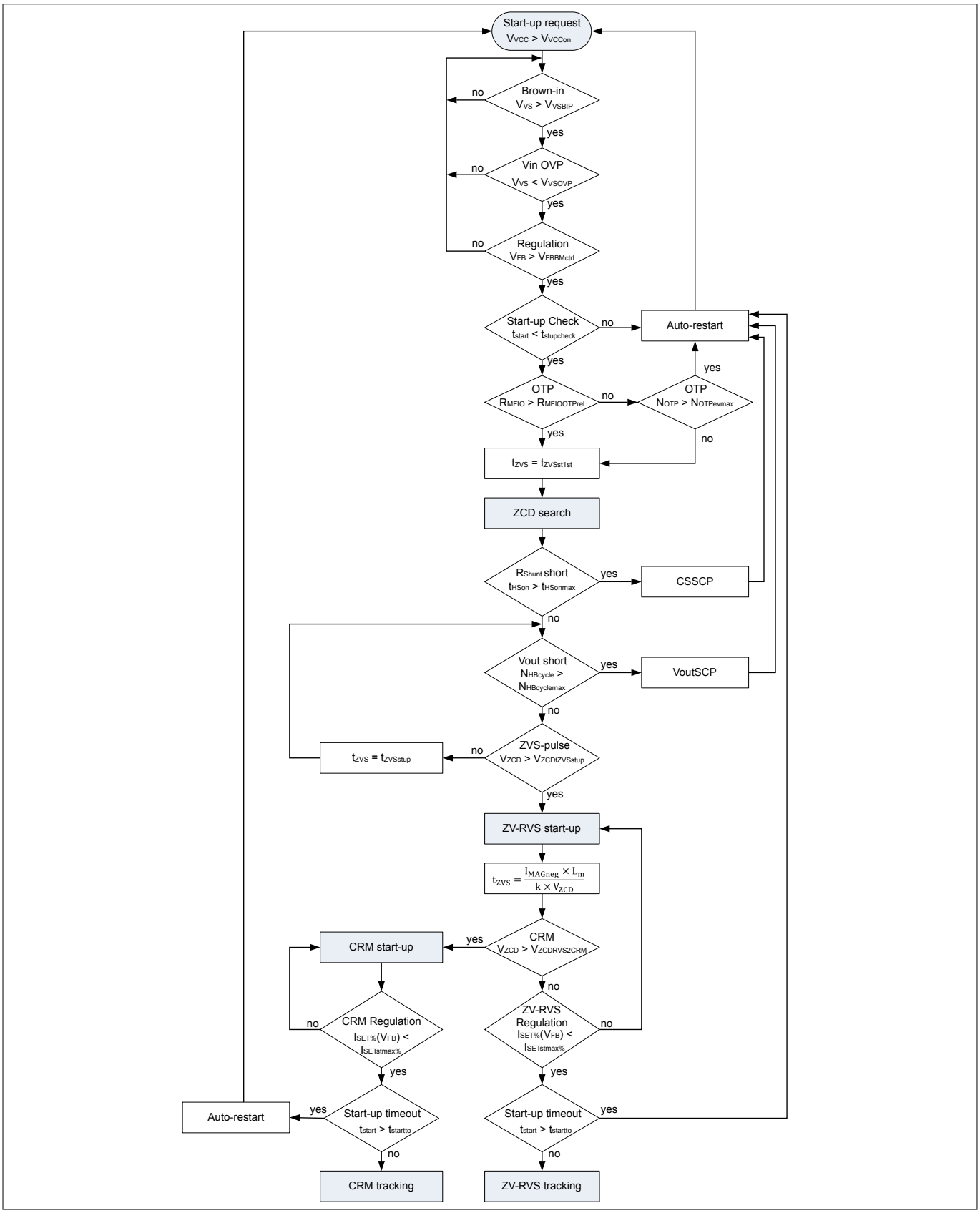


Figure 34 Start-up sequence

3.3.4 Burst mode control

The IC contains a burst mode control block to enter a highly efficient operation mode at light-load. By introducing longer non-switching phases with IC entering a sleep mode the average switching and bias losses are reduced during burst mode operation. A slow and fast burst mode exit is supported in order to have a smooth take-over for feedback voltage regulation, when changing back from hysteretic burst frame on/off control to linear feedback loop control. ***Figure 35*** shows the main functions for the burst mode control as listed and described in the following:

- Burst mode entry (see ***Chapter 3.3.4.1***)
- Burst mode operation (see ***Chapter 3.3.4.2***)
- Burst mode bootstrap precharge (see ***Chapter 3.3.4.3***)
- Burst mode exit control (see ***Chapter 3.3.4.4***)

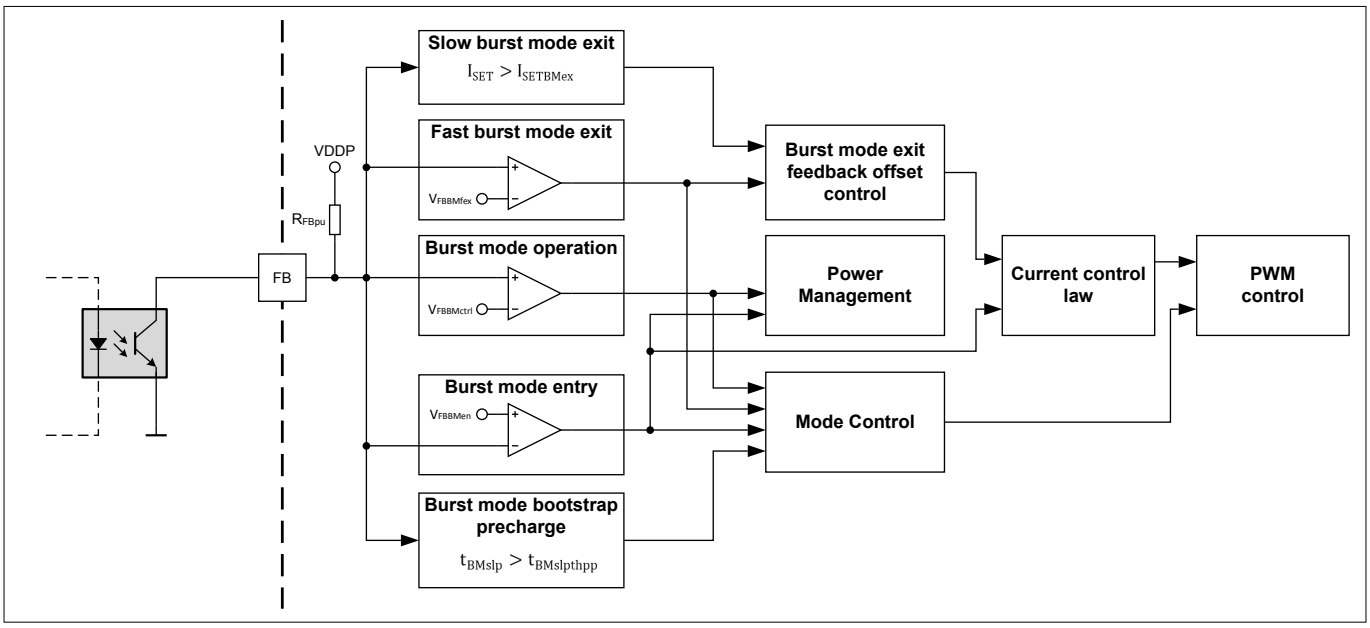


Figure 35 Burst mode control block

3.3.4.1 Burst mode entry

The burst mode entry is based on comparing the voltage at *FB* pin with the threshold V_{FBBMen}. Once V_{FB} is dropping below V_{FBBMen} the generation of next switching pulse is stopped and burst mode is enabled by entering sleep mode with the reduced current consumption $I_{VCCBMpsm}$. V_{FBBMen} is correlated with the current set-point $I_{SETBMen\%}$[14], which is defined by the output current control law (see ***Chapter 3.3.1.3***).

$$V_{FBBMen} = (I_{SETBMen\,\%} \times I_{SETnom\,\%} \times V_{FBOPmax}) + V_{FBOPmin}$$

Equation 39

Once entered burst mode the current control law is switched over to a minimum fixed peak current setting at *CS* pin, which is based on $I_{MAGposRVS(+)} + I_{MAGneg}$ (see ***Figure 30***).

At burst mode entry the HV start-up cell is used once to charge up the VCC and VCC current consumption is reduced during the sleep phases (see ***Chapter 3.2.4***).

14 configurable, see ***Table 10***

3.3.4.2 Burst mode operation

The steady state burst mode operation is based on a burst frame on/off control by means of comparing the voltage at *FB* pin with the feedback burst mode control threshold $V_{FBBMctrl}$. This threshold determines when the IC enters the sleep phase (falling edge) after having generated at least one switching pulse during the active phase. The same comparator is also used during the sleep phase for waking up (rising edge) by triggering a burst on-frame pattern t_{BMfon} (see ***Figure 36***). During sleep phase $V_{FBBMctrl}$ might be slightly lower than during the active phase. Here the burst frame duty cycle and burst mode frequency is fully controlled by means of V_{FB}.

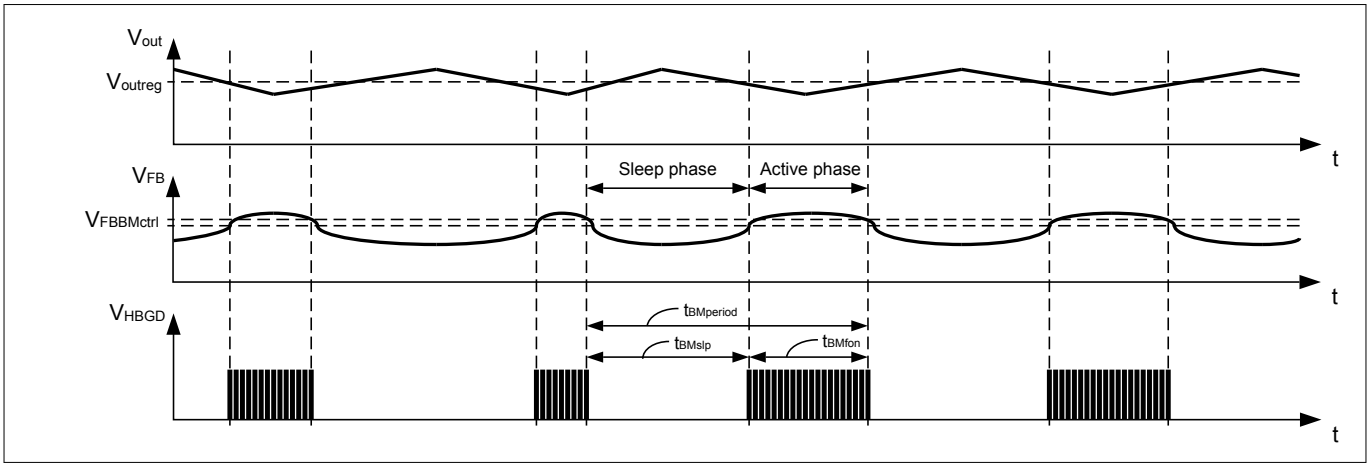


Figure 36 Pulse pattern during burst mode operation

During burst frame on-time t_{BMfon} the transferred energy is based on ZV-RVS mode switching cycles (see ***Chapter 3.3.1.3.2***) with a peak current setting at *CS* pin only dependent on *Vout* and taking the first valley as base for initiating the ZVS pulse.

In burst mode the peak current setting I_{MAGpos} is fixed to $I_{MAGposRVS(+)} + I_{MAGneg}$ (see ***Figure 30***). This results in a limited output current during the burst on-frame phase I_{outBM}:

$$I_{outBM} = \frac{t_{HBperiod}}{t_{HBperiodex}} \times \frac{1}{2} \times N \times \left(I_{MAGposRVS(+)} + I_{MAGneg}\right)$$

Equation 40

The average output current is now depending on the burst on-frame duty cycle (see ***Figure 37***):

$$I_{out} = \frac{t_{BMon}}{t_{BMperiod}} \times I_{outBM}$$

Equation 41

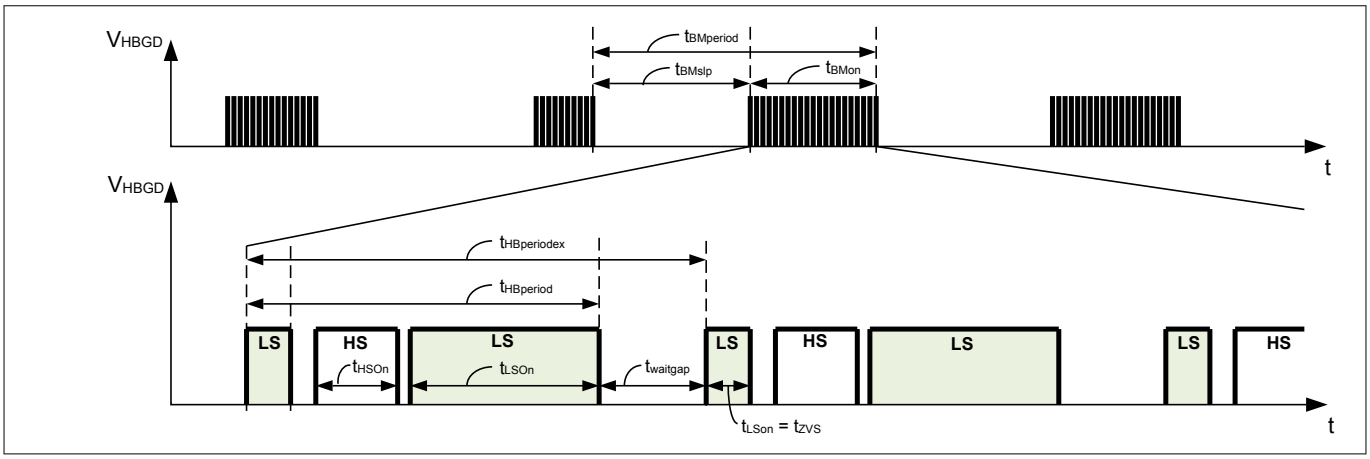


Figure 37 Burst mode timings for average current set-point calculation

3.3.4.3 Burst mode bootstrap precharge

Operation in burst mode at very light-load leads to long IC sleep phases without switching activities. During this sleep-time period t_{BMslp} (see ***Figure 36***) the HSVCC voltage is dropping below the off-threshold $V_{HSVCCoff}$ and deactivating the floating *HS* gate driver (HSUVOFF, see ***Chapter 3.4.3***). When HSVCC is exceeding the on-threshold $V_{HSVCCon}$ the *HS* gate driver is enabled for turning on the power switch after a delay $t_{HSGDdelen}$ (see ***Chapter 3.3.6***). To ensure that a proper HSVCC supply is in place for turning on the *HS* switch after a long IC sleep phase, a precharge pulse is introduced first before the ZV-RVS pattern is executed (see ***Figure 38***). The precharge pulse shall only charge the HSVCC above $V_{HSVCCon}$ in order to get the *HS* gate driver prematurely enabled. Dimensioning the length of this precharge pulse $t_{BMprepulse}$[15)] needs to consider the required delay time period $t_{HSGDendel}$ for getting enabled the HS gate driver after the HSVCC voltage has exceeded the $V_{HSVCCon}$ threshold. During this delay time period also one half-bridge oscillation and one ZVS pulse period are taking place. The precharge pulse is only introduced at the beginning of the burst mode on-frame for a subsequent ZV-RVS switching cycle when the captured burst mode sleep-time period is exceeding the threshold $t_{BMslpthrpp}$[15)].

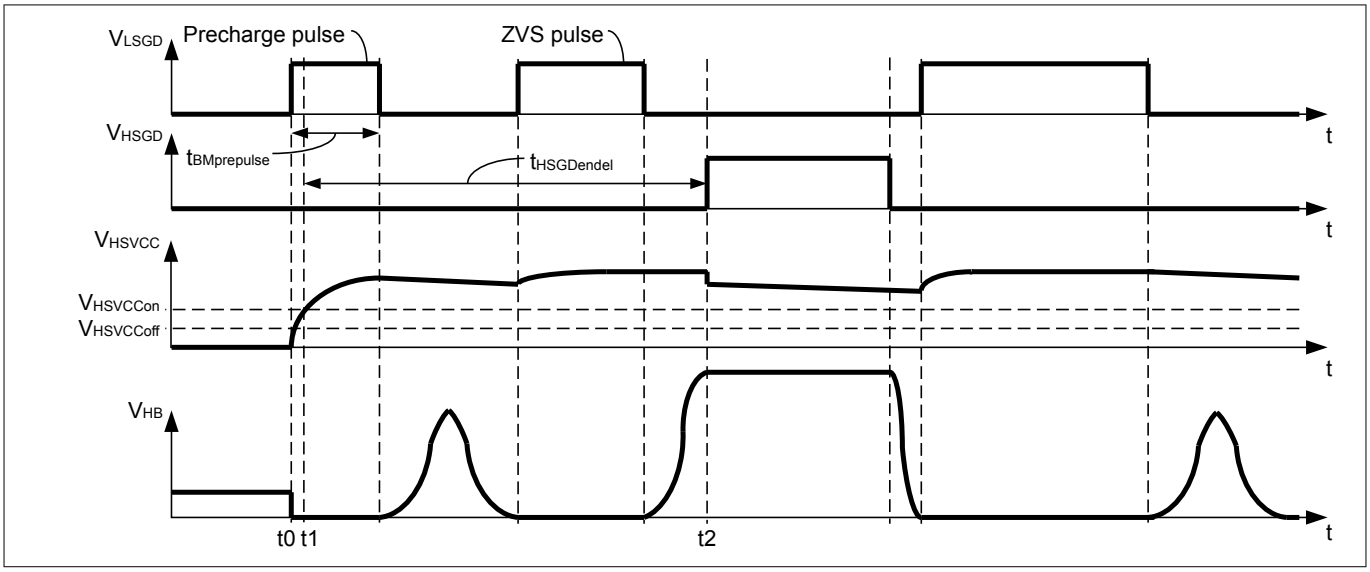


Figure 38 Precharge pulse pattern

15 configurable, see ***Table 10***

3.3.4.4 Burst mode exit control

The burst mode exit control supports a smooth switch-over for the closed feedback control loop when leaving burst mode due to load jump or load is slowly increasing beyond a burst mode exit current set-point threshold. There are two burst mode exit paths supported. A strong load jump requires a fast burst mode exit (see ***Chapter 3.3.4.4.2***) and immediate full power delivery whereas a slightly increasing load shall be controlled for a smooth switch-over (see ***Chapter 3.3.4.4.1***) for the feedback voltage control in order to avoid oscillations at the output. A smaller load jump that leads to a fast burst mode exit shall also not lead to oscillations at the output.
Both requirements are covered by introducing an offset $\Delta V_{FBBM<x>exoffs}$ on the measured feedback voltage V_{FB}, when determining the correlated internal current set-point $I_{SET\%}$ based on the output current control law (see ***Chapter 3.3.1.3***). Once tracking mode is entered (CRM or continuous ZV-RVS mode operation) $\Delta V_{FBBM<x>exoffs}$ is linearly reduced by every half-bridge switching cycle (see ***Figure 39***).

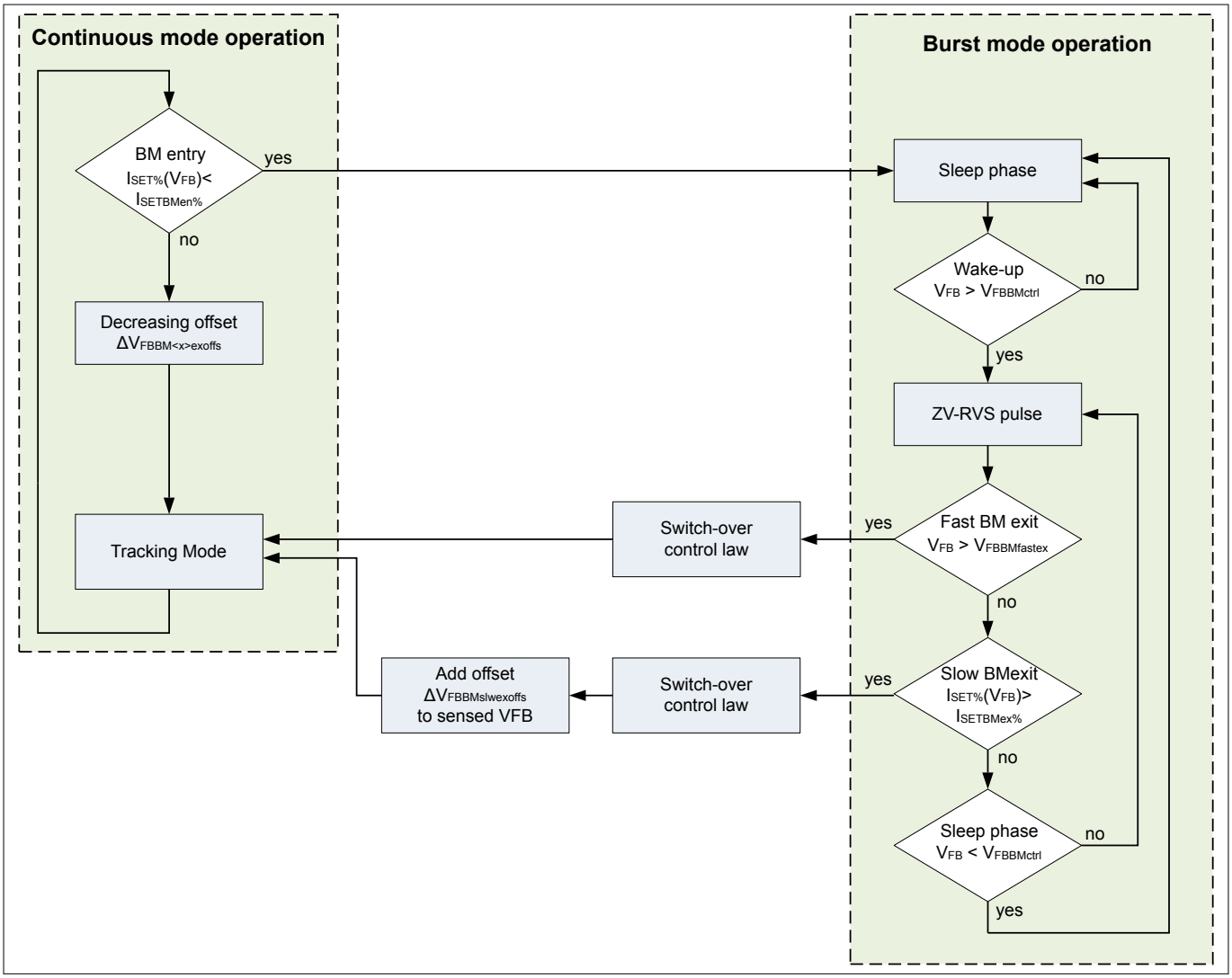


Figure 39 Burst mode exit flow diagram

During burst mode operation the feedback control law only contains two thresholds at *FB* pin and one for the internal current set-point $I_{SET\%}$ (see ***Figure 40***):

- $V_{FBBMctrl}$ for controlling the burst on-frame and the sleeping phase
- $V_{FBBMfastex}$ for immediately leaving the burst mode
- $I_{SETBMex\%}$ based on output current estimation for slowly leaving the burst mode

When a burst mode exit condition is met a switch-over of the output current control law is taking place. The feedback voltage level corresponds at that point of time to a different current set-point compared to steady state continuous operation. E.g. if a slow burst mode exit takes place with $I_{SET\%}(V_{FB}) > I_{SETBMex\%}$, the feedback

voltage is ca. $V_{FBBMctrl}$, which is then close to the nominal current set-point $I_{SETnom\%}$. The normally required $I_{SETBMex\%}$ and associated V_{FBBMex} levels are much lower, which then can lead to an output voltage overshoot depending on how fast the external control loop is adjusting V_{FB} to the required lower level. The added offset on the measured V_{FB} is immediately ensuring the right internal current set-point for peak current control at *CS* pin. By afterwards linearly reducing every half-bridge switching cycle the offset the regulator is supported to smoothly settle to the target feedback point, which matches then to the required internal current set-point defined by the control law. The target feedback point after burst mode slow exit can be calculated by ***Equation 13***:

$$V_{FBBMex} = (I_{SETBMex\%} \times I_{SETnom\%} \times V_{FBOPmax}) + V_{FBOPmin}$$

Equation 42

The added offset after burst mode slow exit is therefore:

$$\Delta V_{FBBMslwexoffs} = V_{FBBMex} - V_{FBBMctrl}$$

Equation 43

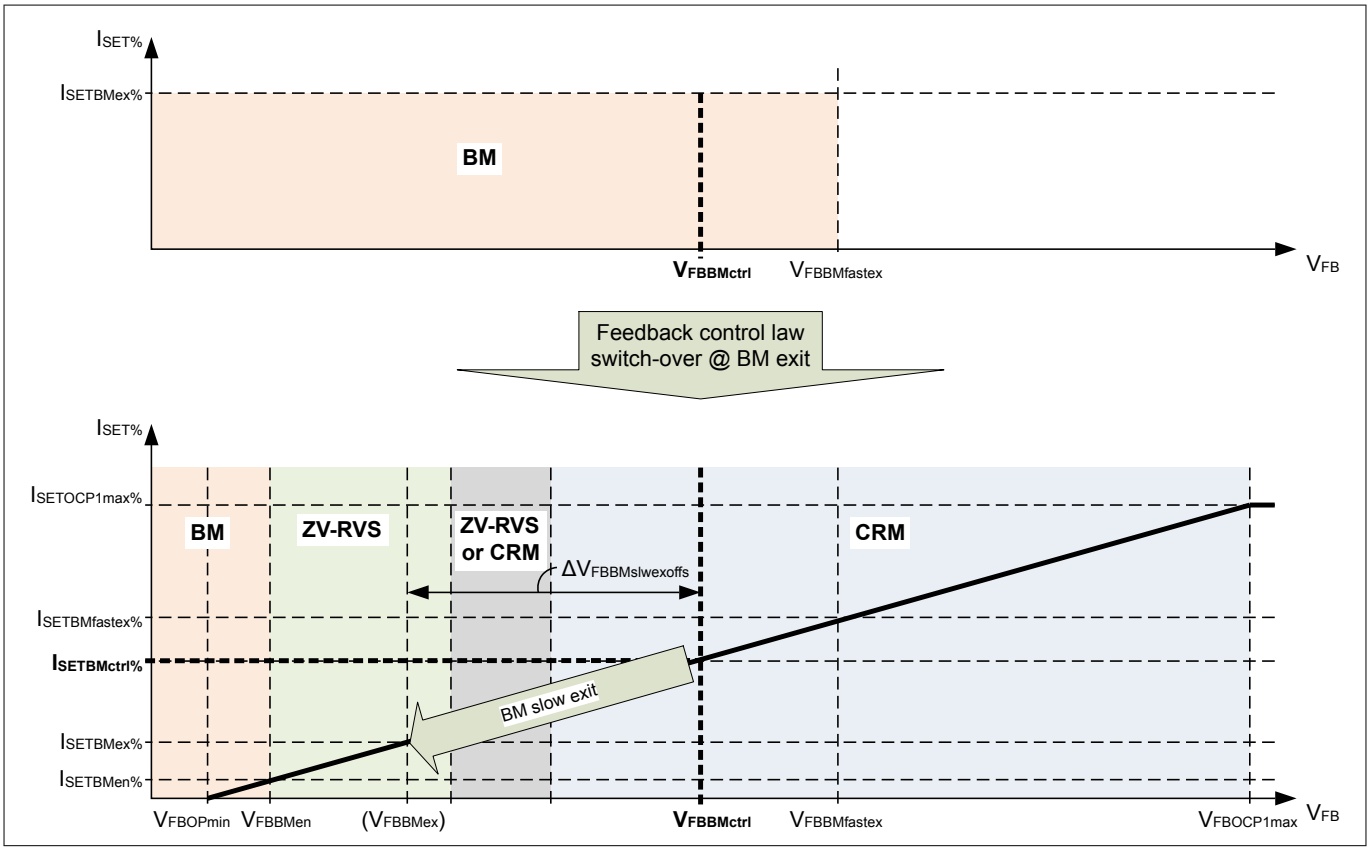


Figure 40 Control law switch-switch over from burst mode to continuous mode operation

3.3.4.4.1 Burst mode slow exit

Burst mode slow exit is based on output current estimation by capturing the burst frame duty cycle during burst mode operation (see ***Equation 41***). When the estimated current is exceeding the current set-point $I_{SETBMex\%}$ [16)] for number of $N_{BMexreqthr}$ [16)] burst frame period cycles the burst mode is left by switching over the control law to continuous operation, activating the offset $\Delta V_{FBBMslwexoffs}$ and entering tracking mode with ZV-RVS mode operation.

16 configurable, see ***Table 10***

3.3.4.4.2 Burst mode fast exit

Once a load jumps exceeds the fixed energy transmission level set during burst on-frame period the feedback voltage is further increasing. The fast burst mode exit threshold $V_{FBBMfastex}$[17] is then exceeded if not slow burst mode has been triggered so far. Afterwards the control law is switched over. The IC is then entering CRM operation for the first half-bridge switching cycles if V_{ZCD} is higher than the threshold $V_{ZCDRVS2CRM}$. This can be disabled by $EN_{BMfastexCRM}$[18].

3.3.5 Frequency jitter

The jitter function is only working in CRM operation. Furthermore it is depending on the voltage at *VS* pin. The jitter function is enabled once the voltage at *VS* pin exceeds the threshold $V_{VSJitteren}$[19]. Frequency jitter is generated by modulating the magnetizing current for I_{MAGpos} and I_{MAGneg} in such a way that the sum of them I_{MAGtot} is kept constant. Then also I_{out} is kept constant not being impacted by modulating the switching period (see ***Equation 5***).

$$I_{MAGtot} = I_{MAGpos} + I_{MAGneg}$$

Equation 44

The modulation of the peak to peak magnetizing current I_{MAGpp} is performed by directly adjusting the peak current threshold at *CS* pin for the positive magnetizing current level I_{MAGpos} and indirectly adjusting the negative magnetizing current level I_{MAGneg} by means of changing the on-time t_{LSon} (see ***Chapter 3.1.1***).

$$I_{MAGpp} = I_{MAGpos} - I_{MAGneg}$$

Equation 45

Once the negative magnetizing current is changing, the closed control loop is adjusting I_{MAGpos} accordingly.

The delta for the change of half-bridge switching frequency ΔF_{HBsw} is set by a constant for the target jitter spread $d_{Jitterspread\%}$[19], which is based on a percentage number of the switching frequency without Jitter.

$$\Delta F_{HBsw} = F_{HBsw} \times d_{Jitterspread\,\%}$$

Equation 46

$$\Delta t_{HBsw} = \frac{1}{\Delta F_{HBsw}}$$

Equation 47

The incremental step for changing the target switching period is one master clock period t_{MCLK}. This adjustment is taking place after a delay time $t_{Jitterstpdel}$[19] in order to provide time for the control loop to settle to the changed level for I_{MAGneg}. The jitter function starts first with increasing I_{MAGneg} step by step until the correlated switching period has exceeded the target maximum jitter switching period $t_{Jitterpermax}$.

$$t_{Jitterpermax} = t_{HBper} + \Delta t_{HBsw}$$

Equation 48

17 configurable, see ***Table 10***
18 configurable, see ***Table 10***
19 configurable, see ***Table 20***

Subsequently I_{MAGneg} is adjusted step by step back to the starting level for the switching period t_{HBper} (see ***Figure 41***)

Note: Increasing the amount of negative magnetization I_{MAGneg} is reducing the dead-time for turning on the high-side switch t_{deadHS}. Therefore the potential target delta for switching period spread $d_{Jitterspread\%}$ is limited by the target minimum time delay between the falling edge of LS switch and following zero-crossing detection $t_{LSdelZCDmin}$.

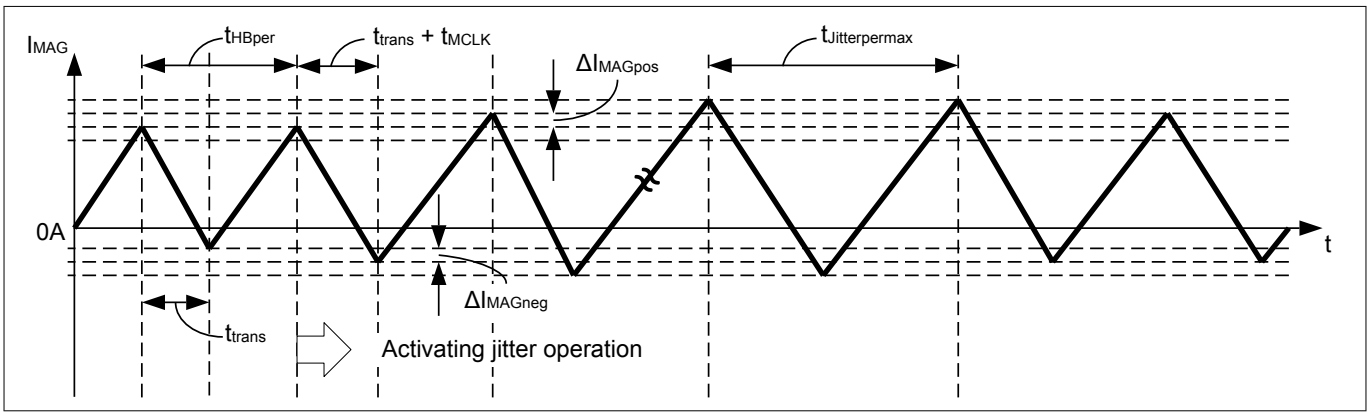


Figure 41 I_{MAG} modulation for frequency jittering

3.3.6 Half-bridge gate driver

The half-bridge gate driver consists of a low-side gate driver for *LS* switch, which is supplied by *VCC* and *GND* pin. The *HS* switch is driven by a floating high-side gate driver supplied by *HSVCC* and *HSGND*. The floating HS domain is galvanically isolated and steered via a coreless pulse transformer. The *LS* and *HS* gate drivers are enabled/disabled based on the corresponding undervoltage lockout thresholds (V_{VCCon}, V_{VCCoff}) and ($V_{HSVCCon}$, $V_{HSVCCoff}$) (see ***Chapter 3.4.2*** and ***Chapter 3.4.3***). Both drivers are clamping the maximum gate driver output voltage to $V_{LSGDhigh}$; $V_{HSGDhigh}$. If disabled the gate driver outputs are actively kept shut down. When HSVCC exceeds the threshold $V_{HSVCCon}$ the high-side gate driver is enabled after a time period of $t_{HSGDendel}$.

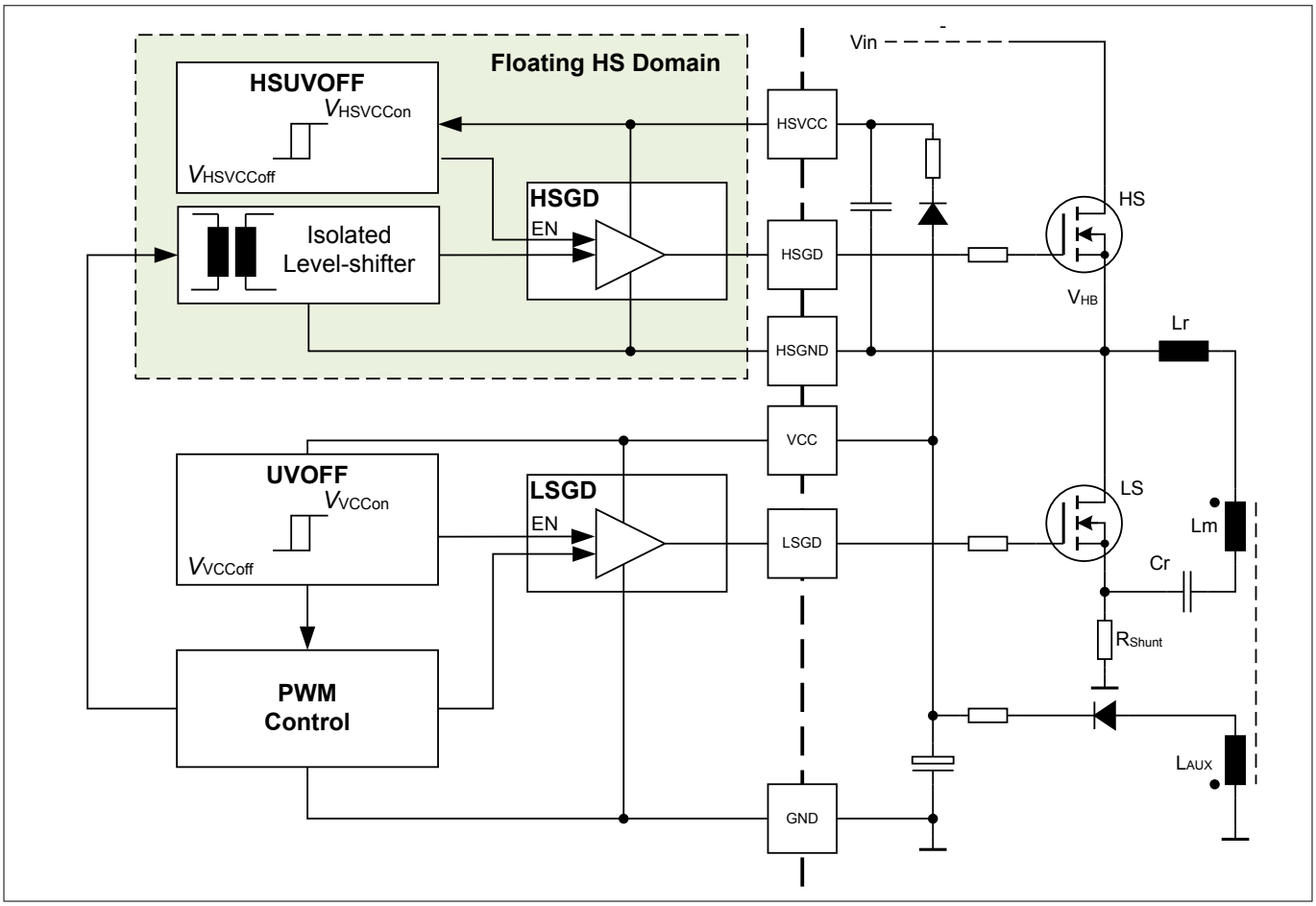


Figure 42 Half-bridge gate driver

3.4 Protection features

Table 4 shows the protection features and their corresponding default reactions. Two protection modes (auto-restart mode and latch mode) as well as a UVOFF HW reset (IC deactivation by VCC undervoltage lockout) are implemented.

Note: All protection features w/o UVOFF and HSUVOFF only apply during normal operation. During sleep phase (in burst or protection mode), no pin protection is active.

Table 4 Protection features

Feature	Symbol	Default reaction	Description
VCC undervoltage lockout	UVOFF	HW reset and restart	*Chapter 3.4.2*
HSVCC undervoltage lockout	HSUVOFF	Disable HS gate driver	*Chapter 3.4.3*
Brown-in protection	BIP	Bang-bang mode without start-up request	*Chapter 3.4.4.1*
Slow brown-out protection	SBOP	Stop operation and enter bang-bang mode for brown-in phase	*Chapter 3.4.4.3*
Fast brown-out protection	FBOP	Stop operation and enter bang-bang mode for brown-in phase	*Chapter 3.4.4.2*
Vin overvoltage protection	VinOVP	Auto-restart mode	*Chapter 3.4.4.4*
Start-up timeout protection	STTOP	Auto-restart mode	*Chapter 3.4.5*
CS pin short circuit protection	CSSCP	Auto-restart mode	*Chapter 3.4.6*
Output overcurrent protection OCP1 level 1	OCP1lev1	Auto-restart mode	*Chapter 3.4.7.1*
Output overcurrent protection OCP1 level 2	OCP1lev2	Auto-restart mode	*Chapter 3.4.7.2*
Output maximum current protection	OCP1max	Auto-restart mode	*Chapter 3.4.7.3*
Peak overcurrent protection OCP2	OCP2	Latch mode[20]	*Chapter 3.4.7.4*
Vout overvoltage protection	VoutOVP	Latch mode[21]	*Chapter 3.4.8.2*
Vout undervoltage protection	VoutUVP	Auto-restart mode	*Chapter 3.4.8.1*
Vout short circuit protection	VoutSCP	Auto-restart mode[22]	*Chapter 3.4.8.3*
External overtemperature protection	extOTP	Auto-restart mode & Latch mode	*Chapter 3.4.9*
Watchdog timer	WDOG	Auto-restart	*Chapter 3.4.10*

20 configurable with EV_{CSOCP2}, see *Table 16*
21 configurable with EV_{ZCDOVP}, see *Table 15*
22 Only active during start-up phase

3.4.1 Protection modes

Once the protection mode is entered, the IC stops the gate driver switching at *LSGD* and *HSGD* pins and enters stand-by mode. During stand-by mode, the HV start-up cell is operating in the bang-bang mode (see ***Chapter 3.2.3***) to keep the VCC voltage at a high level to have enough energy stored in the VCC capacitor for the system start-up. Two protections modes are supported as described in the sequel.

Latch mode (LM)

In latched operation the system keeps staying in stand-by mode without any restart attempt. The latched operation can only be reset by VCC dropping below the UVOFF HW reset threshold V_{VCCoff}.

Note: Reset of latch mode is done by disconnecting the AC line. By connecting the HV start-up cell via diodes in front of the rectifier the reset time is mainly determined by the size of the capacitor at VCC pin.

Auto-restart mode (ARM)

In auto-restart mode operation the IC triggers a restart after the approximated auto-restart sleep time t_{ARMslp}[23)]. The control IC resumes its operation with soft-start after the VCC capacitor is charged up and the VCC voltage has reached its turn-on threshold V_{VCCon}. t_{ARMslp} determines the number of set sleep cycles $N_{ARMstep}$, which are based on the time period $t_{ARMbase}$. (see ***Chapter 3.2.3***).

$$t_{ARMslp} = N_{ARMstep} \times t_{ARMbase}$$

Equation 49

3.4.2 VCC undervoltage lockout (UVOFF)

The implemented VCC undervoltage lockout (UVOFF) ensures a defined activation and deactivation of the IC operation depending on the supply voltage at pin VCC. The UVOFF contains a hysteresis with the upper voltage threshold V_{VCCon} for activating the IC. A VCC voltage level dropping below the bottom threshold V_{VCCoff} resets and deactivates the IC during normal operation. In reset state the HV start-up cell is turned on, starting the next VCC charge cycle until VCC voltage exceeds V_{VCCon} (see ***Chapter 3.2.1***).

3.4.3 HSVCC undervoltage lockout (HSUVOFF)

The implemented HSVCC undervoltage lockout (UVOFF) ensures a defined activation and deactivation of the floating high-side driver. The HSUVOFF contains a hysteresis with the upper voltage threshold $V_{HSVCCon}$ for activating the high-side gate driver. A HSVCC voltage level dropping below the bottom threshold $V_{HSVCCoff}$ turns off and deactivates immediately the high-side driver. During deactivation phase the high-side driver current consumption is reduced to $I_{HSVCCUVOFF}$.

3.4.4 Input voltage Vin protection

The IC contains 4 detection thresholds at *VS* pin for input voltage *Vin* protection to ensure a safe operation within a reliable input voltage range (see ***Figure 43***). Following *Vin* protections are provided:

- Vin brown-in protection (BIP, see ***Chapter 3.4.4.1***)
- Vin slow brown-out protection (SBOP, see ***Chapter 3.4.4.3***)
- Vin fast brown-out protection (FBOP, see ***Chapter 3.4.4.2***)
- Vin overvoltage protection (VinOVP see ***Chapter 3.4.4.4***)

23 configurable, see ***Table 12***

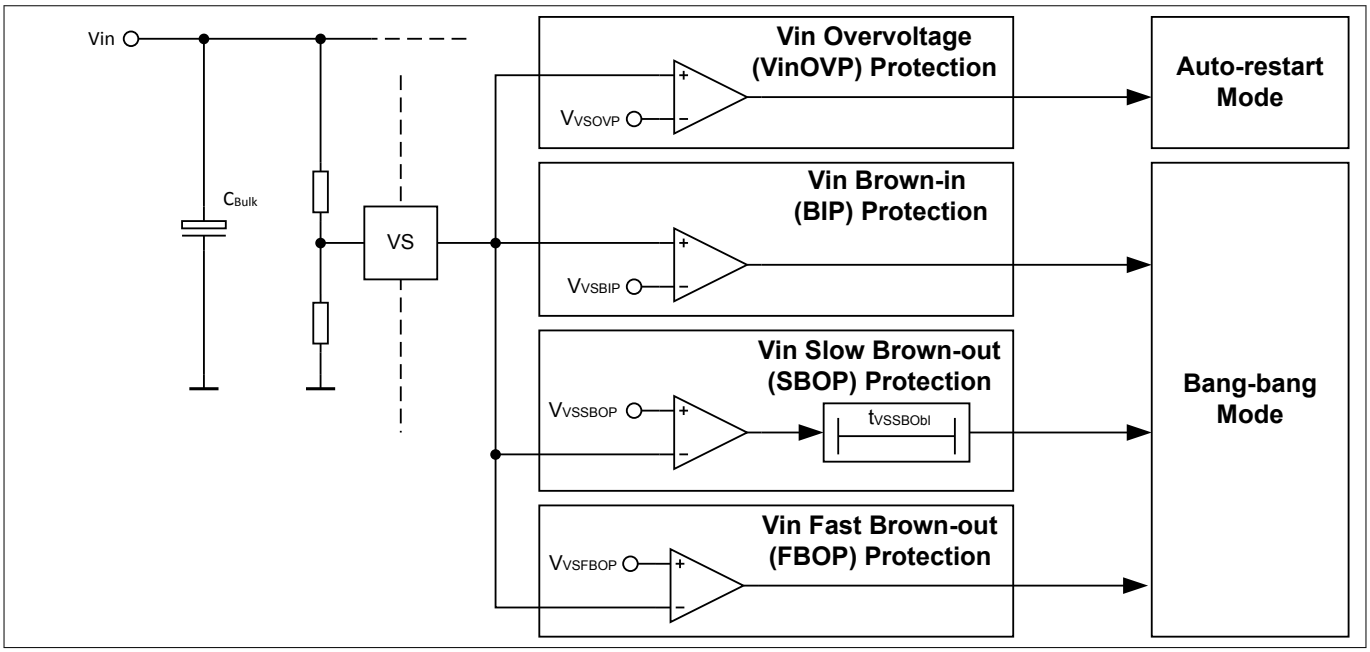


Figure 43 Input voltage *Vin* protection

3.4.4.1 Brown-in protection (BIP)

At initial power-up or auto-restart, the brown-in condition at *VS* pin must be fulfilled for initiating the switching start-up procedure. Brown-in conditions are met when voltage at *VS* pin exceeds the threshold V_{VSBIP}[24] within the time period $t_{stupcheck}$ during start-up (see ***Chapter 3.3.3***). If the IC is activated and *Vin* brown-in condition are not reached the IC enters the bang-bang mode to keep the IC alive and ensure a high VCC level for immediate start-up once *Vin* brown-in conditions are detected (see ***Chapter 3.2.2***).

3.4.4.2 Fast brown-out protection (FBOP)

The fast brown-out protection (FBOP) is realized by comparing the voltage at *VS* pin with the threshold V_{VSFBOP}[24] that is set below the slow brown-out protection threshold V_{VSSBOP} (see ***Chapter 3.4.4.3***). Fast brown-out occurrence is not blanked and sampled with a time period t_{sample}.

3.4.4.3 Slow brown-out protection (SBOP)

The slow brown-out protection (SBOP) is realized by comparing the voltage at *VS* pin with the threshold V_{VSSBOP}[24] for a blanking time $t_{VSSBOPbl}$. Once triggered the bang-bang mode for *Vin* brown-in detection is entered (see ***Chapter 3.2.2***).

3.4.4.4 Vin overvoltage protection (VinOVP)

Vin overvoltage protection (VinOVP) is taking place by comparing the voltage at *VS* pin with the threshold V_{VSOVP}[25]. The result is sampled with a time period t_{sample}. Once VinOVP is triggered the auto-restart mode is entered (see ***Chapter 3.4.1***).

At *Vout* start-up the VinOVP is checked together with brown-in protection (BIP) (see ***Chapter 3.3.3***). When a time period $t_{stupcheck}$ is exceeded and *Vin* voltage level is not within the target range the bang-bang mode during

24 configurable, see ***Table 11***
25 configurable, see ***Table 13***

brown-in phase is entered (see ***Chapter 3.3.3***). Furthermore also at wake-up during burst mode operation the start of burst on-frame is only initiated if no VinOVP is detected at wake-up.

3.4.5 Start-up timeout protection (STTOP)

In case of overload during start-up the output voltage *Vout* may not reach the regulation nominal voltage target *Voutnom*, preventing the system from entering regulation and staying permanently in start-up condition. To avoid such situation a timer is initiated at start-up request from the very first switching pulse to observe the ongoing start-up time t_{start}. A timeout is detected when after a maximum time period $t_{startto}$[26)] the current set-point determined by V_{FB} is not dropping below the current set-point determined by *Vout* start-up control (see ***Chapter 3.3.3***).

3.4.6 CS pin short circuit protection (CSSCP)

During *Vout* start-up a short circuit detection at *CS* pin is activated for the very first *HS* switch pulse to protect the application operating with a shortened R_{Shunt}. Hereby the maximum on-time of *HS* switch is limited to a precalculated time period $t_{HSonmax}$:

$$t_{HSonmax} = 2 \times t_{TRANSnom} \times \left(\frac{(V_{outnom} \times N)/k_{Rvs}}{V_{VS}} \right)$$

Equation 50

V_{VS} is the instantaneous input voltage measured at *VS* pin. Once the on-time of *HS* switch exceeds $t_{HSonmax}$ auto-restart mode is entered.

3.4.7 Overcurrent protection

The overcurrent protection contains several detection functions, which protect the application when exceeding a primary side peak current or operating under output overcurrent conditions (see ***Figure 44***).

- Output overcurrent protection OCP1 level 1 (OCP1lev1, see ***Chapter 3.4.7.1***)
- Output overcurrent protection OCP1 level 2 (OCP1lev2, see ***Chapter 3.4.7.2***)
- Output maximum current protection (OCP1max, see ***Chapter 3.4.7.3***)
- Primary peak overcurrent protection OCP2 (OCP2, see ***Chapter 3.4.7.4***)

26 configurable, see ***Table 14***

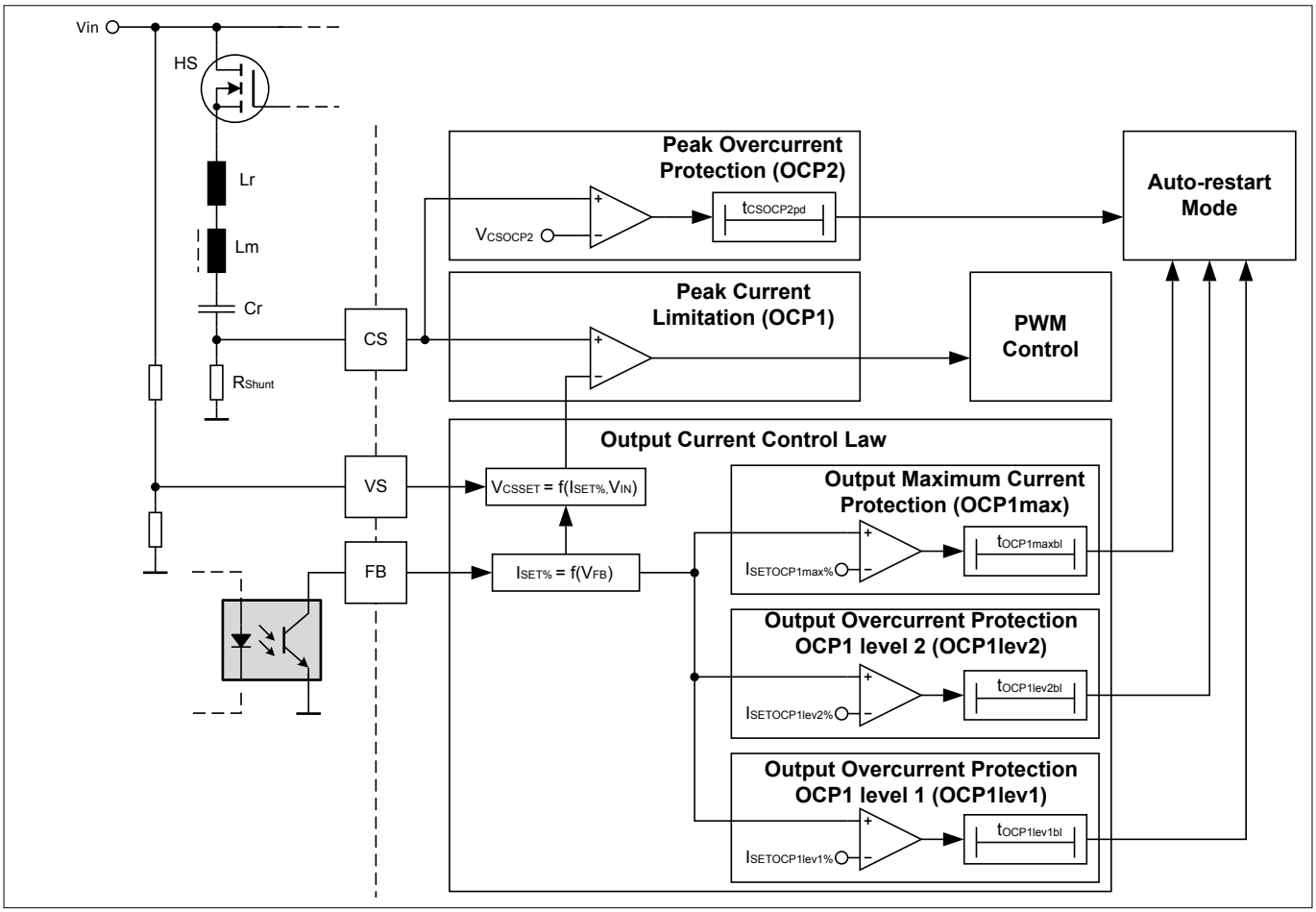


Figure 44 Overcurrent protection overview

3.4.7.1 Output overcurrent protection OCP1 level 1 (OCP1lev1)

The output overcurrent protection level $I_{SETOCP1lev1\%}$[27] is defined by the output current control law (see ***Figure 25***). Once the current set-point $I_{SET\%}$ exceeds the threshold $I_{SETOCP1lev1\%}$ a timer is started. Auto-restart mode is triggered when the timer reaches the threshold $t_{OCP1lev1bl\%}$[27]. The timer is also reset when $I_{SET\%}$ is dropping back below $I_{SETOCP1lev1\%}$.

The associated peak current setting at *CS* pin can be calculated with ***Equation 15*** and ***Equation 16***:

CRM operation

$$V_{CSOCP1lev1} = (I_{SETOCP1lev1\,\%} \times I_{SETnom\,\%} \times V_{CSOPmax}) + (I_{MAGneg}(Vin) \times R_{Shunt})$$

Equation 51

ZV-RVS operation

$$V_{CSOCP1lev1} = \frac{t_{HBperiodex}}{t_{HBperiod}} \times [(I_{SETOCP1lev1\,\%} \times I_{SETnom\,\%} \times V_{CSOPmax}) + (I_{MAGneg}(Vin) \times R_{Shunt})]$$

Equation 52

The associated feedback voltage at *FB* pin can be calculated with ***Equation 13***:

27 configurable, see ***Table 16***

$$V_{\mathrm{FBOCP1lev1}} = (I_{\mathrm{SETOCP1lev1\,\%}} \times I_{\mathrm{SETnom\,\%}} \times V_{\mathrm{FBOPmax}}) + V_{\mathrm{FBOPmin}}$$

Equation 53

3.4.7.2 Output overcurrent protection OCP1 level 2 (OCP1lev2)

The threshold $I_{\mathrm{SETOCP1lev2\%}}$[28] provides a 2nd output overcurrent protection level. Once the current set-point $I_{\mathrm{SET\%}}$ exceeds the threshold $I_{\mathrm{SETOCP1lev2\%}}$ the timer for OCP1lev2 is started. Auto-restart mode is triggered when the timer reaches the threshold $t_{\mathrm{OCP1lev2bl\%}}$[28]. This timer is also reset when I_{SET} is dropping back below $I_{\mathrm{SETOCP1lev2\%}}$

The associated peak current setting at *CS* pin can be calculated with ***Equation 15*** and ***Equation 16***:

CRM operation

$$V_{\mathrm{CSOCP1lev2}} = (I_{\mathrm{SETOCP1lev2\,\%}} \times I_{\mathrm{SETnom\,\%}} \times V_{\mathrm{CSOPmax}}) + \left(I_{\mathrm{MAGneg}}(\mathrm{Vin}) \times R_{\mathrm{Shunt}}\right)$$

Equation 54

ZV-RVS operation

$$V_{\mathrm{CSOCP1lev2}} = \frac{t_{\mathrm{HBperiodex}}}{t_{\mathrm{HBperiod}}} \times \left[(I_{\mathrm{SETOCP1lev2\,\%}} \times I_{\mathrm{SETnom\,\%}} \times V_{\mathrm{CSOPmax}}) + \left(I_{\mathrm{MAGneg}}(\mathrm{Vin}) \times R_{\mathrm{Shunt}}\right)\right]$$

Equation 55

The associated feedback voltage at *FB* pin can be calculated with ***Equation 13***:

$$V_{\mathrm{FBOCP1lev2}} = (I_{\mathrm{SETOCP1lev2\,\%}} \times I_{\mathrm{SETnom\,\%}} \times V_{\mathrm{FBOPmax}}) + V_{\mathrm{FBOPmin}}$$

Equation 56

3.4.7.3 Output maximum current protection (OCP1max)

The threshold $I_{\mathrm{SETOCP1max}}$[29] defines the maximum output current level of output current control. Once a higher output current is requested via V_{FB} control the output current is kept limited and a timer for IoutMaxP is started. During this phase output voltage is dropping because output current is higher than what is provided by the converter ($I_{\mathrm{SETOCP1max}}$). Auto-restart mode is entered when the timer reaches the threshold $t_{\mathrm{OCP1maxbl}}$[29]. The timer is reset when auto-restart mode is entered or I_{SET} is dropping below $t_{\mathrm{OCP1maxbl}}$.

The associated peak current setting at *CS* pin can be calculated with ***Equation 15*** and ***Equation 16***:

CRM operation

$$V_{\mathrm{CSOCP1max}} = I_{\mathrm{SETOCP1max\,\%}} \times I_{\mathrm{SETnom\,\%}} \times V_{\mathrm{CSOPmax}} + \left(I_{\mathrm{MAGneg}}(\mathrm{Vin}) \times R_{\mathrm{Shunt}}\right)$$

Equation 57

ZV-RVS operation

28 configurable, see ***Table 16***

29 configurable, see ***Table 16***

$$V_{\mathrm{CSOCP1max}} = \frac{t_{\mathrm{HBperiodex}}}{t_{\mathrm{HBperiod}}} \times \left[I_{\mathrm{SETOCP1max\,\%}} \times I_{\mathrm{SETnom\,\%}} \times V_{\mathrm{CSOPmax}} + \left(I_{\mathrm{MAGneg}}(\mathrm{Vin}) \times R_{\mathrm{Shunt}} \right) \right]$$

Equation 58

The associated feedback voltage at *FB* pin can be calculated with ***Equation 13***:

$$V_{\mathrm{FBOCP1max}} = I_{\mathrm{SETOCP1max\,\%}} \times I_{\mathrm{SETnom\,\%}} \times V_{\mathrm{FBOPmax}} + V_{\mathrm{FBOPmin}}$$

Equation 59

3.4.7.4 Primary peak overcurrent protection OCP2 (OCP2)

V_{CSOCP2} is a fixed threshold at *CS* pin and beyond the maximum operating range V_{CSOPmax}. The OCP2 function is not blanked during the leading edge blanking time t_{HSleb}. Once exceeded the latch mode is entered as default.

3.4.8 Vout voltage protection

The IC provides 2 output voltage *Vout* protection threshold levels V_{ZCDUVP} (VoutUVP, see ***Chapter 3.4.8.1***) and V_{ZCDOVP} (VoutOVP, see ***Chapter 3.4.8.2***) to ensure a reliable operation within a defined *Vout* operating range. The measurement is done via the reflected voltage at the auxiliary winding of the transformer during the demagnetization phase when the LS switch is turned on (see ***Figure 19***). Furthermore the zero-crossing detection during start-up phase is observed to detect short circuit conditions at the output (VoutSCP, see ***Chapter 3.4.8.3***).

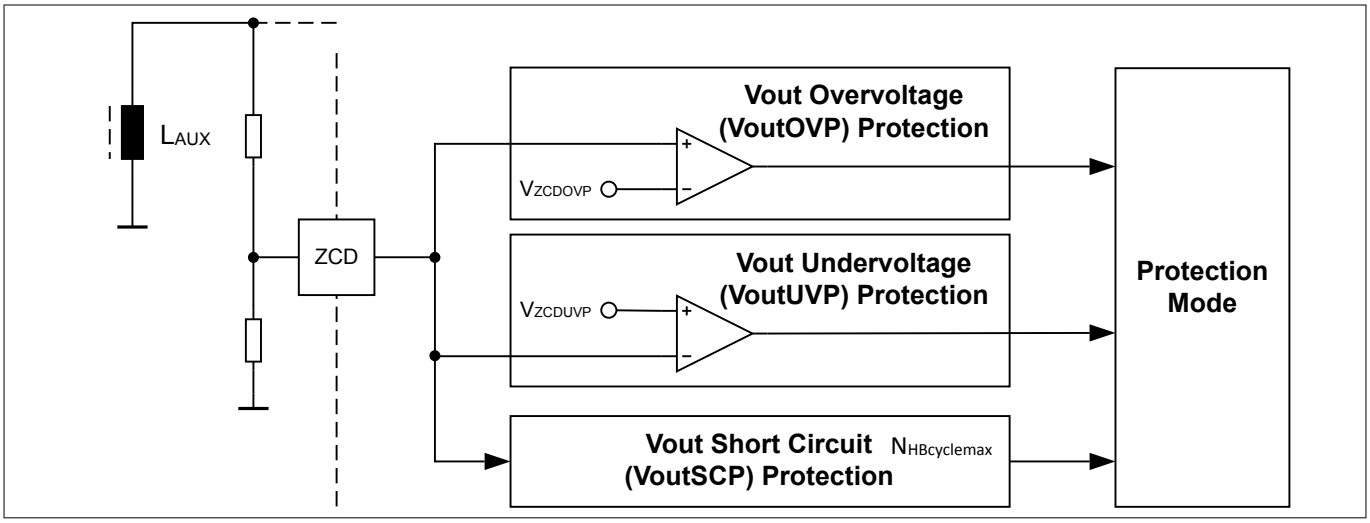


Figure 45

3.4.8.1 Vout undervoltage protection (VoutUVP)

Vout undervoltage is detected when the reflected output voltage measured via *ZCD* pin is dropping below the threshold V_{ZCDUVP}[30)]. Once detected the auto-restart mode is immediately triggered. *VoutUVP* can be disabled during burst mode operation by means of $EN_{\mathrm{BMVoutUVP}}$[30)].

30 configurable, see ***Table 15***

3.4.8.2 Vout overvoltage protection (VoutOVP)

Vout overvoltage is detected when the reflected output voltage measured via *ZCD* pin is exceeding the threshold V_{ZCDOVP}[31]. Once detected a protection mode is immediately triggered. The default reaction is set to latch mode and can be changed to auto-restart mode with EV_{ZCDOVP}[31].

3.4.8.3 Vout short circuit protection (VoutSCP)

The *Vout* short circuit protection is only active during start-up phase in order to limit the number of half-bridge switching cycles during the auto-restart. When operating under short circuit condition at the output the magnitude of reflected voltage is too low, which inhibits a proper zero-crossing detection at *ZCD* pin. After start-up request only a maximum of $N_{HBcyclemax}$[32] consecutive half-bridge switching cycles without zero-crossing detection are allowed. If $N_{HBcyclemax}$ is exceeded the restart phase is stopped and auto-restart mode sleeping phase is prematurely entered.

3.4.9 External overtemperature protection (extOTP)

The external overtemperature protection is based on measuring an external NTC resistor. The external NTC is biased by the internal *VREF* supply via the internal pull-up resistor R_{MFIOpu}. The voltage at *MFIO* pin is measured and taken for calculation of the external resistor connected to *MFIO* pin. The calculated resistor is then compared with 2 resistor thresholds. When the external resistor R_{EXT} is falling below the threshold $R_{MFIOOTPtrig}$[33] auto-restart mode is entered. An auto-restart cycle can only take place if R_{EXT} value is exceeding the threshold $R_{MFIOOTPrel}$. The auto-restart cycles after being triggered with an external overtemperature event are counted. When the number of external OTP events exceeds the threshold $N_{OTPevmax}$[33] latch mode is entered, which can be only released by VCC dropping below V_{VCCoff}.

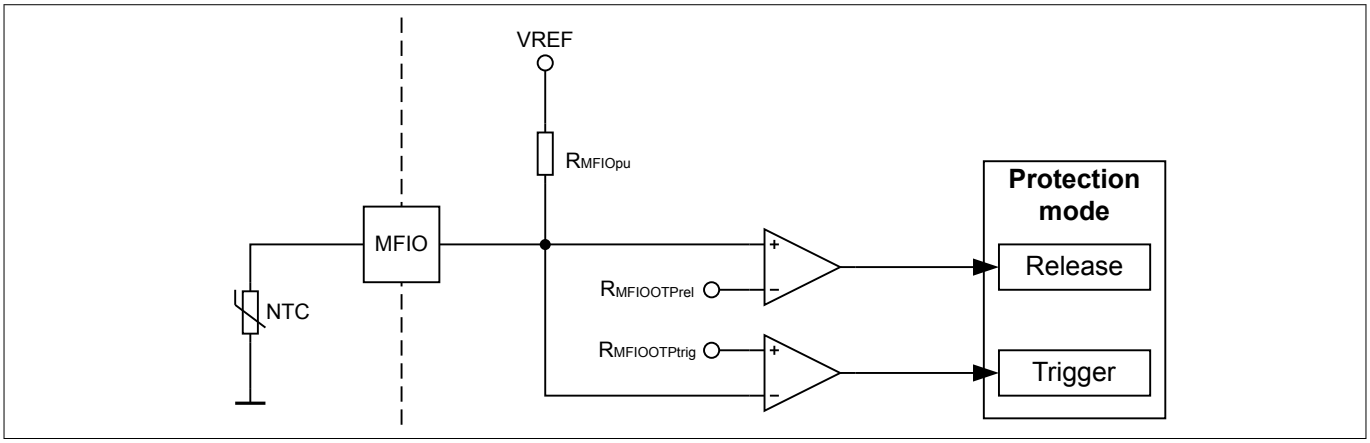


Figure 46

3.4.10 Watchdog timer

A watchdog timer is observing the internal control procedure by being continuously reset within a set time period. Once the timer is not reset in time a protection mode is entered, which is determined by the parameter EV_{WDOG}[34].

31 configurable, see ***Table 15***
32 configurable, see ***Table 11***
33 configurable, see ***Table 17***
34 configurable see ***Table 18***

4 Configuration

The configuration of XDPS2201 is supported by the GUI tool .dp Vision provided by Infineon. This chapter gives an overview about the configurable parameters, which are programmable via the UART interface at *MFIO* pin. ***Chapter 4.1*** shows the relationship between the parameter symbols described in the functional description and the parameter names shown in .dp Vision GUI tool. Furthermore the associated tolerance classes are assigned to the configurable typical parameters, which can be found in ***Chapter 4.2***.

4.1 Configurable parameters and functions

The following tables show the IC configurable parameters and their default programmed values, which some of them are either derived from or being configurable system parameters defined in XDP™Vision tool.

4.1.1 System settings

Table 5 System settings

Symbol	Description	Value	Unit	Tol.-Class	Chapter
N	Transformer turns ratio of primary winding N_p and secondary winding N_s, defined by N_p/N_s	2.83	—	—	***Chapter 3.4.6***
k_{Rvs}	Ratio of resistor divider connected at *VS* pin and bulk voltage	168.25	—	—	
V_{outnom}	Maximal nominal regulated output voltage	20	V	—	
I_{outnom}	Maximal nominal output current without over-current condition	3.25	A	—	

4.1.2 Dimensioning

Table 6 Dimensioning for output current control

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$I_{MAGnegnom\%}$	Nominal negative magnetizing current level in percentage in relation to $I_{outnom} \times 2/N$	17.4	%	—	***Chapter 3.3.1***
$I_{MAGnegmaxCRM\%}$	Maximum negative magnetizing current level in percentage in relation to $I_{outnom} \times 2/N$ required to achieve ZVS at maximum input voltage *Vin* during CRM operation	31.6	%	—	
$I_{MAGnegmaxRVS\%}$	Maximum negative magnetizing current level in percentage in relation to $I_{outnom} \times 2/N$ required to achieve ZVS at maximum input voltage *Vin* during ZV-RVS mode operation	39.5	%	—	
$I_{MAGposRVS0V\%}$	Minimum peak current setting determined by $I_{MAGposRVS}$ for *Vout* = 0V in percentage in relation to $I_{MAGposnom}$	75	%	—	***Chapter 3.3.2.2.1***
V_{ZCDnom}	*ZCD* pin nominal voltage during *LS* switch turn-on at V_{outnom}[35)]	1.3984	V	TC_V3a	***Chapter 3.3.1.2***

Table 6 Dimensioning for output current control (continued)

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$t_{TRANSnom}$	Minimum *LS* switch on-time during energy transfer at V_{outnom}	2.8	µs	TC_T1	
$t_{TRANSRVS0V\%}$	Representing the value t_{TRANS} in RVS mode for *Vout* = 0V in percentage in relation to $t_{TRANSnom}$ for t_{TRANS} modulation depending on output voltage measured via *ZCD* pin.	166	%	—	

4.1.3 Half-bridge

Table 7 Half-bridge timings

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$t_{LS2ZCDnom}$	Target time delay target for *LS* pulse falling edge to *ZCD* pulse falling edge at minimum *Vin*	650	ns	TC_T1	***Chapter 3.3.2.1***
$t_{LS2ZCDmin}$	Target time delay target for *LS* pulse falling edge to *ZCD* pulse falling edge at maximum *Vin*	234	ns	—	
t_{deadLS}	Dead-time between *HS* pulse falling edge and *LS* pulse rising edge	150	ns	TC_T1	
$t_{ZCDfefilCRM}$	Time delay between falling edge ZCD and *HS* pulse rising edge in CRM operation	172	ns	TC_T1	
t_{HSleb}	*HS* switch leading edge blanking (LEB) determining minimum on-time	300	ns	TC_T1	

Table 8 Half-bridge timings only for ZV-RVS mode

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$t_{deadHSRVS}$	Dead-time between *LS* (ZVS pulse) falling edge and *HS* pulse rising edge in ZV-RVS mode	400	ns	TC_T1	***Chapter 3.3.2.2***
t_{ZVSmin}	Minimum ZVS pulse width during ZV-RVS mode operation	600	ns	TC_T1	
$t_{ZCDrefilRVS}$	Filtering time between *ZCD* pulse rising edge and *HS* pulse rising edge in ZV-RVS mode operation	410	ns	TC_T1	
$t_{ZCDfefilRVS}$	Filtering time for *ZCD* pulse falling edge for valley detection in ZV-RVS mode operation	210	ns	TC_T1	***Chapter 3.3.2.2.1***

35 for wide output voltage range

4.1.4 ZV-RVS/DCM operation

Table 9 Transition between ZV-RVS mode and DCM operation

Symbol	Description	Value	Unit	Tol.-Class	Chapter
EN_{DCM}	Enable for DCM operation (when maximum valley in RVS operation is reached)	Enabled	—	n.a.	*Chapter 3.3.2.3*
F_{DCMmin}	Minimum switching frequency limit during DCM operation	20	kHz	TC_T1	
$N_{RVSvalmax}$	Maximum number of valleys during ZV-RVS operation	10	—	n.a.	*Chapter 3.3.2.4*

4.1.5 Burst

Table 10 Burst mode operation

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$I_{SETBMen\%}$	Burst mode entry current set-point in percentage of nominal set-point	4	%	—	*Chapter 3.3.4.1*
$I_{SETBMex\%}$	Burst mode exit current set-point in percentage of nominal set-point	15	%	—	*Chapter 3.3.4.4.1*
$N_{BMexreqthr}$	Number of burst frames with average current level higher than $I_{SETBMex\%}$ to leave burst mode	3	—	—	
$V_{FBBMfastex}$	*FB* pin fast burst mode exit threshold	1.82	V	TC_V4	*Chapter 3.3.4.4.2*
$EN_{BMfastexCRM}$	Allow for CRM operation directly after burst mode fast exit. If disabled, ZV-RVS mode is first used after burst mode fast exit.	Enabled	—	—	
$t_{BMprepulse}$	Pulse width to precharge the bootstrap capacitor after a pause longer than $t_{BMslpthrpp}$	1.3	µs	TC_T1	*Chapter 3.3.4.3*
$t_{BMslpthrpp}$	Burst pause time threshold for enabling precharge pulse	1.0	ms	TC_T2	

4.1.6 Start-up

Table 11 Start-up operation

Symbol	Description	Value	Unit	Tol.-Class	Chapter
V_{VSBIP}	*VS* pin threshold for input voltage *Vin* brown-in protection	0.737	V	TC_V1b	*Chapter 3.4.4.1*
$I_{SETstmax\%}$	Maximum target current set-point during start-up phase in percentage of nominal set-point	140	%	—	*Chapter 3.3.3*
$t_{startramp}$	Output voltage ramp-up target time period during start-up phase[36)]	12	ms	TC_T1	

Table 11 Start-up operation (continued)

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$N_{HBcyclemax}$	Maximum number of allowed half-bridge switching cycles without subsequent zero-crossing detection (ZCD) during ZCD search phase at *Vout* start-up	150	—	—	
$t_{startzcdto}$	Maximum time period without zero-crossing detection for generating next pulse[37] only during ZCD search phase	70	µs	TC_T1	
$t_{ZVSst1st}$	Very first ZVS pulse initial length at to precharge the *HS* bootstrap capacitor	7	µs	TC_T1	

4.1.7 Protections

Table 12 Auto-restart mode [ARM]

Symbol	Description	Value	Unit	Tol.-Class	Chapter
t_{ARMslp}	Approximated auto-restart mode sleep time period[38]	3.0	s	TC_T2	***Chapter 3.4.1***

Table 13 Input voltage Vin protection at VS pin

Symbol	Description	Value	Unit	Tol.-Class	Chapter
V_{VSSBOP}	*VS* pin threshold for input voltage *Vin* slow brown-out protection	0.713	V	TC_V1b	***Chapter 3.4.4.3***
V_{VSFBOP}	*VS* pin threshold for input voltage *Vin* fast brown-out protection	0.392	V	TC_V1b	***Chapter 3.4.4.2***
V_{VSOVP}	*VS* pin threshold for input voltage *Vin* overvoltage protection	2.270	V	TC_V1b	***Chapter 3.4.4.4***

Table 14 Start-up timeout protection

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$t_{startto}$	Maximum allowed start-up time until start drop of feedback voltage[36]	48	ms	TC_T3	***Chapter 3.3.3***

36 based on $t_{SLWTASK}$, see ***Table 35***
37 based on t_{MCLK}, see ***Table 35***
38 based on $t_{ARMbase}$, see ***Table 35***

Table 15 Vout voltage protection

Symbol	Description	Value	Unit	Tol.-Class	Chapter
V_{ZCDUVP}	*ZCD* pin undervoltage protection threshold for output voltage	0.220	V	TC_V3b	***Chapter 3.4.8.1***
$EN_{BMVoutUVP}$	Activation of *Vout* UVP in burst mode operation	Enable	—	—	
EV_{ZCDOVP}	Reaction event for *ZCD* pin overvoltage detection	Latch	—	—	***Chapter 3.4.8.2***

Table 16 Overcurrent protection

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$I_{SETOCP1lev1\%}$	Current set-point threshold in percentage of nominal set-point for OCP1 overcurrent protection level 1	125	%	—	***Chapter 3.4.7.1***
$t_{OCP1lev1bl}$	OCP1 overcurrent protection level 1 blanking time[39]	12	s	TC_T4	
$I_{SETOCP1lev2\%}$	Current set-point threshold in percentage of nominal set-point for OCP1 overcurrent protection level 2	140	%	—	***Chapter 3.4.7.2***
$t_{OCP1lev2bl}$	OCP1 overcurrent protection level 2 blanking time[36]	1000	ms	TC_T3	
$I_{SETOCP1max\%}$	Current set-point in percentage of nominal set-point for OCP1 maximum current limitation	160	%	—	***Chapter 3.4.7.3***
$t_{OCP1maxbl}$	OCP1 maximum current limitation blanking time[36]	6	ms	TC_T3	
EV_{CSOCP2}	Reaction on exceeding OCP2 overcurrent threshold	Latch	—	—	

Table 17 Overtemperature protection

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$R_{MFIOOTPtrig}$	*MFIO* pin external overtemperature protection trigger resistor threshold	7.7	kΩ	TC_R1	***Chapter 3.4.9***
$R_{MFIOOTPrel}$	*MFIO* pin external overtemperature protection release resistor threshold	51.4	kΩ	TC_R2	
$N_{OTPevmax}$	*MFIO* pin external overtemperature protection number of allowed triggered events before entering latch mode	2	—	—	

39 based on $t_{VSLWTASK}$, see ***Table 35***

36 based on $t_{SLWTASK}$, see ***Table 35***

Table 18 Watchdog timer

Symbol	Description	Value	Unit	Tol.-Class	Chapter
EV_{WDOG}	Reaction if watchdog timer is not reset in time	Auto-restart	—	—	***Chapter 3.4.10***

4.1.8 Mode thresholds

Table 19 CRM and ZV-RVS mode thresholds

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$I_{SETRVS2CRM\%}$	Current set-point threshold in percentage of nominal set-point for switching over from ZV-RVS mode to CRM	70	%	—	***Chapter 3.3.2.4***
$I_{SETCRM2RVS\%}$	Current set-point threshold in percentage of nominal set-point for switching over from CRM to ZV-RVS mode	50	%	—	
$V_{ZCDRVS2CRM}$	*ZCD* pin threshold for switching over from ZV-RVS mode to CRM	0.81	V	TC_V3a	
$V_{ZCDCRM2RVS}$	*ZCD* pin threshold for switching over from CRM to ZV-RVS mode	0.74	V	TC_V3a	

4.1.9 Jitter

Table 20 Frequency Jitter

Symbol	Description	Value	Unit	Tol.-Class	Chapter
$V_{VSJitteren}$	*VS* pin Input voltage Vin jitter enable threshold	1.486	V	TC_V1a	***Chapter 3.3.5***
$d_{Jitterspread\%}$	Frequency jitter spread on a percentage base of switching frequency	10	%	TC_T1	
$t_{Jitterstpdel}$	Time delay for next frequency jitter step based on time period[36)]	1.3	ms	TC_T1	

4.1.10 Others

Table 21 Propagation delay compensation (PDC)

Symbol	Description	Value	Unit	Tol.-Class	Chapter
t_{PDC}	Total propagation delay period to compensate OCP1 peak current control	200	ns	—	***Chapter 3.3.1.4***

36 based on $t_{SLWTASK}$, see ***Table 35***

4.2 Tolerance classes for configurable parameters

The are several configurable parameters for voltages, currents, timings, and frequencies and temperatures available, which are correlated with different tolerance ranges. The configurable parameters can be clustered based on the associated hardware peripheral. This clustering is done by means of tolerance classes, which are assigned to each configurable parameter. Parameters defining events, configuration registers, digital numbers or constants are not assigned to tolerance ranges.

The available tolerance classes are named with *TC_xxx* and listed in the following ***Table 22***. Described is how minimum and maximum tolerance values can be derived for the typical value X_{typ} of the configurable parameters.

Table 22 Tolerance classes

Tol.-Class	Description	Min. value	Max. value
TC_T1	Timing parameter below 1215ns [40]	t_{typ} x 0.95 - 15.8ns	t_{typ} x 1.05 + 15.8ns
	Timing parameter above 1215ns[40]	t_{typ} x 0.937	t_{typ} x 1.063
	Frequency parameter below 500kHz[40]	F_{typ} x 0.937	F_{typ} x 1.063
TC_T2	Timing parameter based on stand-by clock[41]	t_{typ} x 0.90	t_{typ} x 1.12
TC_T3	Timing parameter (integer multiple of 0.1ms) based on slow task period[42]	t_{typ} x 0.937 - 0.11ms	t_{typ} x 1.063 + 0.11ms
TC_T4	Timing parameter (integer multiple of 5ms) based on very slow task period[43]	t_{typ} x 0.937 - 5.5ms	t_{typ} x 1.063 + 5.5ms
TC_V1a	Voltage threshold at pin *VS*	(V_{VStyp} x 0.994) - 0.099V	(V_{VStyp} x 1.006) + 0.099V
TC_V1b	Voltage threshold at pin *VS*	(V_{VStyp} x 0.994) - 0.040V	(V_{VStyp} x 1.006) + 0.040V
TC_V2	Voltage threshold for OCP1 comparator at pin CS	$V_{CSOCP1typ}$ - 0.034V	$V_{CSOCP1typ}$ + 0.034V
TC_V3a	Voltage threshold at pin *ZCD*	(V_{ZCDtyp} x 0.995) - 0.091V	(V_{ZCDtyp} x 1.005) + 0.091V
TC_V3b	Voltage threshold at pin *ZCD*	(V_{ZCDtyp} x 0.995) - 0.024V	(V_{ZCDtyp} x 1.005) + 0.024V
TC_V4	Voltage threshold at pin *FB*	(V_{FBtyp} x 0.984) - 0.084V	(V_{FBtyp} x 1.016) + 0.084V
TC_R1	Range 1 for resistor threshold at pin *MFIO*	see ***Figure 47***	see ***Figure 47***
TC_R2	Range 2 for resistor threshold at pin *MFIO*	see ***Figure 48***	see ***Figure 48***

40 based on main clock t_{MCLK} = 15.8ns(typ.)
41 t_{STBCLK} = 10µs(typ.)
42 $t_{SLWTASK}$ = 0.1ms (typ.)
43 $t_{VSLWTASK}$ = 5ms (typ.)

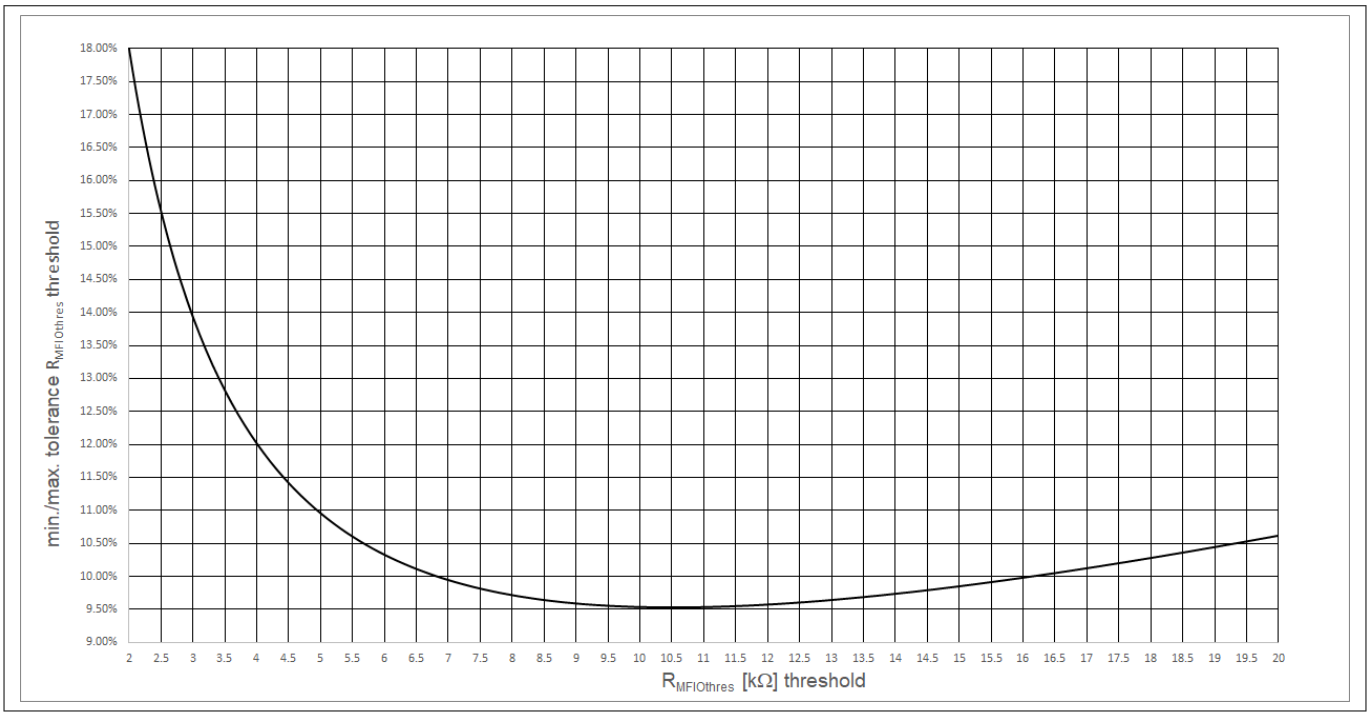


Figure 47 Tolerance class TC_R1 for resistor threshold $R_{MFIOthres}$ at pin *MFIO*

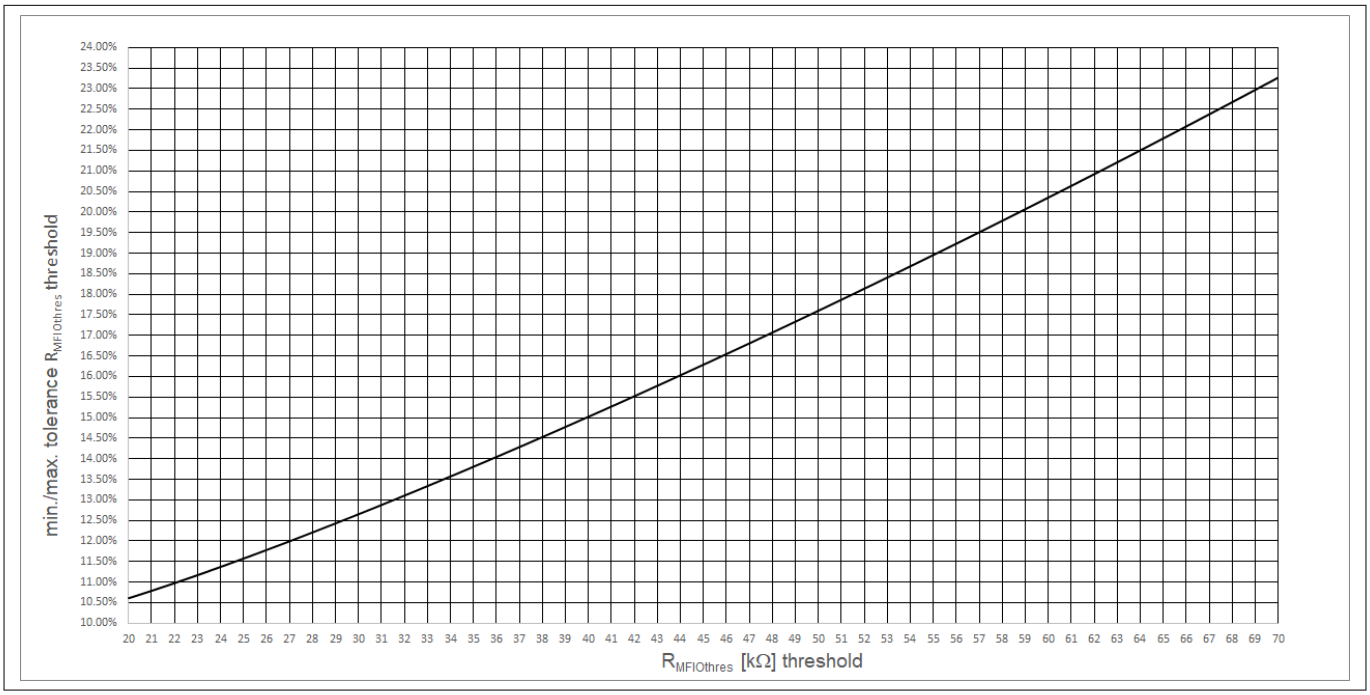


Figure 48 Tolerance class TC_R2 for resistor threshold $R_{MFIOthres}$ at pin *MFIO*

5 Electrical characteristics

All signals are measured with respect to ground pin *GND*, except the high-side signals at pins *HSVCC* and *HSGD*, which are measured with respect to pin *HSGND*. The voltage levels are valid if other ratings are not violated.

5.1 Definitions

Figure 49 illustrates the definition for the voltage and current parameters used in this data sheet.

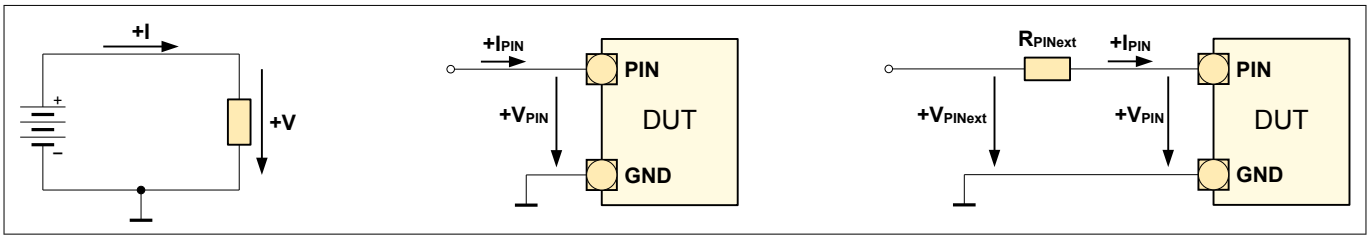


Figure 49 Voltage and current definitions

Values indicated under “absolute maximum ratings” must not be exceeded.

Values indicated under “operating conditions” can be exceeded if a corresponding explicit “absolute maximum rating” is given for this parameter, but the related function of the device is not ensured.

5.2 Absolute maximum ratings

Attention: ***Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test. For the same reason make sure that any capacitors that will be connected to pins VCC and HSVCC are discharged before assembling the application circuit.***

Table 23 Absolute maximum rantings

Parameter	Symbol	Limit values		Unit	Remarks
		Min.	Max.		
Voltage at pin *HV*	V_{HV}	–0.3	600	V	***44)***
Current into pin *HV*	I_{HV}	—	10	mA	***44)***
Voltage at pin *VCC*	V_{VCC}	–0.5	26	V	***44)***
Voltage at pin *MFIO*	V_{MFIO}	–0.5	3.6	V	***44)***
Voltage at pin *VS*	V_{VS}	–0.5	3.6	V	***44)***
Voltage at pin *FB*	V_{FB}	–0.5	3.6	V	***44)***
Voltage at pin *ZCD*	V_{ZCD}	–0.5	3.6	V	***44)***
Maximum negative transient voltage at pin *ZCD*	$-V_{ZCDN_TR}$	—	1.5	V	pulse < 500ns
Maximum permanent negative clamping current for pin *ZCD*	$-I_{ZCDCLN_DC}$	—	2.5	mA	RMS

44 Permanently applied as DC value.

Table 23 Absolute maximum rantings (continued)

Parameter	Symbol	Limit values		Unit	Remarks
		Min.	Max.		
Maximum transient negative clamping current for pin *ZCD*	$-I_{ZCDCLN_TR}$	—	10	mA	pulse < 500ns
Voltage at pin *CS*	V_{CS}	–0.5	3.6	V	[44]
Maximum negative transient voltage at pin *CS*	$-V_{CSN_TR}$	—	3.0	V	pulse < 500ns
Maximum permanent negative clamping current for pin *CS*	$-I_{CSCLN_DC}$	—	2.5	mA	RMS
Maximum transient negative clamping current for pin *CS*	$-I_{CSCLN_TR}$	—	10	mA	pulse < 500ns
Maximum permanent positive clamping current for pin *CS*	I_{CSCLP_DC}	—	2.5	mA	RMS
Maximum transient positive clamping current for pin *CS*	I_{CSCLP_TR}	—	10	mA	pulse < 500ns
Voltage at pin *LSGD*	V_{LSGD}	–0.5	V_{VCC}+0.3	V	Limited by internal clamping
Voltage at pin *HSGND*	V_{HSGND}	-650	650	V	referred to *GND*
Voltage at pin *HSVCC*	V_{HSVCC}	–0.5	26	V	referred to *HSGND*
Voltage at pin *HSGD*	V_{HSGD}	–0.5	V_{HSVCC}+0.3	V	referred to *HSGND*
Slew-rate for floating high-side domain	dV_{HS}/dt	–50	50	V/ns	
Junction operation temperature	T_J	–40	125	°C	
Storage temperature	T_S	–55	150	°C	
Maximum power dissipation	P_{TOT}	—	0.63	W	T_A = 50 °C, T_J = 125 °C, R_{thJA} = 119 K/W
Soldering temperature	T_{Sold}	—	260	°C	[45] Wave soldering
ESD capability	V_{HBM}	—	1500	V	[46] Human body model
	V_{CDM}	—	500	V	[47] Charged device model
Latch-up capability	I_{LU}	—	150	mA	[48] Pin voltages acc. to abs. max. ratings

44 Permanently applied as DC value.
45 According to JESD22-A111
46 According to ANSI/ESDA/JEDEC JS-001
47 According to JESD22-C101
48 According to JESD78, 85 °C (Class II) temperature

5.3 Package characteristics

Table 24 Package characteristics

Parameter	Symbol	Values		Unit	Remarks
		Min.	Max.		
Thermal resistance from junction to ambient	R_{thJA}	—	119	K/W	PG-DSO-14, JEDEC 1s0p
Creepage distance between HV and HSxxx pins vs. GND-related pins	D_{CR}	2.1	—	mm	

5.4 Operating range

Table 25 shows the recommended operating range.

Table 25 Operating conditions

Parameter	Symbol	Limit values		Unit	Remarks
		Min.	Max.		
Junction operation temperature	T_J	–25	125	°C	
Voltage at pin *HV*	V_{HV}	–0.3	600	V	
External voltage at pin *VCC*	V_{VCC}	11	24	V	Max. value needs to consider internal power losses
Voltage at pin *MFIO*	V_{MFIO}	–0.3	3.3	V	
Voltage at pin *FB*	V_{FB}	–0.3	3.3	V	
Voltage at pin *ZCD*	V_{ZCD}	–0.3	3.3	V	
Voltage at pin *CS*	V_{CS}	–0.3	3.3	V	
Voltage at pin *LSGD*	V_{LSGD}	–0.3	V_{VCC} + 0.3	V	Internally clamped at $V_{LSGDhigh}$
Low state output reverse current at pin *LSGD*	$-I_{LSGDLREV}$	—	100	mA	[49] Applies if V_{LSGD} < 0 V and driver at low state
Voltage at pin *HSGD*	V_{HSGD}	–0.3	V_{HSVCC} + 0.3	V	Internally clamped at $V_{HSGDhigh}$
Low state output reverse current at pin *HSGD*	$-I_{HSGDLREV}$	—	100	mA	[49] Applies if V_{HSGD} < 0 V and driver at low state
Voltage at pin *HSVCC*	V_{HSVCC}	10	24	V	Referred to *HSGND*
Voltage at pin *HSGND*	V_{HSGND}	–0.3	600	V	
UART Baudrate at pin *MFIO*	t_{BD}	10k	115k	Bd	

49 Assured by design.

5.5 DC electrical characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from –25 °C to 125 °C. Typical values represent the median values related to T_J = 25 °C. All voltages refer to *GND*, *HSGND* and the assumed supply voltage is V_{VCC} = 12 V and V_{HSVCC} = 12 V, if not otherwise mentioned.

The following characteristics are specified:

- Pin *HV* (***Table 26***)
- Pin *VCC* (***Table 27***)
- Floating HS domain (***Table 28***)
- Pin *LSGD* (***Table 29***)
- Pin *VS* (***Table 30***)
- Pin *CS* (***Table 31***)
- Pin *FB* (***Table 32***)
- Pin *MFIO* (***Table 33***)
- Pin *ZCD* (***Table 34***)
- Central control functions (***Table 35***)

Table 26 Electrical characteristics of Pin *HV*

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
HV peak VCC charge current capability	$I_{HVchargeVCC}$	2.4	5.0	7.5	mA	[50] V_{VCC} = 1 V, V_{HV} = 30 V
Leakage current at HV pin	I_{HVLK}	—	—	10	µA	V_{HV} = 600 V, HV start-up cell disabled

Table 27 Electrical characteristics of Pin *VCC*

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VCC turn-on threshold	V_{VCCon}	19.0	20.5	22.0	V	Rising slope
VCC turn-off threshold	V_{VCCoff}	7.98	8.40	8.82	V	Falling slope
VCC threshold for turning on the HV start-up cell during sleep mode	$V_{VCCslpHVon}$	9.97	10.50	11.03	V	Falling slope
VCC UVOFF current	$I_{VCCUVOFF}$	—	20	40	µA	$V_{VCC} < V_{VCCoff(min)} - 0.3$ V
VCC operating current	I_{VCCop}	—	11.0	14.5	mA	Without gate driver gate charge losses and during brown-in phase
VCC quiescent current during burst mode power saving-phase	$I_{VCCBMpsm0}$	—	0.7	3.4	mA	Burst mode entered; pin *MFIO* and *FB* open
		—	—	1.5	mA	as for $I_{VCCBMpsm0}$, T_J = 85 °C

50 Max. peak charge current will be limited in the application by an external resistor connected to HV pin.

Table 27 Electrical characteristics of Pin *VCC* (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VCC quiescent current during bang-bang mode	I_{VCCBB}	—	0.32	0.58	mA	Protection mode entered; pin *MFIO* and *FB* open

Table 28 Electrical characteristics of Floating HS domain

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
HSVCC turn-on threshold	$V_{HSVCCon}$	8.7	9.2	9.7	V	Rising slope
HSVCC turn-off threshold	$V_{HSVCCoff}$	6.2	6.7	7.2	V	Falling slope
HSVCC idle current	$I_{HSVCCidle}$	—	0.3	0.8	mA	Without gate driver gate charge losses, V_{HSVCC} = 14 V
HSGD enabling delay time after HSVCC voltage is exceeding $V_{HSVCCon}$*(max)*	$t_{HSGDendel}$	—	2.3	4.1	µs	V_{HSVCC} = 11 V
HSGD voltage at high state	$V_{HSGDhigh}$	10	11	12	V	I_{HSGD} = –20 mA
		7	—	—	V	I_{HSGD} = –20 mA, V_{HSVCC} = 8 V
HSGD voltage at active shutdown	$V_{HSGDaSD}$	—	25	200	mV	I_{HSGD} = 20 mA, V_{HSVCC} = 5 V
HSGD peak source current	$-I_{HSGDpksrc}$	130	—	—	mA	
HSGD peak sink current	$I_{HSGDpksnk}$	450	—	—	mA	

Table 29 Electrical characteristics of Pin *LSGD*

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
LSGD voltage at high state	$V_{LSGDhigh}$	9.9	10.5	11.1	V	I_{LSGD} = –20 mA
		7.5	—	—	V	I_{LSGD} = –20 mA, V_{VCC} = 8 V
LSGD voltage at active shutdown	$V_{LSGDaSD}$	—	—	1.6	V	I_{LSGD} = 5 mA, V_{VCC} = 5 V
LSGD peak source current	$-I_{LSGDpksrc}$	—	360	—	mA	
LSGD peak sink current	$I_{LSGDpksnk}$	800	—	—	mA	

Table 30 Electrical characteristics of Pin *VS*

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VS leakage current	I_{VSlk}	–0.2	—	0.2	µA	0 V < V_{VS} < 2.9 V
VS dynamic voltage range	V_{VS}	0	—	V_{REF}	V	
VS brown-in detection time period	$t_{VSBIdet}$	—	5.2	—	ms	Brown-in phase

Table 30 Electrical characteristics of Pin *VS* (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VS pin blanking time for input voltage *Vin* slow brown-out protection	$t_{VSSBOPbl}$	41.1	44.0	46.9	ms	$V_{VS} < V_{VSSBOP}$

Table 31 Electrical characteristics of Pin *CS*

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
CS leakage current	I_{CSlk}	–10	—	10	µA	$0\ V < V_{CS} < 2.8\ V$
CS OCP1 maximum operating current range	$V_{CSOPmax}$	405	437	469	mV	
CS OCP1 propagation delay	$t_{CSOCP1pd}$	121	213	305	ns	input signal slope, dV_{CS}/dt = 150 mV/µs
CS OCP2 threshold	V_{CSOCP2}	550	600	650	mV	
CS OCP2 propagation delay	$t_{CSOCP2pd}$	125	135	190	ns	dV_{CS}/dt = 100 V/µs

Table 32 Electrical characteristics of Pin *FB*

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
FB open circuit output voltage	V_{FBoc}	3.04	3.20	3.36	V	
FB pull-up resistor	R_{FBpu}	24	30	36	kΩ	
FB minimum operating range	$V_{FBOPmin}$	0.309	0.400	0.491	V	
FB threshold maximum usable range	$V_{FBOPmax}$	—	—	2.428	V	
FB burst mode wake-up and sleep control threshold	$V_{FBBMctrl}$	1.48	1.60	1.72	V	During active phase in burst mode
		1.36	1.55	1.61	V	During sleep phase in burst mode
FB burst mode wake-up delay	$t_{FBBMWKdel}$	—	25	31	µs	Burst mode, rising slope

Table 33 Electrical characteristics of Pin *MFIO*

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
MFIO open circuit output voltage	V_{MFIOoc}	—	V_{VREF}	—	V	During active phase
MFIO pull-up resistor	R_{MFIOpu}	—	11	—	kΩ	Active phase, internally calibrated for OTP resistor thresholds $R_{MFIOOTPx}$
MFIO input capacitance	C_{MFIOIN}	—	—	10	pF	

Table 33 Electrical characteristics of Pin *MFIO* (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
MFIO input threshold for logic “0”	V_{MFIOIL}	—	—	1.0	V	
MFIO input threshold for logic “1”	V_{MFIOIH}	2.0	—	—	V	
MFIO output voltage for logic “0”	V_{MFIOOL}	—	—	0.8	V	I_{MFIOOL} = 2 mA
MFIO output voltage for logic “1”	V_{MFIOOH}	2.2	—	—	V	I_{MFIOOH} = –2 mA
MFIO output sink current	I_{MFIOOL}	—	—	2	mA	
MFIO output source current	$-I_{MFIOOH}$	—	—	2	mA	
Output rise time (0 → 1)	$t_{MFIOrise}$	—	—	25	ns	20 pF load
Output fall time (1 → 0)	$t_{MFIOfall}$	—	—	25	ns	20 pF load

Table 34 Electrical characteristics of Pin *ZCD*

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
ZCD leakage current	I_{ZCDlk}	–10	—	10	µA	V_{ZCD} = 0 V / 3.0 V
		–1	—	1	µA	T_J = 85°C V_{ZCD} = 0V / 3.0V
ZCD threshold for Vout overvoltage protection	V_{ZCDOVP}	1.511	1.600	1.632	V	
ZCD voltage threshold for determining ZVS pulse length based on V_{ZCD}	$V_{ZCDtZVSstup}$	0.194	0.220	0.246	V	Start-up phase, rising slope
ZCD zero-crossing detection threshold	V_{ZCDTHR}	15	40	70	mV	Falling slope
ZCD input voltage negative clamping	$-V_{ZCDCLN}$	140	180	220	mV	

Table 35 Electrical characteristics of Central control functions

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VDDP power supply	V_{VDDP}	3.04	3.20	3.36	V	
VREF reference voltage	V_{VREF}	2.391	2.428	2.465	V	
Main clock oscillation period time base	t_{MCLK}	15.0	15.8	16.6	ns	
Stand-by clock oscillation period time base	t_{STBCLK}	9.0	10.0	11.2	µs	
Slow task period time base	$t_{SLWTASK}$	93	100	107	µs	
Very slow task period time base	$t_{VSLWTASK}$	4.68	5.00	5.32	ms	
Sampling time period	t_{sample}	93	100	107	µs	
Restart step time base for auto-restart mode	$t_{ARMbase}$	270	300	336	ms	Base for configurable auto-restart time t_{ARMslp} when auto-restart mode entered

Table 35 Electrical characteristics of Central control functions (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
HW initialization time period after IC activation for VCC turn-on	t_{HWini}	—	3.2	—	ms	$V_{VCC} > V_{VCCon}$ after UVOFF
Time period for initial start-up conditions check	$t_{stupcheck}$	1.80	—	2.13	ms	Start-up after $V_{VCC} > V_{VCCon}$
Limited maximum change in on-time control for *HS* switch during CRM operation	$\Delta t_{HSonmaxCRM}$	75	80	85	ns	CRM operation, t_{HSon} not limited by V_{CSSET}

6 Package dimensions

You can find all of our packages, sorts of packing and others in our Infineon internet page “Products: ***http://www.infineon.com/products***”.

PG-DSO-14 outline and footprint

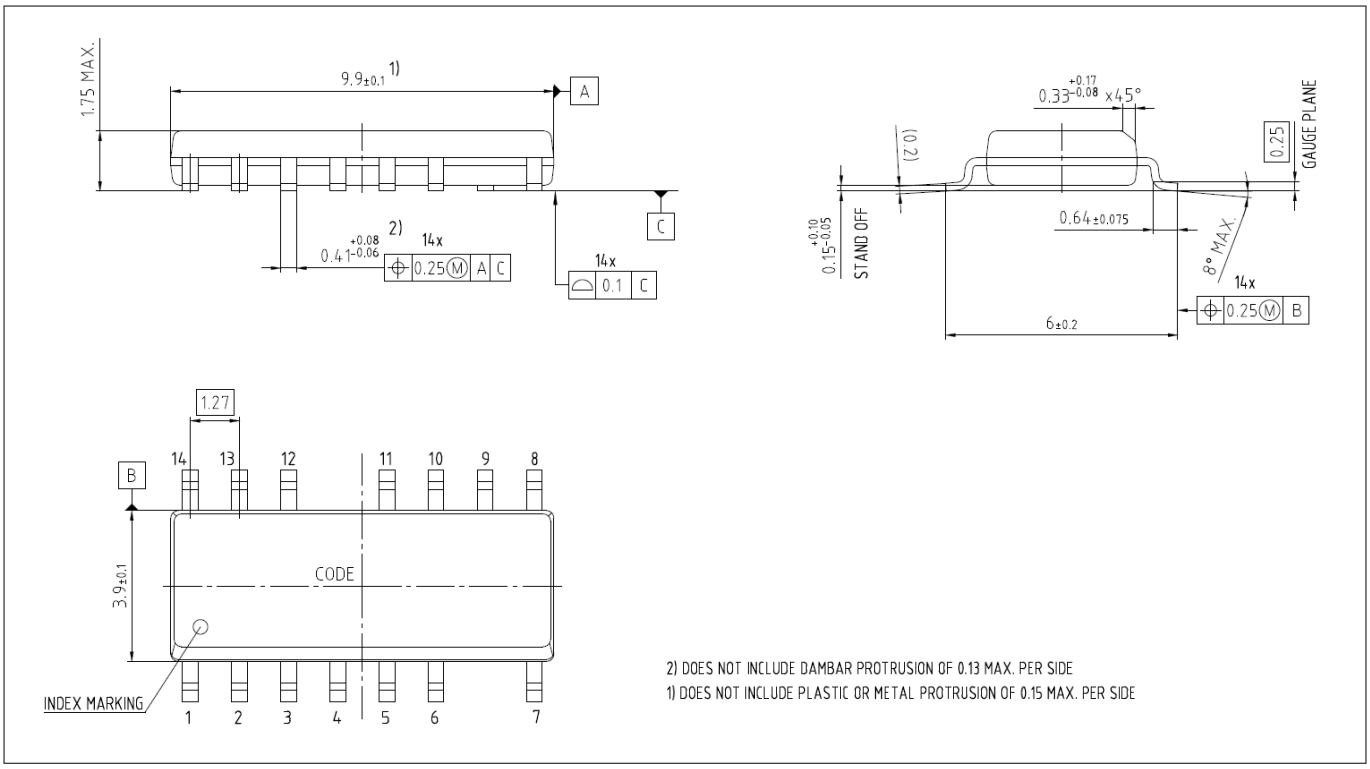


Figure 50 Outline

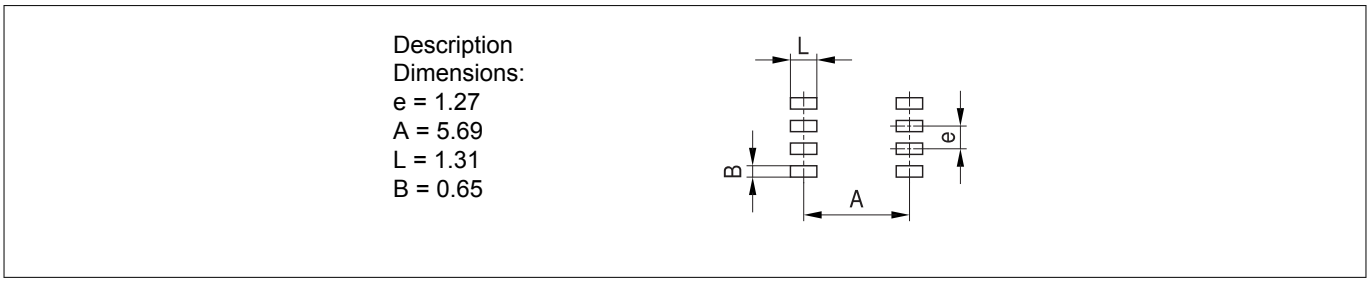


Figure 51 Footprint

Revision history

Document version	Date of release	Description of changes
R1.0	30.10.20	• Release of final datasheet
R1.1	20.01.21	• Corrected default value for V_{ZCDUVP} in table 15 • Added specification for I_{ZCDlk} in table 34 • Corrected tolerances for $V_{ZCDtZVSstup}$ in table 34 • Corrected TC_V3a and TC_V3b in table 22
R1.2	10.06.21	• Editorial corrections in ***Table 1*** • Corrected "mode transmission" to "mode transition" in ***Chapter 3.3.2*** • Corrected parameter names in ***Figure 19*** • Corrected default values of *N* in ***Table 5*** • Corrected default values of V_{ZCDnom} and $t_{Transnom}$ in ***Table 6*** • Corrected default value and description of $t_{LS2ZCDnom}$, description and tolerance class of $t_{LS2ZCDmin}$ in ***Table 7*** • Corrected description of $t_{ZCDrefilRVS}$ and $t_{ZCDfefilRVS}$ in ***Table 8*** • Corrected default value of $N_{RVSvalmax}$ in ***Table 9*** • Corrected default value of $I_{SETBMen\%}$, $I_{SETBMex\%}$, and $V_{FBBMfastex}$ in ***Table 10*** • Corrected default value of $N_{HBcyclemax}$ in ***Table 11*** • Corrected default value of V_{VSFBOP} in ***Table 13*** • Corrected tolerance class of $t_{startto}$ in ***Table 14*** • Corrected tolerance classes of $t_{OCP1lev1bl}$, $t_{OCP1lev2bl}$, and $t_{OCP1maxbl}$ in ***Table 16*** • Corrected default values of $I_{SETRVS2CRM\%}$ and $I_{SETCRM2RVS\%}$ in ***Table 19*** • Corrected default value of $d_{Jitterspread\%}$ in ***Table 20*** • Corrected default value of t_{PDC} in ***Table 21*** • Corrected LSGD peak source current $-I_{LSGDpksrc}$ in ***Table 29*** • Corrected VS pin blanking time for input voltage *Vin* slow brown-out protection $t_{VSSBOPbl}$ in ***Table 30*** • Corrected tolerance classes *TC_T1* and *TC_T2*, added tolerance classes *TC_T3* and *TC_T4* in ***Table 22*** • Corrected Slow task period time base $t_{SLWTASK}$, Very slow task period time base $t_{VSLWTASK}$, Sampling time period t_{sample}, Time period for initial start-up conditions check $t_{stupcheck}$, in ***Table 35*** • Removed Minimum HS switch on-time $t_{HSonmin}$ from ***Table 35*** which is configurable and duplicates t_{HSleb} in ***Table 7*** (refer to errata sheet ES_2105_PL21_2105_051535)

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