CMOS Digital Integrated Circuits Silicon Monolithic

TC7WPN3125FK

1. Functional Description

- Low-Voltage, Low-Power 2-Bit Dual-Supply Bus Buffer

2. General

The TC7WPN3125FK is a dual supply, advanced high-speed CMOS 2-bit dual supply voltage interface bus buffer fabricated with silicon gate CMOS technology.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V. Designed for use as an interface between a 1.2-V, 1.5-V, 1.8-V, or 2.5-V bus and a 1.8-V, 2.5-V or 3.6-V bus in mixed 1.2-V, 1.5-V, 1.8-V or 2.5-V/1.8-V, 2.5-V or 3.6-V supply systems.

The A-input interfaces with the 1.2-V, 1.5-V, 1.8-V or 2.5-V bus, the B-output with the 1.8-V, 2.5-V, 3.3-V bus.

The enable input $\overline{OE}$ can be used to disable the device so that the signal lines are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features (Note)

(1) Wide operating temperature range: T_{opr} = -40 to 125 °C (Note 1)

(2) Operating voltage: 1.2 V to 1.8 V / 1.2 V to 2.5 V / 1.2 V to 3.3 V / 1.5 V to 2.5 V
1.5 V to 3.3 V / 1.8 V to 2.5 V / 1.8 V to 3.3 V / 2.5 V to 3.3 V

(3) High-speed operation: t_{pd} = 13.7 ns (max) (V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 3.3 ± 0.3 V)
t_{pd} = 14.8 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 3.3 ± 0.3 V)
t_{pd} = 16.0 ns (max) (V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V)
t_{pd} = 29 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V)
t_{pd} = 18.5 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V)
t_{pd} = 19.7 ns (max) (V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V)
t_{pd} = 33 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V)
t_{pd} = 43 ns (max) (V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 1.8 ± 0.15 V)

(4) Output current: $|I_{OHB}|/I_{OLB}$ = 3 mA (min) (V_{CCB} = 3.0 V)
$|I_{OHB}|/I_{OLB}$ = 2 mA (min) (V_{CCB} = 2.3 V)
$|I_{OHB}|/I_{OLB}$ = 0.5 mA (min) (V_{CCB} = 1.65 V)

(5) Ultra-small package: US8

(6) Low power dissipation: By using the new circuit, the power consumption is reduced significantly when $\overline{OE}$ = "H".
Suitable for battery-driven applications such as PDAs and cellular phones.

(7) Floating of A-bus is permitted (when $\overline{OE}$ = "H").

(8) 3.6 V tolerance and power-down protection are provided to all inputs and outputs.

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

Note 1: For devices with the ordering part number ending in (CT. T_{opr} = -40 to 85 °C for the other devices.

Start of commercial production
2020-12

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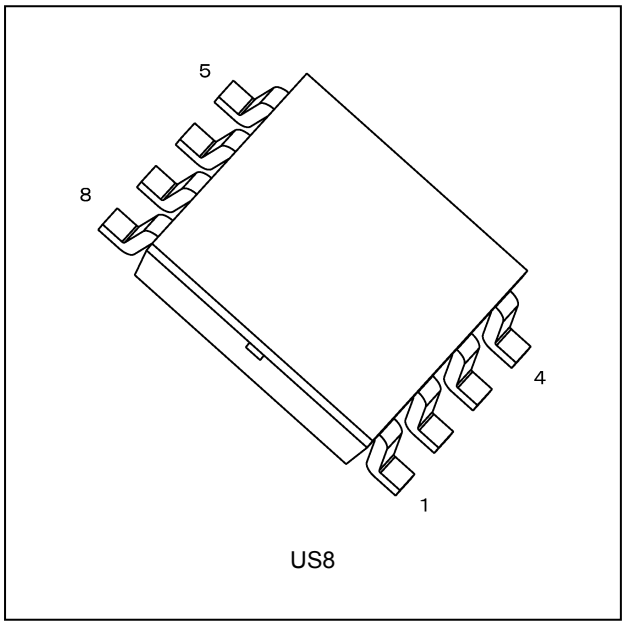
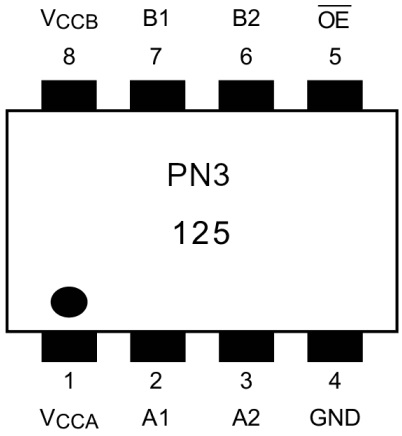
4. Packaging



US8

5. Pin Assignment



(Top view)

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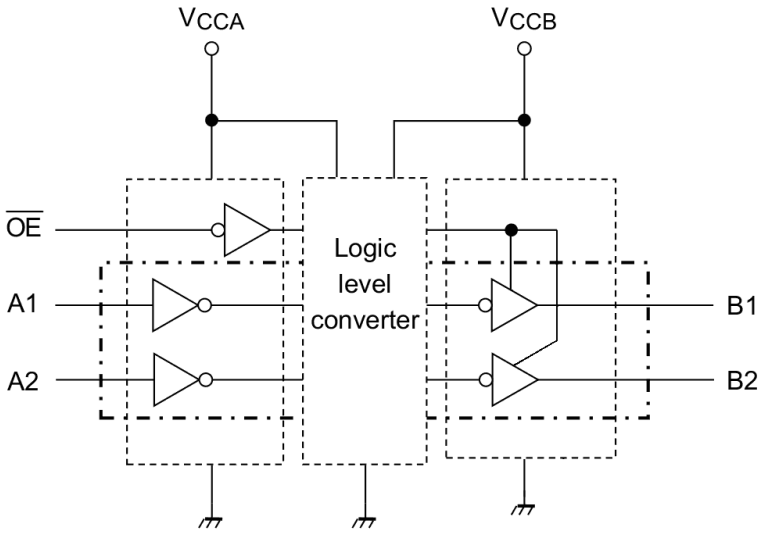
6. Truth Table

Input $\overline{OE}$	Input A1,A2	Outputs B1,B2
L	L	L
L	H	H
H	X	Z

X: Don't care
Z: High impedance

7. Block Diagram



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8. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCA}	(Note 1)	-0.5 to 4.6	V
	V_{CCB}		-0.5 to 4.6	
Input voltage (An, $\overline{OE}$)	V_{IN}		-0.5 to 4.6	V
Output voltage (Bn)	V_{OUTB}	(Note 2)	-0.5 to 4.6	V
		(Note 3)	-0.5 to V_{CCB} + 0.5	
Input diode current	I_{IK}		-50	mA
Output diode current	I_{OK}	(Note 4)	±50	mA
Output current	I_{OUTB}		±6	mA
V_{CC}/ground current per supply pin	I_{CCA}		±25	mA
	I_{CCB}		±50	
Power dissipation	P_D		200	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Don't supply a voltage to V_{CCB} pin when V_{CCA} is in the OFF state.
Note 2: Output in OFF state.
Note 3: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.
Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

9. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CCA}	(Note 1)	—	1.1 to 2.7	V
	V_{CCB}			1.65 to 3.6	
Input voltage (An, $\overline{OE}$)	V_{IN}		—	0 to 3.6	V
Output voltage (Bn)	V_{OUTB}	(Note 2)	—	0 to 3.6	V
		(Note 3)		0 to V_{CCB}	
Output current (Bn)	I_{OUTB}		V_{CCB} = 3.0 to 3.6 V	±3	mA
			V_{CCB} = 2.3 to 2.7 V	±2	
			V_{CCB} = 1.65 to 1.95 V	±0.5	
Operating temperature	T_{opr}	(Note 4)	—	-40 to 125	°C
		(Note 5)		-40 to 85	
Input rise and fall times	dt/dv		V_{IN} = 0.8 to 2.0 V, V_{CCA} = 2.5 V, V_{CCB} = 3.0 V	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 1: Don't use at V_{CCA} > V_{CCB}.
Note 2: Output in OFF state.
Note 3: High (H) or Low (L) state.
Note 4: For devices with the ordering part number ending in (CT.
Note 5: For devices except those with the ordering part number ending in (CT.

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10. Electrical Characteristics

10.1. DC Characteristics

10.1.1. 1.1 V ≤ V_{CCA} ≤ 2.7 V, 1.65 V < V_{CCB} ≤ 3.6 V (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Sym-bol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	V_{IN}		1.1 ≤ V_{CCA} ≤ 1.4	1.65 to 3.6	0.65× V_{CCA}	—	V
				1.4 ≤ V_{CCA} ≤ 1.65	1.65 to 3.6	0.65× V_{CCA}	—	
				1.65 ≤ V_{CCA} ≤ 2.3	2.3 to 3.6	0.65× V_{CCA}	—	
				2.3 ≤ V_{CCA} ≤ 2.7	2.7 to 3.6	1.6	—	
Low-level input voltage	V_{ILA}	V_{IN}		1.1 ≤ V_{CCA} ≤ 1.4	1.65 to 3.6	—	0.3× V_{CCA}	V
				1.4 ≤ V_{CCA} ≤ 1.65	1.65 to 3.6	—	0.3× V_{CCA}	
				1.65 ≤ V_{CCA} ≤ 2.3	2.3 to 3.6	—	0.35× V_{CCA}	
				2.3 ≤ V_{CCA} ≤ 2.7	2.7 to 3.6	—	0.7	
High-level output voltage	V_{OHB}	An = V_{IH}	I_{OHB} = -100 μA	1.1 to 2.7	1.65 to 3.6	V_{CCB} -0.2	—	V
			I_{OHB} = -0.5 mA	1.1 to 1.65	1.65	1.25	—	
			I_{OHB} = -2 mA	1.1 to 2.3	2.3	1.7	—	
			I_{OHB} = -3 mA	1.1 to 2.7	3.0	2.2	—	
Low-level output voltage	V_{OLB}	An = V_{IL}	I_{OLB} = 100 μA	1.1 to 2.7	1.65 to 3.6	—	0.2	V
			I_{OLB} = 0.5 mA	1.1 to 1.65	1.65	—	0.3	
			I_{OLB} = 2 mA	1.1 to 2.3	2.3	—	0.6	
			I_{OLB} = 3 mA	1.1 to 2.7	3.0	—	0.55	
3-state output OFF-state leakage current	I_{OZB}	An = V_{IHA} or V_{ILA} Bn = 0 to 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±2.0	μA
Input leakage current	I_{IN}	V_{IN} = 0 to 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±1.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, Bn = 0 to 3.6 V		0	0	—	2.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} An, Bn = 0 to 3.6 V		1.1 to 2.7	0	—	2.0	
	I_{OFF3}			1.1 to 2.7	Open	—	2.0	
Quiescent supply current	I_{CCA}	V_{IN} = V_{CCA} or GND		1.1 to 2.7	1.65 to 3.6	—	2.0	μA
	I_{CCB}	V_{IN} = V_{CCA} or GND		1.1 to 2.7	1.65 to 3.6	—	2.0	
	I_{CCA}	V_{CCA} ≤ V_{IN} ≤ 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±2.0	
	I_{CCB}	V_{IN} = V_{CCA} V_{CCB} ≤ Bn ≤ 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±2.0	

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10.1.2. 1.1 V ≤ V_{CCA} ≤ 2.7 V, 1.65 V < V_{CCB} ≤ 3.6 V (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Sym-bol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	V_{IN}		1.1 ≤ V_{CCA} ≤ 1.4	1.65 to 3.6	0.65× V_{CCA}	—	V
				1.4 ≤ V_{CCA} ≤ 1.65	1.65 to 3.6	0.65× V_{CCA}	—	
				1.65 ≤ V_{CCA} ≤ 2.3	2.3 to 3.6	0.65× V_{CCA}	—	
				2.3 ≤ V_{CCA} ≤ 2.7	2.7 to 3.6	1.6	—	
Low-level input voltage	V_{ILA}	V_{IN}		1.1 ≤ V_{CCA} ≤ 1.4	1.65 to 3.6	—	0.3× V_{CCA}	V
				1.4 ≤ V_{CCA} ≤ 1.65	1.65 to 3.6	—	0.3× V_{CCA}	
				1.65 ≤ V_{CCA} ≤ 2.3	2.3 to 3.6	—	0.35× V_{CCA}	
				2.3 ≤ V_{CCA} ≤ 2.7	2.7 to 3.6	—	0.7	
High-level output voltage	V_{OHB}	An = V_{IH}	I_{OHB} = -100 μA	1.1 to 2.7	1.65 to 3.6	V_{CCB} -0.2	—	V
			I_{OHB} = -0.5 mA	1.1 to 1.65	1.65	1.15	—	
			I_{OHB} = -2 mA	1.1 to 2.3	2.3	1.6	—	
			I_{OHB} = -3 mA	1.1 to 2.7	3.0	2.0	—	
Low-level output voltage	V_{OLB}	An = V_{IL}	I_{OLB} = 100 μA	1.1 to 2.7	1.65 to 3.6	—	0.2	V
			I_{OLB} = 0.5 mA	1.1 to 1.65	1.65	—	0.45	
			I_{OLB} = 2 mA	1.1 to 2.3	2.3	—	0.8	
			I_{OLB} = 3 mA	1.1 to 2.7	3.0	—	0.8	
3-state output OFF-state leakage current	I_{OZB}	An = V_{IHA} or V_{ILA} Bn = 0 to 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±20.0	μA
Input leakage current	I_{IN}	V_{IN} = 0 to 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±10.0	μA
Power-off leakage current	I_{OFF1}	V_{IN}, Bn = 0 to 3.6 V		0	0	—	20.0	μA
	I_{OFF2}	$\overline{OE}$ = V_{CCA} An, Bn = 0 to 3.6 V		1.1 to 2.7	0	—	20.0	
	I_{OFF3}			1.1 to 2.7	Open	—	20.0	
Quiescent supply current	I_{CCA}	V_{IN} = V_{CCA} or GND		1.1 to 2.7	1.65 to 3.6	—	20.0	μA
	I_{CCB}	V_{IN} = V_{CCA} or GND		1.1 to 2.7	1.65 to 3.6	—	20.0	
	I_{CCA}	V_{CCA} ≤ V_{IN} ≤ 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±20.0	
	I_{CCB}	V_{IN} = V_{CCA} V_{CCB} ≤ Bn ≤ 3.6 V		1.1 to 2.7	1.65 to 3.6	—	±20.0	

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10.2. AC Characteristics

10.2.1. V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	13.7	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	16.6	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	7.2	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	0.5	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

10.2.2. V_{CCA} = 2.5 ± 0.2 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	14.7	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	18.5	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	8.1	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.0	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

10.2.3. V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	14.8	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	18.9	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	8.7	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	0.5	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

10.2.4. V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	15.8	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	20.5	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	9.5	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.0	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

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10.2.5. V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	16.0	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	22.8	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	10.2	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

10.2.6. V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	17.0	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	23.4	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	10.5	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	2.0	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

10.2.7. V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	29	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	63	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	23	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

10.2.8. V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	29	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	63	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	23	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	2.0	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

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10.2.9. V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	18.5	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	23.6	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	6.9	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	0.5	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

10.2.10. V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	19.9	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	25.8	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	7.8	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.0	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

10.2.11. V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	19.7	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	26.6	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	8.3	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

10.2.12. V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	20.8	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	27.9	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	8.6	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	2.0	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

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10.2.13. V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	33	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	66	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	20	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

10.2.14. V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	33	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	66	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	20	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	2.0	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

10.2.15. V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 1.8 ± 0.15 V (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	43	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	78	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	20	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	1.5	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

10.2.16. V_{CCA} = 1.2 ± 0.1 V, V_{CCB} = 1.8 ± 0.15 V (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	43	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{PZL}/t_{PZH}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	78	
3-state output disable time ($\overline{OE}$ → Bn)	t_{PLZ}/t_{PHZ}		See Fig. 11.1, 12.1 Table 11.1.1, 11.1.2, 12.1.1	1.0	20	
Output skew	t_{osLH}/t_{osHL}	(Note 1)		—	2.0	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

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10.3. Capacitive Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note		V_{CCA} (V)	V_{CCB}(V)	Typ.	Unit
Input capacitance	C_{IN}		An,$\overline{OE}$	2.5	3.3	7	pF
Output capacitance	C_{OUT}		Bn	2.5	3.3	8	pF
Power dissipation capacitance	C_{PDA}	(Note 1)	$\overline{OE}$ = "L"	2.5	3.3	3	pF
		(Note 1)	$\overline{OE}$ = "H"	2.5	3.3	0	
	C_{PDB}	(Note 1)	$\overline{OE}$ = "L"	2.5	3.3	13	
		(Note 1)	$\overline{OE}$ = "H"	2.5	3.3	0	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per bit)

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11. AC Test Circuit

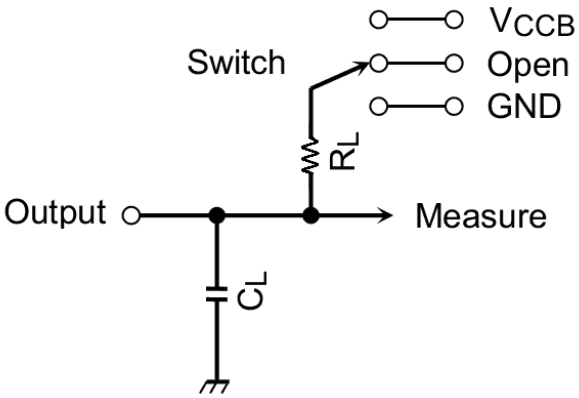

Fig. 11.1 AC Test Circuit

Table 11.1.1 Parameter for AC Test Circuit

Parameter	Switch
t_{PLH}, t_{PHL}	Open
t_{PLZ}, t_{PZL}	V_{CCB}
t_{PHZ}, t_{PZH}	GND

Table 11.1.2 Parameter for AC Test Circuit

Symbol	V_{CCB} = 3.3 ± 0.3 V V_{CCB} = 2.5 ± 0.2 V	V_{CCB} = 1.8 ± 0.15 V
R_L	1 kΩ	1 kΩ
C_L	30 pF	30 pF

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12. AC Waveform

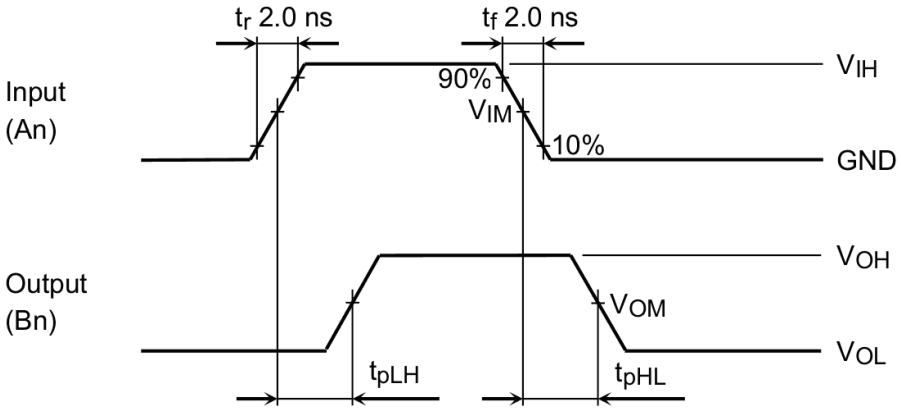

Fig. 12.1 t_{PLH}, t_{PHL}

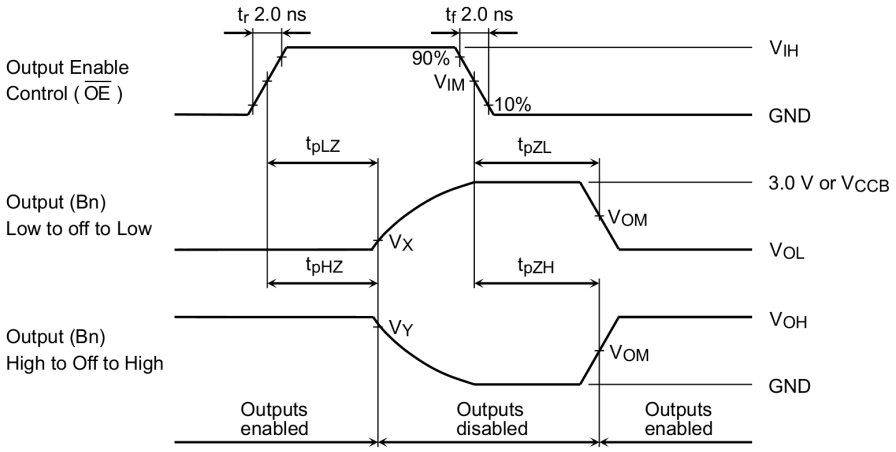

Fig. 12.2 t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

Table 12.1.1 AC Waveform Symbols

Symbol	V_{CC} = 3.3 ± 0.3 V	V_{CC} = 2.5 ± 0.2 V V_{CC} = 1.8 ± 0.15 V	V_{CC} = 1.5 ± 0.1 V V_{CC} = 1.2 ± 0.1 V
V_{IH}	—	V_{CCA}	V_{CCA}
V_{IM}	—	$V_{CCA}/2$	$V_{CCA}/2$
V_{OM}	$V_{OH}/2$	$V_{OH}/2$	—
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	—
V_Y	V_{OH} - 0.3 V	V_{OH} - 0.15 V	—

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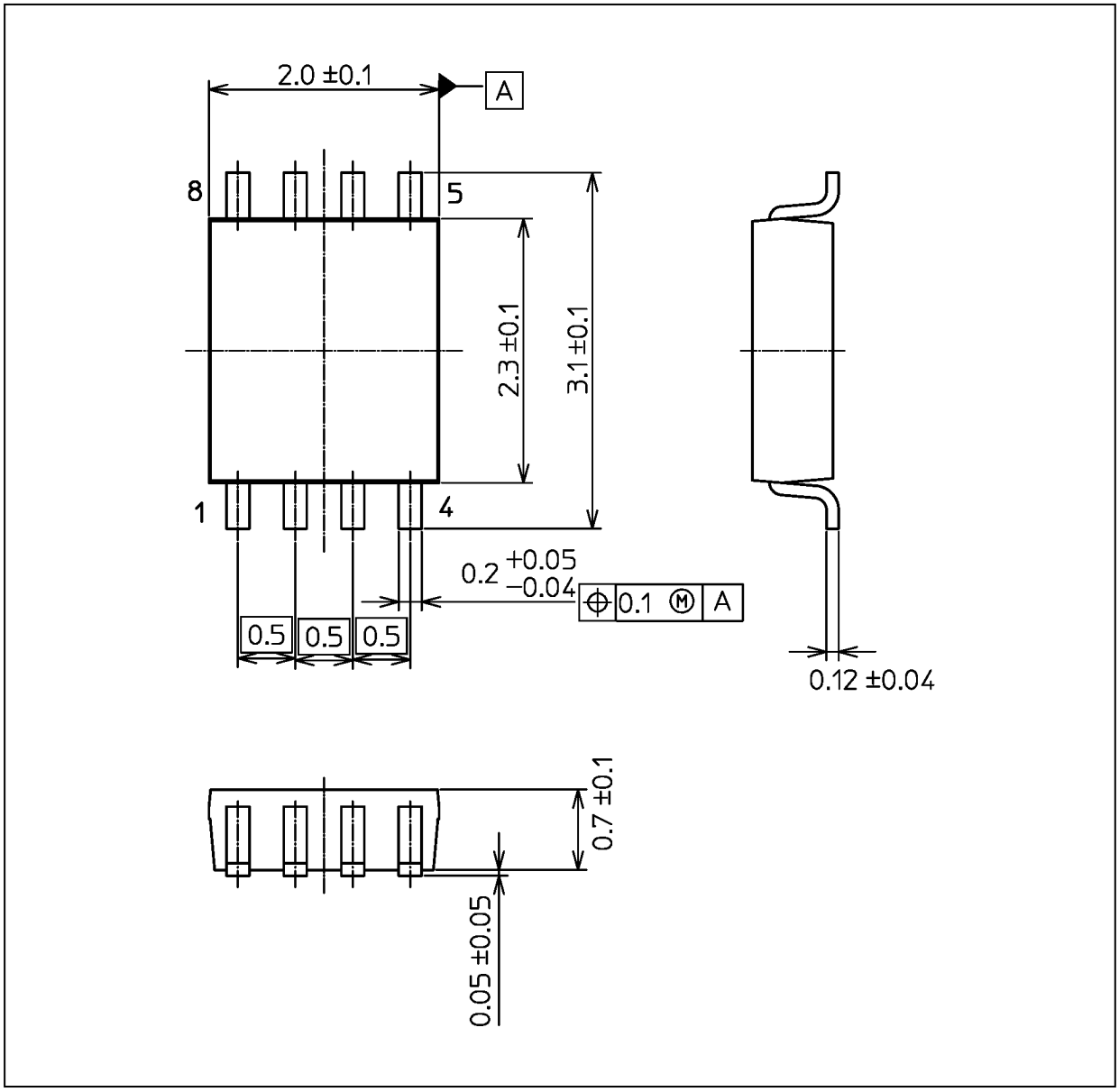
Package Dimensions

Unit: mm



Weight: 0.01 g (typ.)

Package Name(s)
JEDEC: SOT-765
Nickname: US8

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