IVCC1102 CCM Totem-Pole PFC Controllers

1 Features

- SOIC-16 and QFN 4x4 20L packages
- 5V VCC with UVLO
- 2 line-frequency switch and 2 high-frequency PWM gate drive signals
- Optimized AC current zero-crossing control
- Average current mode control with fixed ratio input voltage feedforward
- Auto reverse current prevention at AC drop
- Optimized step load response with non-linear voltage loop and accelerated current loop
- Low THD with Vo harmonic rejection sensing
- Up to 150kHz programmable PWM frequency
- Overvoltage Protection, Open-Loop Protection,
- AC Overvoltage Protection and UVLO
- Peak Current Limiting
- Burst mode options
- Burst starts at Vac zero-crossing to minimize audible noise
- Suitable for both AC and DC inputs
- Suitable for hall and resistor current sensing
- Suitable for over 400Hz PFC control
- Relay signal, synchronized with Vac, ease timing control to reduce inrush current

2 Applications

- Server Power supplies
- Compact PFC power modules
- TV and gaming Xbox power supplies
- High power phone and laptop chargers
- Avionics power supplies

3 Description

The IVCC1102 is a high-speed, precise and compact totem-pole PFC analog controller.

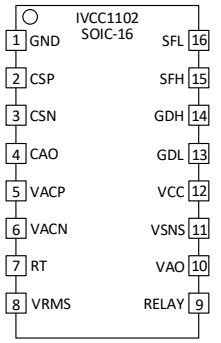
It employs the advanced average current mode and fixed-ratio input voltage feedforward control. The control generates a duty cycle baseline D' = Vin/400V, while the current loop just provides small duty cycle adjustment. It essentially speeds up the current loop and results in excellent current command tracking. For the same reason, when AC drops abruptly, the PWM duty cycle can be adjusted without delay, which prevents the boost inductor current from reversing. The IVCC1102 controller can be used for high AC frequency avionics power factor correction, which usually operates at 400Hz.

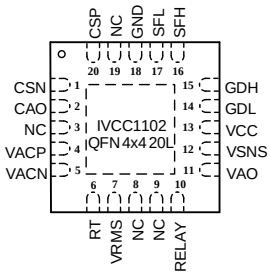
For the voltage loop, output Vo is sampled and held at Vac zero-crossing. By doing so, the Vo's second harmonic is rejected and Vo average voltage is precisely sensed. A non-linear control is added to accelerate the voltage loop when output voltage error exceeds 5% of the set value. A high frequency (about 200kHz) soft-start PWM pattern is inserted at each AC crossover point to smooth out the AC current waveform.

Device Information

PART NUMBER	PACKAGE	PACKING
IVCC1102DR	SOIC-16	Tape and Reel
IVCC1102F4AR	QFN 4x4 20L	Tape and Reel

Pinout





Contents

1 Features 1
2 Applications 1
3 Description 1
4 Pin Configuration and Functions 4
5 Specifications 5
5.1 Absolute Maximum Ratings 5
5.2 ESD Rating 5
5.3 Recommended Operation Conditions 5
5.4 Thermal Information 5
5.5 Electrical Specifications 6
6 Function Description 8
6.1 Functional Block Diagram 8
6.2 Relay Control and Start Up 8
6.2.1 Relay Control 8
6.2.2 Soft Start Up 9
6.3 Protection Features 9
6.3.1 UVLO 9
6.3.2 Open Loop Protection (OLP) 9
6.3.3 Over Voltage Protection (OVP) 9
6.4 Current Loop 9
6.4.1 Current Sense (CS) 9
6.4.2 Peak Current Limit (PCL) and Constant Current Limit 9
6.4.3 Current Error Amplifier (CEA) 9
6.5 Voltage Loop 10
6.5.1 Output Voltage Sensing (VSNS) 10
6.5.2 Voltage Error Amplifier (VEA) 10
6.5.3 Multiplier (MP) 11
6.5.4 AC Fixed-Ratio Feed-Forward (ACFF) 11
6.6 PWM and Timing 11
6.6.1 Frequency (RT) 11
6.6.2 Deadtime (DT) 11
6.7 AC Zero-Crossing 11

6.8 Burst Mode 12
6.9 Bootstrap supporting PWM 12
6.10 Gate Drive Outputs 12
7 Typical Characteristics 13
8 Application Implementation 14
8.1 Typical Applications 14
8.2 Design Calculation Example (2.5kW Totem-Pole PFC Reference Design) 17
8.2.1 PFC Specifications 17
8.2.2 Circuit Parameter Selection 17
8.2.3 Control Loops 18
8.3 2.5kW Reference Design Waveforms 21
9 Package Information 25

4 Pin Configuration and Functions

IVCC1102DR	IVCC1102F4AR	NAME	I/O	DESCRIPTION
1	18	GND	G	Ground
2	20	CSP	I	Current Sense Positive Input
3	1	CSN	I	Current Sense Negative Input
4	2	CAO	O	Current Loop Amplifier Output
5	4	VACP	I	AC Amp Non-Inverting Input, Connected to AC Line or DC+ Input
6	5	VACN	I	AC Amp Inverting Input, Connected to AC Neutral or DC- Input
8	7	VRMS	I	AC RMS Voltage
9	10	RELAY	O	Relay Control Output, A pull-down resistor is used for deadtime programming
7	6	RT	I	Switching Frequency Programming
10	11	VAO	O	Voltage Loop Amplifier Output
11	12	VSNS	I	Output Voltage Sense
12	13	VCC	P	Power Supply
13	14	GDL	O	High Frequency Gate Drive Low Side MOSFET
14	15	GDH	O	High Frequency Gate Drive High Side MOSFET
15	16	SFH	O	Line Frequency Gate Drive High Side MOSFET
16	17	SFL	O	Line Frequency Gate Drive Low Side MOSFET

5 Specifications

5.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Total supply voltage	-0.3	5.5	V
GDL, GDH, SFH, SFL, RELAY	Gate driver output voltage	-0.3	V_{CC}+0.3	V
CAO, VREF, VACP, VACN, VACO, VRMS, RT, VAO, VSNS	Signal input/output voltage	-0.3	V_{CC}+0.3	V
CSP, CSN	Current sense input voltage	-24	V_{CC}+0.3	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

5.2 ESD Rating

		Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operation Conditions

		MIN	MAX	UNIT
V_{CC}	Total supply voltage	4.75	5.25	V
CSP, CSN	Current sense input voltage	-0.3	4	V
T_A	Operating ambient temperature	-40	125	°C

5.4 Thermal Information

	IVCC1102DR	IVCC1102F4AR	UNIT
$R_{\theta JA}$ Junction-to-Ambient	90	41	°C/W

5.5 Electrical Specifications

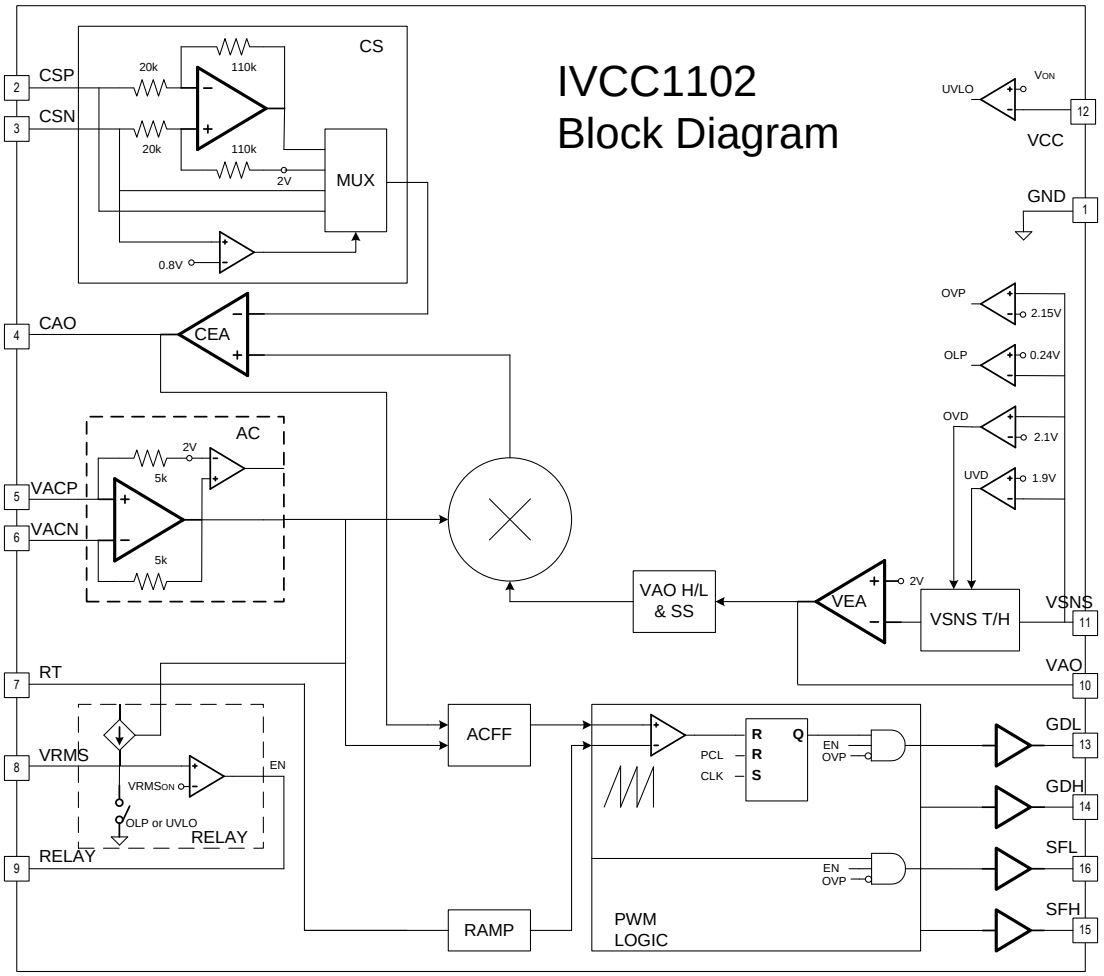
Unless otherwise noted, V_{CC} = 5 V, T_A = –40°C to 125°C
Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current						
I_{CCq}	Quiescent supply current	VSNS = 0V		4	6	mA
I_{CC}	Operating supply current	VSNS = 2.05V		4.5	8	mA
I_{CCoff}	Below UVLO supply current	VCC = 3V		1	3	mA
UVLO						
V_{ON}	Under voltage lockout thresholds	Rising threshold		3.76	4.2	V
V_{OFF}		Falling threshold	3.3	3.64		V
SWITCHING FREQUENCY						
V_{RT}	RT voltage	Measure RT voltage	0.75	0.8	0.85	V
FREQ	Switching frequency	R_{RT}=27kΩ	58	65	75	kHz
		R_{RT}=18kΩ	88	100	112	kHz
AC INPUT						
G_{AC}	AC amplifier gain with resistor feedback	External Rac = 10kΩ	0.45	0.5	0.56	V/V
CURRENT AMPLIFIER						
GM_C	Current amplifier transconductance			50		uS
$ICAO_U$	CAO source current	VAO-VACP=1.5V		-62		uA
$ICAO_D$	CAO sink current	VAO-VACP=0V		71		uA
CURRENT SENSE						
VCS_{BP}	CS amplifier bypass threshold	measured at CSN	0.77	0.8	0.83	V
G_{CS}	CS amplifier gain		5.3	5.44	5.6	V/V
VCS_{CM}	CS amplifier input range	Shunt resistor sensing	-0.3		0.3	V
PCL	Peak current limit at CS amplifier output	CSP-CSN, measured at CSN=2V	1.51	1.61	1.71	V
VOLTAGE AMPLIFIER and FEEDBACK						
GM_V	Voltage amplifier transconductance			140		uS
$IVAO_U$	VAO source current	VSNS=1.8V, VAO-VACP=1.5V		-73		uA
$IVAO_D$	VAO sink current	VSNS=OVD+20mV, VAO-VACP=0V		54		uA
VREF	Reference voltage	25°C	-1%	2	1%	V
		-40℃~125℃	-2%	2	2%	V
OVP	Over voltage protection threshold	VSNS/VREF	105.3	107.3	109.3	%
OVD	Over voltage dynamic response threshold	VSNS/VREF	103	105	107	%
UVD	Under voltage dynamic response	VSNS/VREF	93.3	95.3	97.3	%

	threshold					
OLP	Open loop protection threshold	Measured at VSNS falling	0.22	0.24	0.28	V
DEADTIME						
DT_m	Deadtime from main switch to free-wheeling switch	R_{DT2} = 39kΩ	140	183	250	ns
DT_{fw}	Deadtime from free-wheeling switch to main switch	R_{DT2} = 39kΩ	70	98	135	ns
VRMS and RELAY						
Irms	VRMS output current	equivalent AC amplifier output 1V, external Rac=10kΩ, measured at VRMS = 0.5V	-66	-52	-41	uA
$VRMS_{ON}$	VRMS rising threshold voltage		0.77	0.84	0.9	V
$VRMS_{HYS}$	VRMS hysteresis			0.26		V
OUTPUTS						
V_{OH}	Output high voltage	I_{OUT} = 10mA		0.12	0.23	V
V_{OL}	Output low voltage	I_{OUT} = 10mA		0.05	0.11	V
T_R	Rise time	C_{LOAD} = 100pF		4		ns
T_F	Fall time	C_{LOAD} = 100pF		2		ns

6 Function Description

6.1 Functional Block Diagram



6.2 Relay Control and Start Up

6.2.1 Relay Control

IVCC1102 is a standalone TTP PFC controller. It has start-up and relay control circuit built in. Its VRMS pin charges external RC network with a controlled current source. The current is in proportional with AC voltage after OLP and UVLO are cleared. When VRMS pin voltage is higher than 0.84V, PFC starts operation at positive AC zero crossing. RELAY turn-on signal is then issued at an AC crossover point. External delay circuit can be inserted to achieve an optimal relay contact closing timing to reduce the second inrush current. When VRMS pin voltage drops below 0.58V, Relay will open and PFC gets into standby mode. VRMS pin voltage can be programmed by changing the pin's pull-down resistance value.

6.2.2 Soft Start Up

During soft start up, VAO is clamped, so the output power is limited until VSNS crosses 2V. The soft start-up power is limited to about 10% of the full power to ensures no voltage overshoot occur at PFC output. If output load demands more power than the soft start-up power limit, the PFC cannot complete the startup.

6.3 Protection Features

6.3.1 UVLO

IVCC1102's VCC has UVLO thresholds set at 3.76V rising and 3.64V falling. When VCC rises across 3.76V, IVCC1102 begins operation. When VCC falls below 3.64V, IVCC1102 is off.

6.3.2 Open Loop Protection (OLP)

IVCC1102 monitors PFC output feedback voltage on VSNS pin. If the feedback loop is broken, VSNS is pulled to 0V by the voltage sensing resistor divider. IVCC1102 goes into standby mode when VSNS drops below 0.24V. VSNS pin can be used as a disable input by connecting to a controllable open-drain/collector transistor.

6.3.3 Over Voltage Protection (OVP)

PFC output voltage is regulated at 2V VSNS. When VSNS rises across 2.15V, IVCC1102 enters OVP mode. During OVP, all gate driver outputs GDL/GDH/SFL/SFH are turned off, and voltage loop output VAO is actively pulled low. OVP mode maintains active until VSNS returns to 2V regulation point and voltage loop starts to operate again.

6.4 Current Loop

The PFC inner control loop is a current loop. The main blocks of IVCC1102 current loop include current sense (CS) with peak current limit (PCL), and current error amplifier (CEA).

6.4.1 Current Sense (CS)

IVCC1102 uses a differential current sensing circuit with automatic gain selection. The sensing circuit is compatible with both shunt resistor sensing and Hall sensor current sensing. When a shunt resistor is connected, where CSN =0V, the differential signal is then amplified by a gain = 5.5. When a Hall current sensor is connected, the common mode voltage (connected to CSN pin) usually is the half of Hall sensor single-ended Vcc and the amplifier is bypassed. By monitoring the sensing signal's common-mode voltage, IVCC1102 is able to distinguish sensor types and determine which gain will be used.

It is recommended to set full-power peak-current sensing signal to 0.185V for shunt resistor sensing and 1V for Hall sensor sensing, so that the internal amplifier output can stay in the range of 2V +/-1V. 2V is the internal signal's center point.

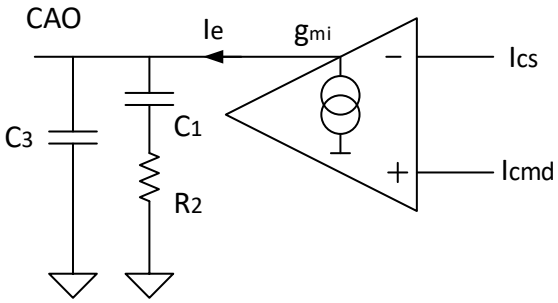
6.4.2 Peak Current Limit (PCL) and Constant Current Limit

IVCC1102 turns off GDL/GDH when the current sense amplifier output is over 1.6V. It performs cycle-by-cycle current limit. IVCC1102 has an average current limit. The current reference is clamped at 1.3V.

6.4.3 Current Error Amplifier (CEA)

IVCC1102 current error amplifier generates a current in proportional to the difference between current sense and current command. The transconductance (GMc) is equal to 50uS. The CEA output is connected to a RC

network to form a Type-2 compensator. Due to the CEA's own bandwidth limit, to maximize the current loop crossover frequency fc, the external pole capacitor C_3 may not be necessary and can be left open.



6.5 Voltage Loop

The PFC outer control loop is a voltage loop. The main blocks of IVCC1102 voltage loop include output voltage sensing with track & hold (VSNS), voltage error amplifier with dynamic response (VEA), multiplier (MP), and AC sensing with fixed-ratio feed-forward (ACFF).

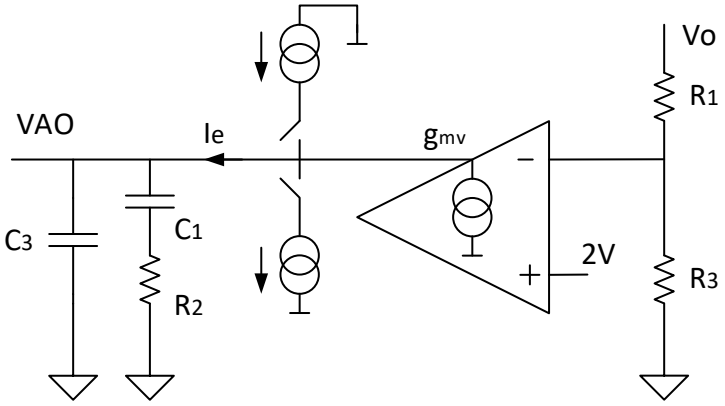
6.5.1 Output Voltage Sensing (VSNS)

IVCC1102 monitors PFC output feedback voltage on VSNS pin through resistor divider network. Resistor divider ratio is set by the desired output voltage divided by internal 2V voltage reference. A small capacitor 1nF is recommended to filter out voltage feedback noise.

To eliminate 2nd harmonica distortion, VSNS track & hold circuit is used. During steady state, VSNS voltage is sampled at AC crossover point and held unchanged for a half of AC cycle. The sensed voltage is sent to VEA for the voltage loop control. When VSNS voltage is out of ±5% Vo window, IVCC1102 enables the dynamic state and the VEA input tracks VSNS voltage directly.

6.5.2 Voltage Error Amplifier (VEA)

IVCC1102 voltage error amplifier generates a current in proportional to the difference between its input VSNS and internal 2V reference. The transconductance (GMv) is equal to 150uS within ±5% Vo steady state window. If VSNS is below 1.9V, undervoltage dynamic (UVD) adds 50uA sourcing current to VEA output. If VSNS is over 2.1V, overvoltage dynamic (OVD) adds 50uA sinking current to VEA output. The non-linear dynamic response speeds up VEA output voltage response during load transient. The VEA output is connected to a RC network to form a Type-2 compensator.



6.5.3 Multiplier (MP)

IVCC1102 multiplier generates a current command by multiplying the internally scaled AC signal and VAO from VEA output. VAO is shifted by 0.5V so that MP operates in linear region:

Highline: $MP = K_{HL} * Vac * k_{VI} * (VAO-0.5)$

Lowline: $MP = K_{LL} * Vac * k_{VI} * (VAO-0.5)$

where K_{HL} and K_{LL} are the internal gains for high line and low line, and k_{VI} is the AC amp gain set by 5kΩ AC feedback resistor divided by the external AC sensing resistor. Vac is sensed at power up and the gain K_{HL} or K_{LL} is selected and held unchanged for rest of operation, disregarding Vac voltage range changes afterward. If the input is DC, K_{HL} is then selected.

6.5.4 AC Fixed-Ratio Feed-Forward (ACFF)

IVCC1102 monitors AC input voltage through the AC sensing resistor network. The AC voltage is scaled by the gain k_{VI} and sent to the multiplier to a current command.

For CCM Boost type PFC, PWM duty cycle D_{on} is near (1 – |Vac|/ Vout). With AC Fixed-Ratio Feed-Forward (ACFF), the internal AC signal is added on top of CEA output to the PWM generator. Therefore, CEA output only provides small variation to feather the PWM duty cycle during steady state, which effectively makes current loop much fast.

6.6 PWM and Timing

6.6.1 Frequency (RT)

IVCC1102 PWM frequency is set by a resistor connected between RT pin and GND. The frequency is:

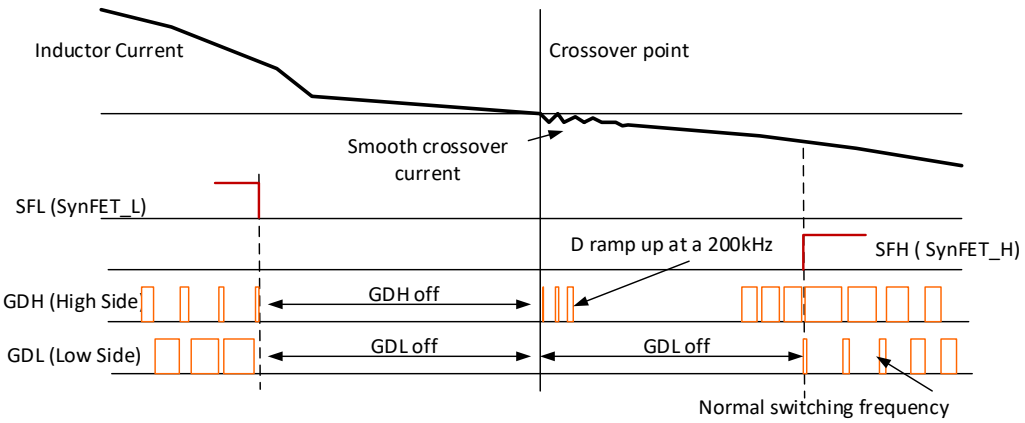
Freq (kHz) = 1800 / Rt (kΩ)

6.6.2 Deadtime (DT)

IVCC1102 has fixed deadtime and the resistor connected between RELAY and GND should be 39kΩ. It is recommended to insert 1kΩ resistor between RELAY pin and the relay's driver MOSFET.

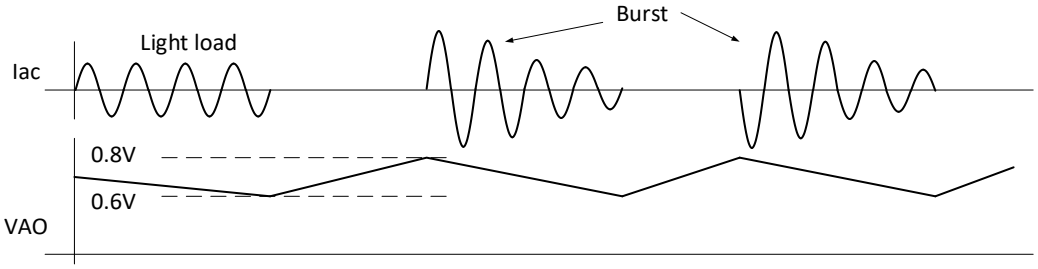
6.7 AC Zero-Crossing

IVCC1102 has AC Zero Crossing Band, in the first half of which it turns off all four gate-drive GDL/GDH/SFL/SFH outputs, and in the second half of which it resumes the switching of the active high frequency switch (SFL or SFH). Instead of starting at near full duty cycle, the active switch ramps up its duty cycle softly from zero at around 200kHz PWM frequency and reaches maximum duty cycle before the Band is expired. By doing so, the high frequency switches can swap their functions between active switch and freewheel switch smoothly. The soft ramping up of the active switch can generate a smooth inductor current to discharge the low frequency bridge phase node capacitor and minimize or eliminate AC crossover current spike. The low frequency synchronous switches are usually super-junction MOSFETs, whose Coss can store significant energy to cause a large AC crossover current spike. The Band is a ±100us zero-crossing window. It prevents potential short circuit when AC sensing signal is near 0V and noisy.



6.8 Burst Mode

At light load, voltage loop output VAO voltage, which is proportional to power command, is low. Gate driver outputs are disabled when VAO drops below 0.6V. Without gate drive signals, PFC output voltage declines, at the meantime VAO increases. When VAO rises above 0.8V, gate drive outputs resume at AC zero crossover points. PFC converter works in burst mode that begins at AC zero crossing as long as PFC output voltage is within ±5% of regulation voltage. It results in less harmonic distortion and a better light load efficiency. The burst mode's entering power and exiting power are around 5% and 10% of rated power respectively. Note the controllers have inherent power derating control. Rated power varies with its input AC voltage. The rated power is directly proportional to the input AC voltage. At light loads, load stepping can cause VAO to decline more rapidly, which could result in entering burst mode at a higher power level. It is a normal phenomenon.



6.9 Bootstrap supporting PWM

Most totem-pole PFCs are used in high density design. Bootstrap is always the first choice for density and cost reasons. However, during burst mode operation, the two high frequency switches stop switching for some period of time, which could cause the high side driver to lose power. IVCC1102 features a bootstrap supporting PWM control to solve this problem, by maintaining the bottom-side switch soft-ramping PWM at AC crossover always.

6.10 Gate Drive Outputs

IVCC1102 generates 2 gate drive signals, GDH and GDL, for high-speed bridge high side and low side switches. It also generates 2 gate drive signals, SFH and SFL, for low-speed bridge high side and low side switches. Each gate drive operates 5V rail to rail with above 100mA peak current driving capability.

7 Typical Characteristics

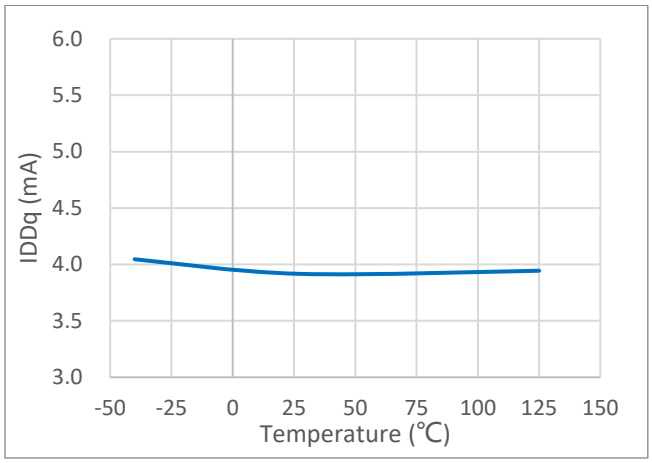


Figure 1. Quiescent Current IDDq vs Temperature

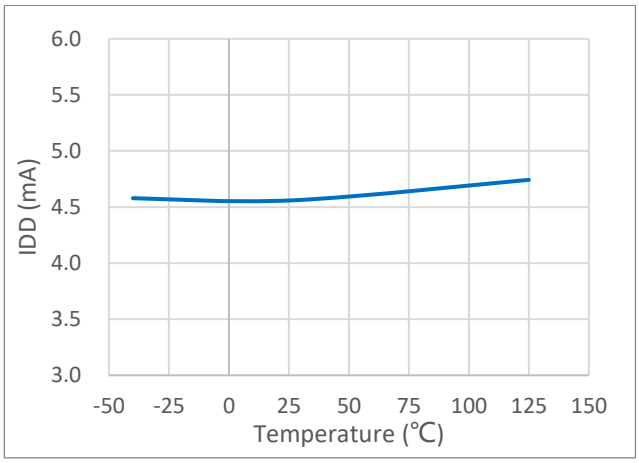


Figure 2. Operating Current IDD vs Temperature

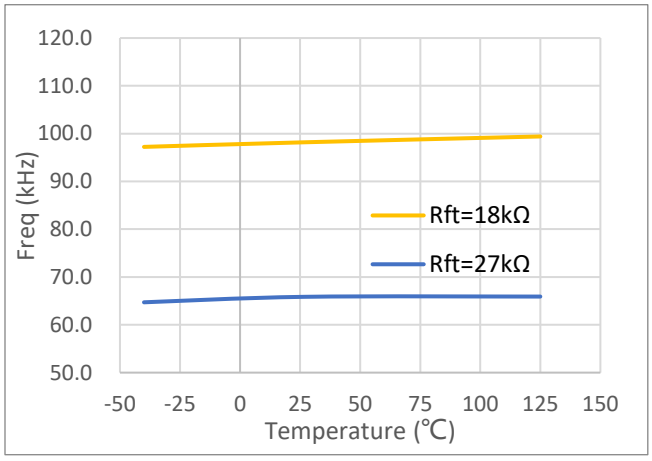


Figure 3. Freq vs Temperature

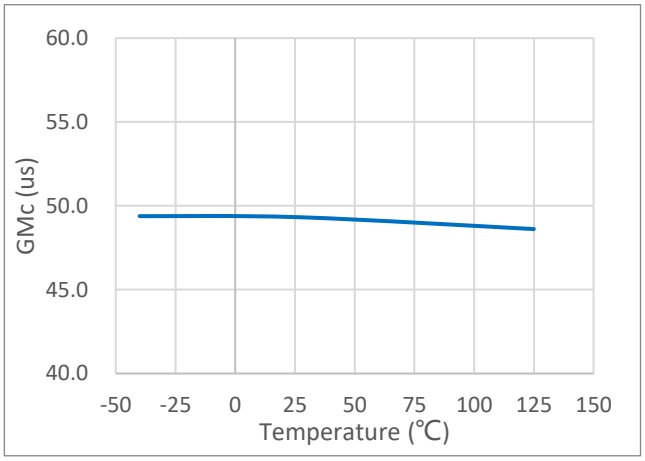


Figure 4. GMc vs Temperature

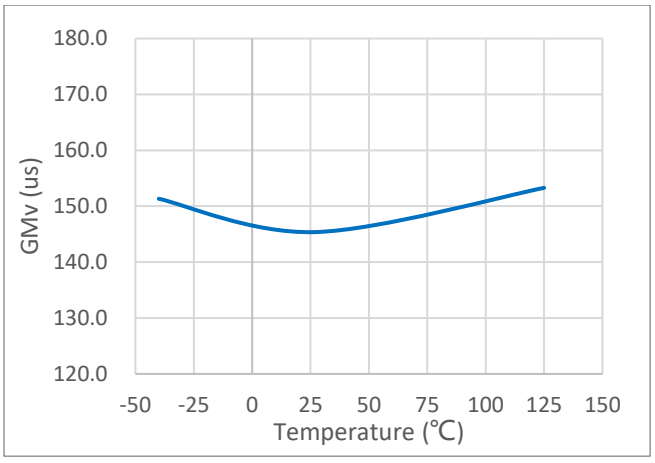


Figure 5. GMv vs Temperature

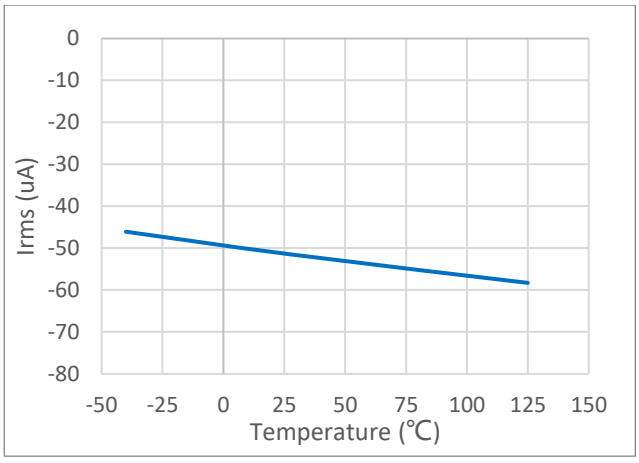
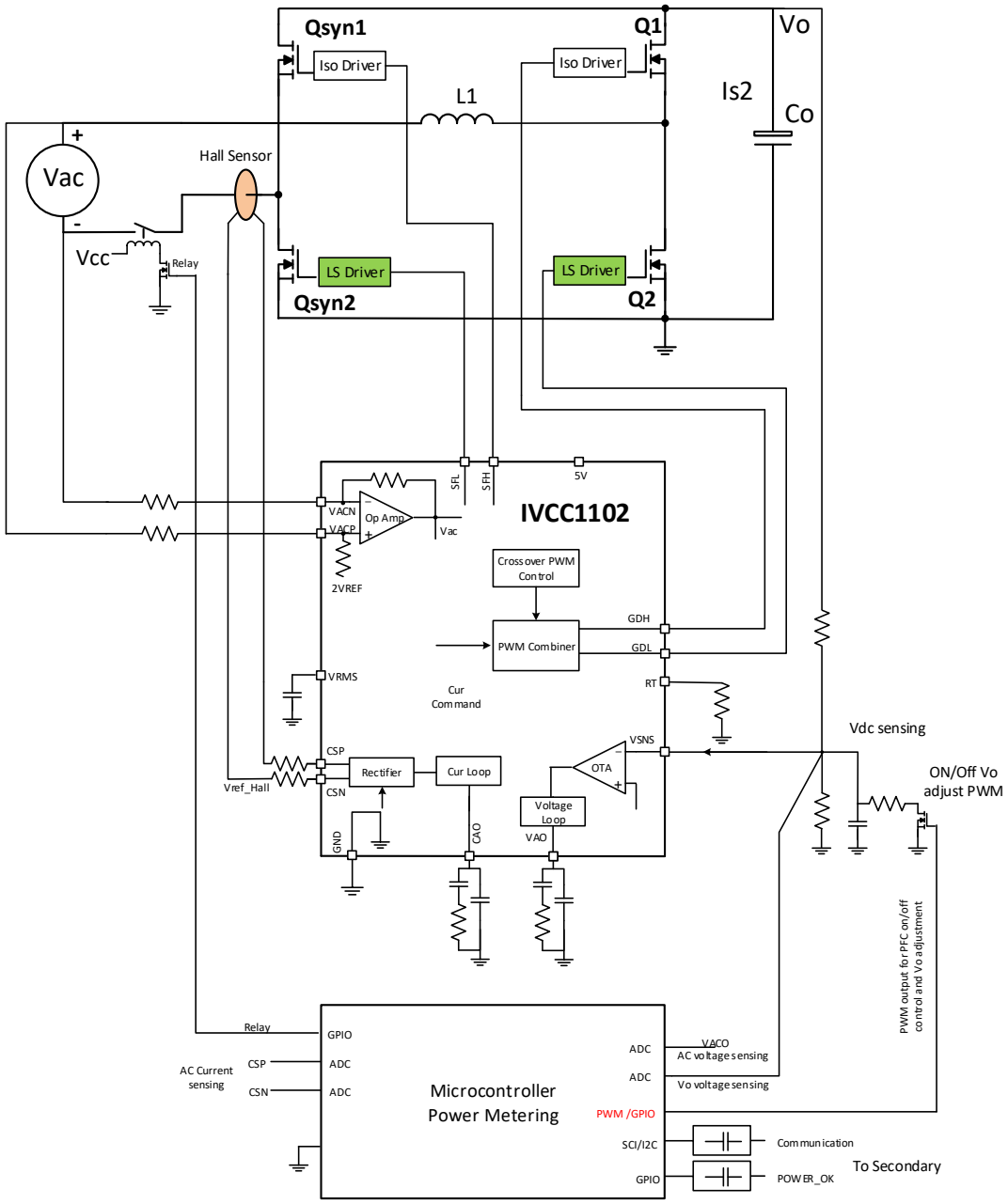


Figure 6. Irms vs Temperature

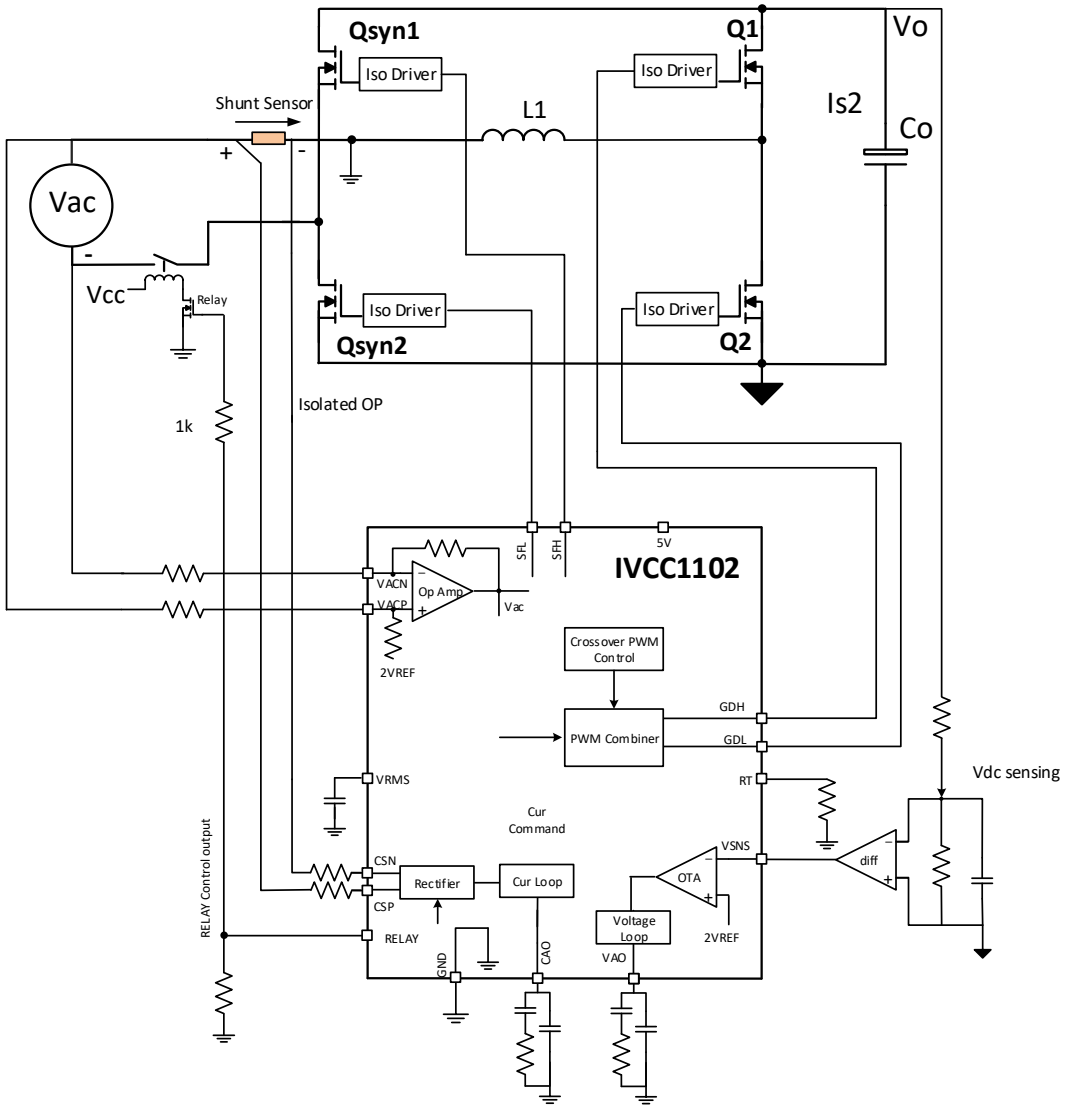
8 Application Implementation

8.1 Typical Applications

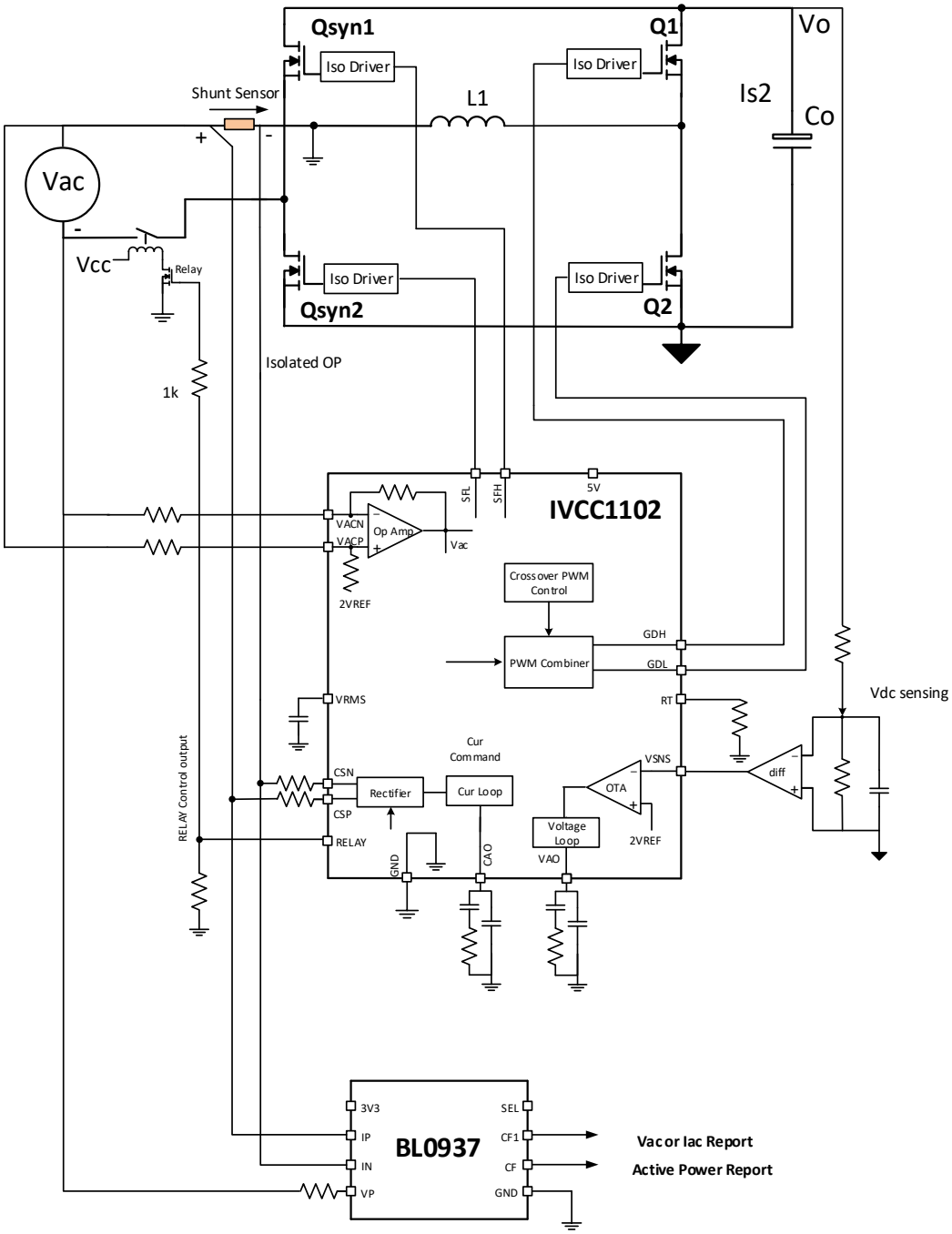
One typical application is to use an IVCC1102 with a Hall current sensor and a micro controller (or power metering circuit). All control circuit is referenced to power ground. The combination of IVCC1102 and an external micro-controller gives an easy and fast way to develop a totem-pole PFC converter and to achieve a superior performance. It also gives maximum flexibility for engineers to choose a micro-controller for their solutions.



Another application is to use IVCC1102 for low cost and compact control. All control circuit is referenced to the low frequency input line, where a shunt current sensing resistor is connected. IVCC1102 has an internal amplifier to gain up the current sensing signal for current loop control and over current protection. The controller provides a control signal for relay on/off control. Note for IVCC1102, RELAY pin is used for deadtime setting. To prevent the gate capacitance of the relay's driving MOSFET impacting on deadtime setting, an 1k resistor is recommended to inserted between RELAY pin and the relay driving MOSFET. Since the control circuit's ground is switching at line frequency, a differential amplifier is needed to sense PFC output voltage. All MOSFETs need to be driven by isolated gate drivers.



More and more server and telecom power supplies require high efficiency, low THD and input power reporting. The combination of IVCC1102 and power meter ICs is able to achieve a low cost and high-performance solution, which aims to replace a high-end DSP directly. The solution doesn't require any firmware programming and reduces development time substantially. The analog-based solution provides fast and precise totem-pole PFC control and has better noise immunity. By selecting a dedicated power meter IC, measurement with a better than 1% accuracy can be achieved without any calibration.


Qsyn1
Q1
Vo
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Iso Driver
Shunt Sensor
L1
Is2
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Vac
-
Vcc
Relay
Iso Driver
Iso Driver
Qsyn2
Q2
Isolated OP
1k
5V
SFL
SFH
IVCC1102
VACN
VACP
Op Amp
Vac
2VREF
Crossover PWM Control
PWM Combiner
GDH
GDL
Vdc sensing
VRMS
RT
Cur Command
VSNS
CSN
Rectifier
Cur Loop
OTA
diff
CSP
Voltage Loop
2VREF
RELAY Control output
RELAY
GND
CAO
VAO
3V3
IP
IN
VP
BL0937
SEL
CF1
CF
GND
Vac or Iac Report
Active Power Report

8.2 Design Calculation Example (2.5kW Totem-Pole PFC Reference Design)

8.2.1 PFC Specifications

Input Voltage Range	85Vrms – 265Vrms
Output Power at 240Vac	2.5kW
Output Power at 120Vac	1.25kW
PFC Output Voltage	400V
Switching Frequency	65kHz
Startup Input Voltage	82Vrms

8.2.2 Circuit Parameter Selection

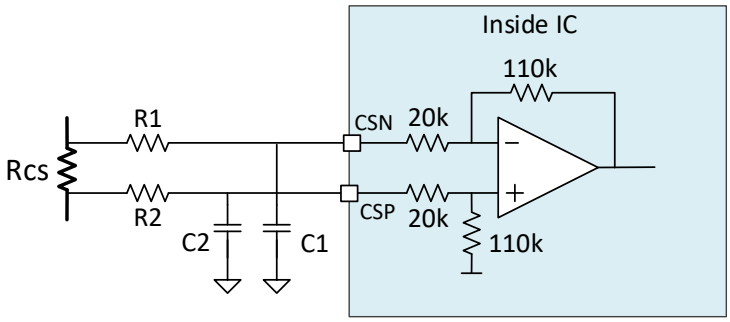
The circuit parameters are calculated, based on the following assumptions:

1. Converter efficiency η=98% at 120Vac and 1.25kW output power;
2. Cycle-by-cycle current limit = 160% of peak AC average current (current ripple not included)。

Since the internal cycle-by-cycle current limit threshold V_cbc = 1.6V, the peak average current = 1.6V / 160% = 1.0V, which is within the recommended signal range for steady state operation.

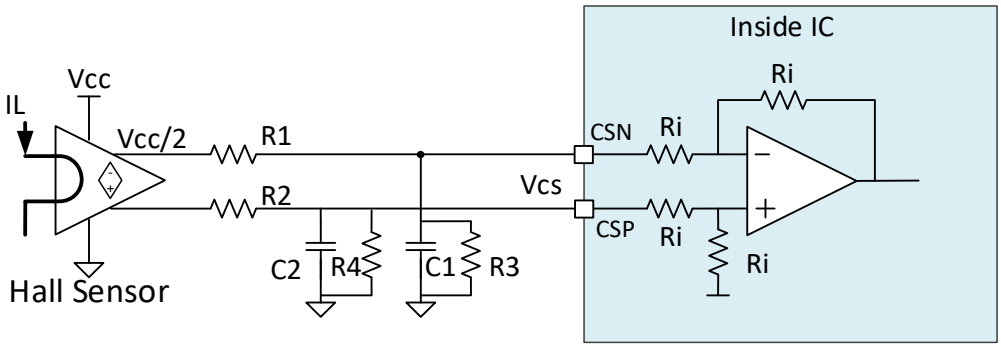
The peak average current = 1.414 x 1250W/(120Vrms x η) = 15.03A.

1) If a shunt resistor is used for current sensing
To maintain 1.0V peak average current signal range after the internal amplifier (gain = 5.5),
The shunt resistor value should be,
Rcs ≤ 1.0V / (5.5 x 15.03A) = 0.0121 Ω, Choose Rcs = 12mΩ
Small filters (R1/C1 and R2/C2) with crossover frequency fc = 65kHz – 165kHz (e.g. R = 1k and C = 1nF) can be used to reduce switching and circuit noise. Note the filter resistance can affect the current amplifier gain and it should not be selected larger than 1kOhm. A heavy filter with *f*c much lower than switching frequency could impair cycle-by-cycle current limit accuracy.



2) If a hall sensor, e.g ACS724llctr-30ab-t , is used, whose current sensitivity is 66mV/A.
At 15.03A current, the hall sensor output,
Vcs = 0.066V/A x 15.03A = 0.992V,
which is within 1.0V peak average current signal range, and no additional resistor divider is needed.

In case that Vcs is beyond 1.0V range, an external voltage divider will be necessary to scale Vcs down. To ensure Vcs is zero voltage at zero current, R1/R3 = R2/R4 should be maintained. When the hall sensor's reference voltage, which is usually Vcc/2, is detected higher than 0.8V at CSN pin, the controller sets the internal amplifier gain to 1 and input impedance to high resistance (> 1Mohm). In this case, external filters' resistance selection would not impact the amplifier's gain.



8.2.3 Control Loops

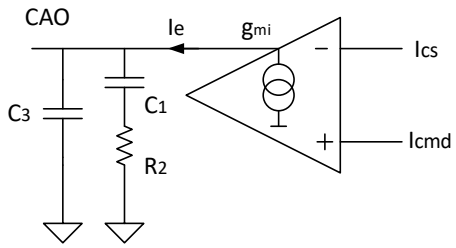
IVCC1102 have an inner current loop and an outer voltage loop. Since totem-pole PFCs with synchronous rectification MOSFETs are essentially bidirectional converters, a traditional current loop would not be fast enough to reduce current command instantaneously when AC input drops to zero abruptly. Such an event can cause a large reversed current, which discharges the PFC's output capacitor energy necessary for hold-up time and could even damage the MOSFETs. To solve this problem, the controller utilizes AC Fixed-Ratio Feed-Forward (ACFF) to dominate the duty cycle control, where D' = |Vac|/Vo. The active switch's duty cycle can then follow VAC voltage's change with no delay and completely prevent the inductor current from reversing. Since the PWM duty cycle follows Vac and the current loop merely feathers the duty cycle, the effective small-signal bandwidth is increased and results in an excellent current waveform and low THD. Due to this same reason, the controller is very suitable for high AC frequency PFC applications, such as 400Hz aviation power supply design.

PFC Vo sensing with a second-order harmonic component is the main contributor to the AC current waveform distortion. To accurately sensing Vo average voltage, a sample-hold circuit is added to sense the Vo voltage at AC crossover point, where the value is right the average output voltage. The sensing scheme fully rejects the second harmonic component. The sample-hold sensing scheme, however, introduce a half AC cycle's time delay and slow down the voltage loop. To alleviate this issue and achieve an excellent step-load response, a non-linear voltage is used to accelerate the loop when the output voltage error excesses 5% of the set point.

IVCC1102 has been optimized for ACFF control. When Vac sensing scale K_{VI} and Vo sensing scale K_{VO} are equal, the current loop stays at its minimum output adjustment and achieves optimal loop performance.

Totem-pole PFC is essentially composed of two traditional PFCs in terms of circuit operation, one of which operates at positive AC cycles and the other at negative AC cycles. Therefore, totem-pole PFCs and traditional PFCs are of the same transfer functions.

The current loop uses OTA (current source) type-II compensator, and its transfer functions is



$$Hi(s) = -gmi\frac{1+R2\cdot C1\cdot S}{(C1+C3)S+R2\cdot C1\cdot C3\cdot S^2} \quad \text{or}$$

$$Hi(s) = -Go\frac{1+\omega z/s}{1+s/\omega p}$$

where,

$$Go = \frac{gmi\cdot R2\cdot C1}{C1+C3}$$

For most time C3 is very small or not needed, then

$$Go = gmi\cdot R2$$

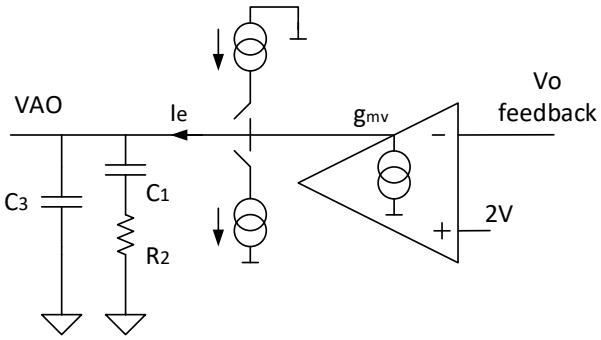
$$fz = \frac{1}{2\pi\cdot R2\cdot C1}$$

$$fp = \frac{C1+C3}{2\pi\cdot R2\cdot C1\cdot C3}$$

Recommended components values for current loop compensation are:

$$Ri2 = 60.4k\Omega,\quad Ci1 = 4.7nF,\quad Ci3 = 22pF$$

The voltage loop uses OTA (current source) type-II compensator, similar as the current loop, and its transfer function is,



$$Hv(s) = -gmv\frac{1+R2\cdot C1\cdot S}{(C1+C3)S+R2\cdot C1\cdot C3\cdot S^2} \quad \text{or}$$

$$Hv(s) = -Go\frac{1+\omega z/s}{1+s/\omega p}$$

where,

$$Go = \frac{gmv \cdot R2 \cdot C1}{C1+C3}$$

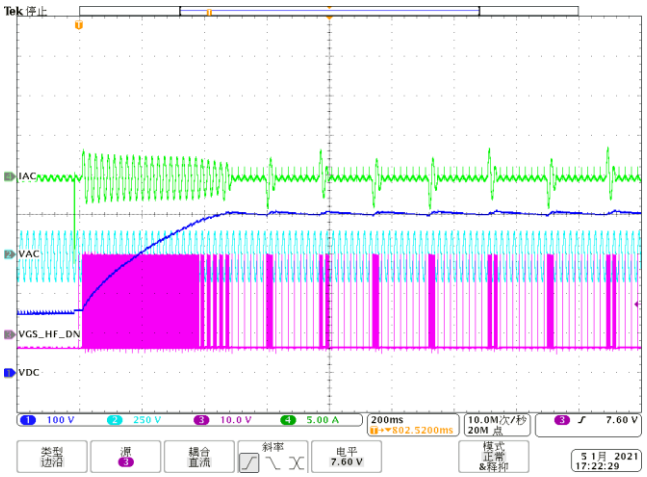
$$fz = \frac{1}{2\pi \cdot R2 \cdot C1}$$

$$fp = \frac{C1+C3}{2\pi \cdot R2 \cdot C1 \cdot C3}$$

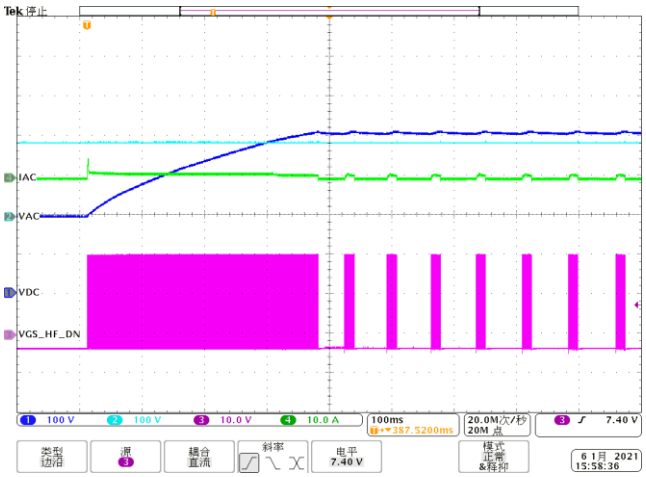
Recommended components values for voltage loop compensation are:

$$Rv2 = 60.4k\Omega,\quad Cv1 = 0.47uF,\quad Cv3 = 22nF$$

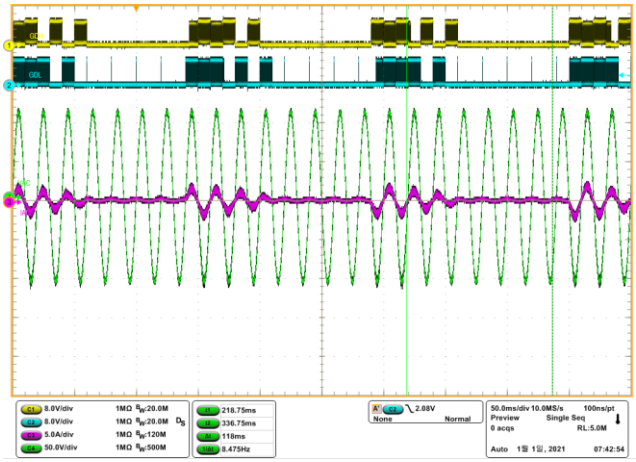
8.3 2.5kW Reference Design Waveforms



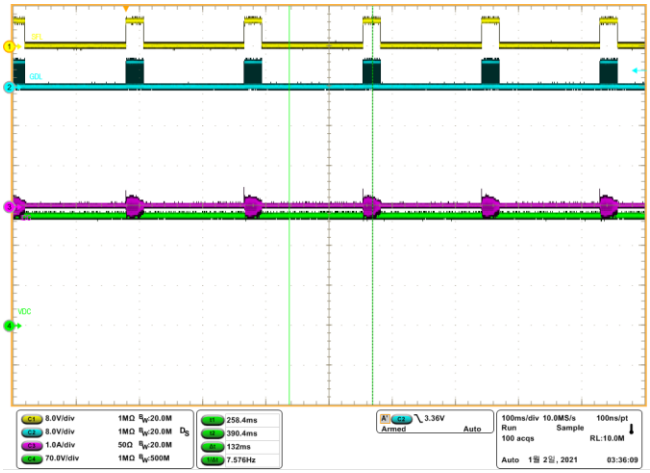
Startup Waveforms with AC input



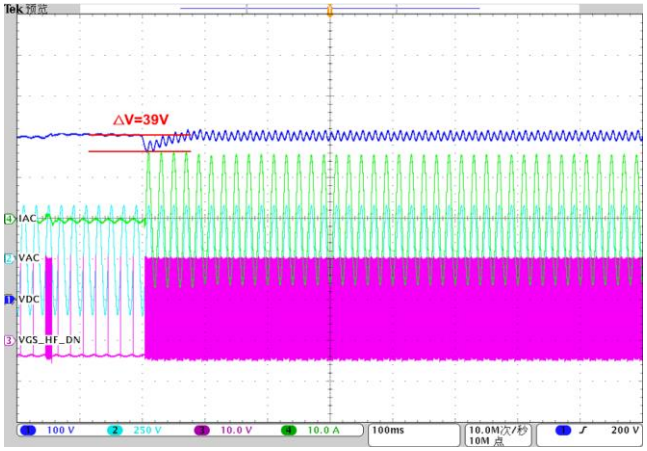
Startup Waveforms with DC input



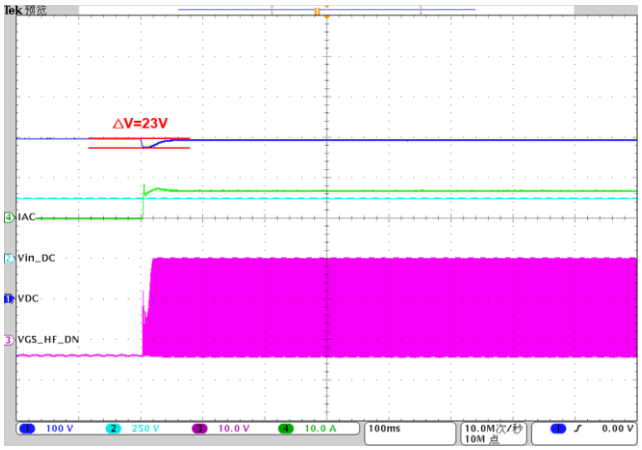
Light Load Burst with AC Input



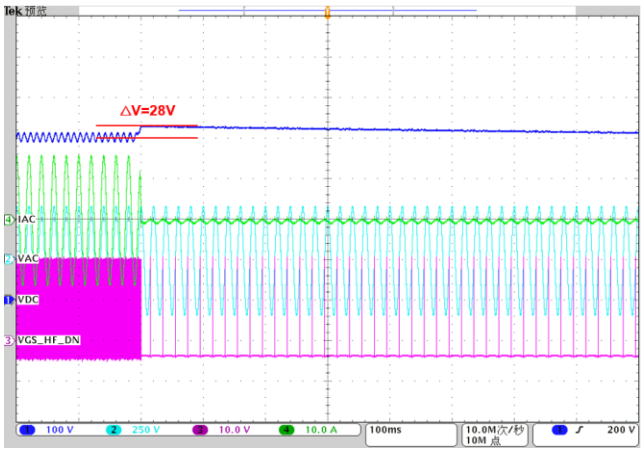
Light Load Burst with DC Input



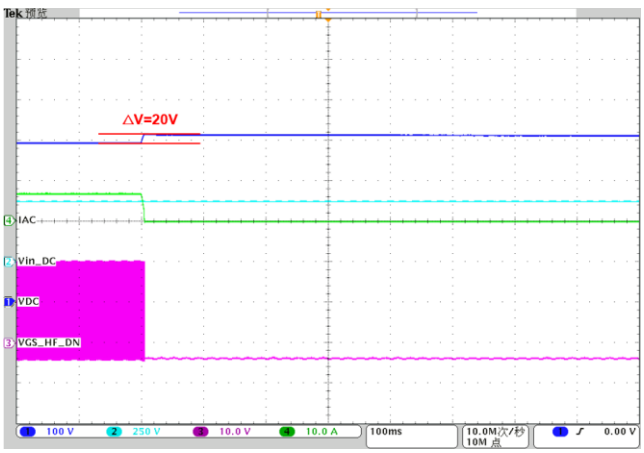
2.5kW Step Load Up with AC Input



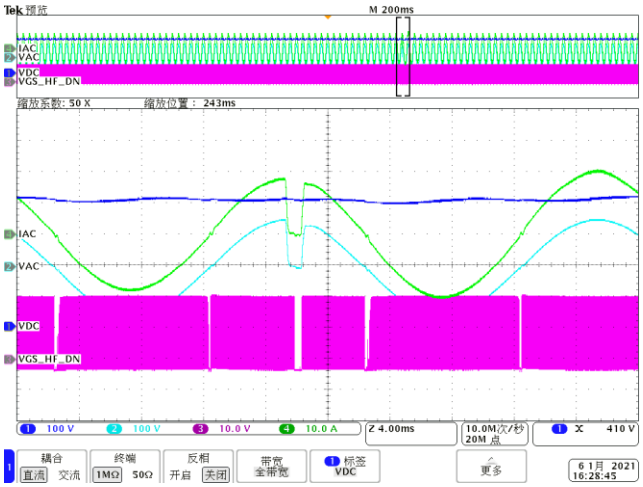
2.5kW Step Load Up with DC Input



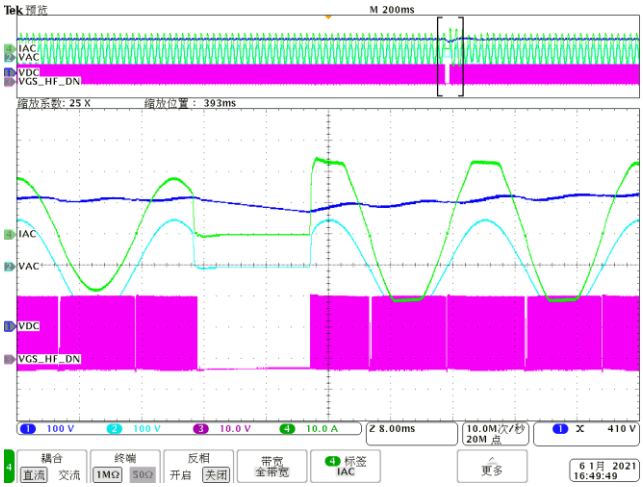
2.5kW Step Load Down with AC Input



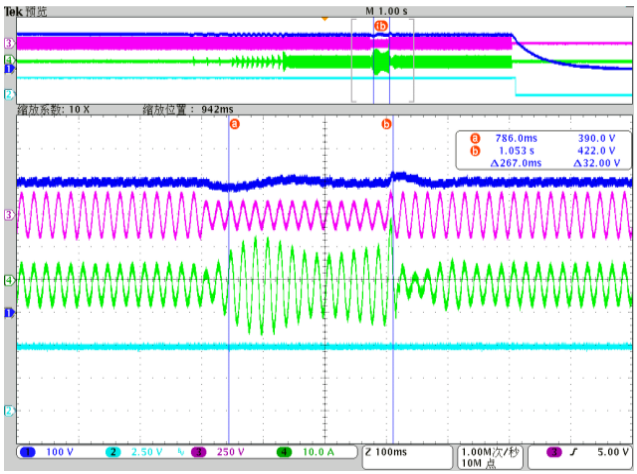
2.5kW Step Load Down with DC Input



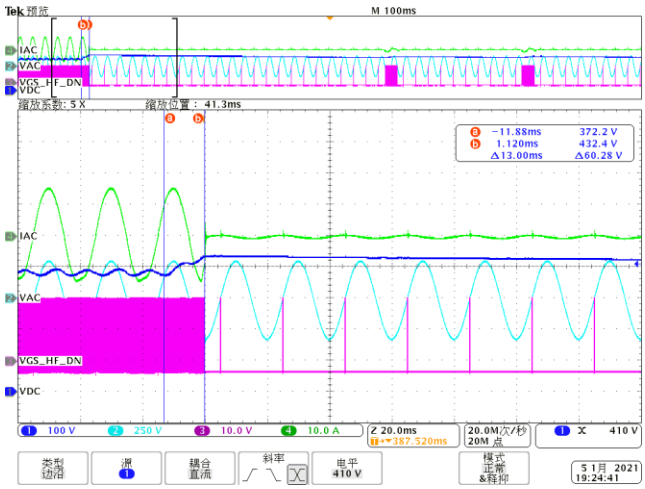
1ms AC Input Drop



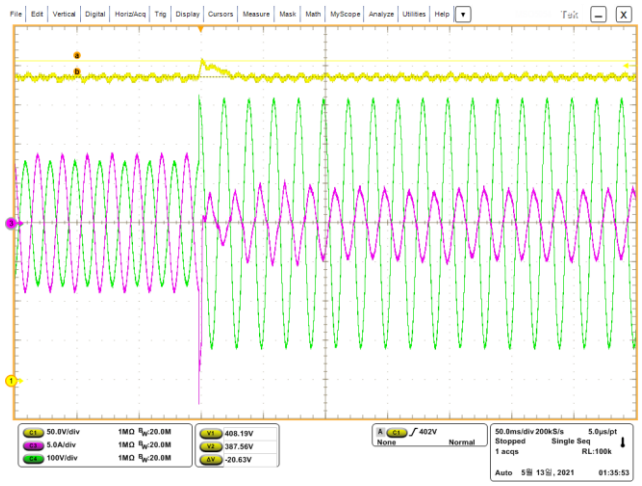
15ms AC Input Drop



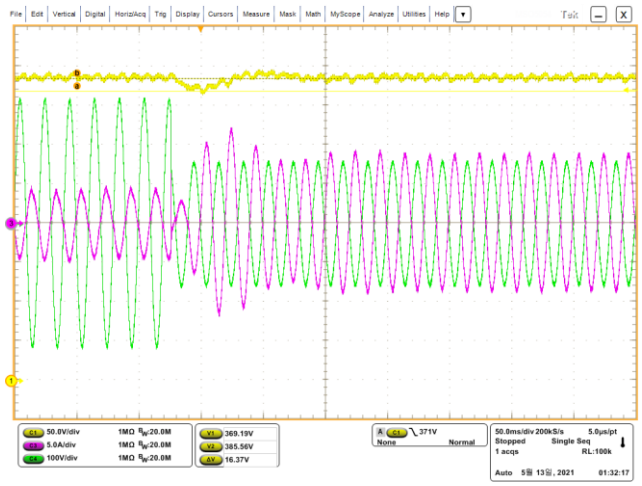
110Vac to 62Vac Sag



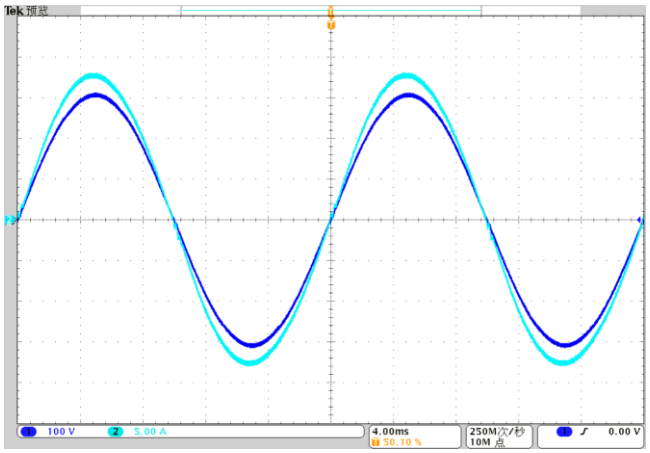
GDL (VGS_HF_DN) Waveform at Burst



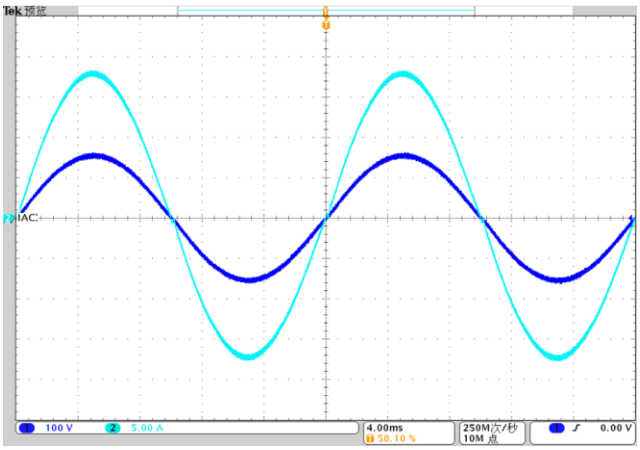
110Vac to 220Vac Step Jump (Bust mode off)



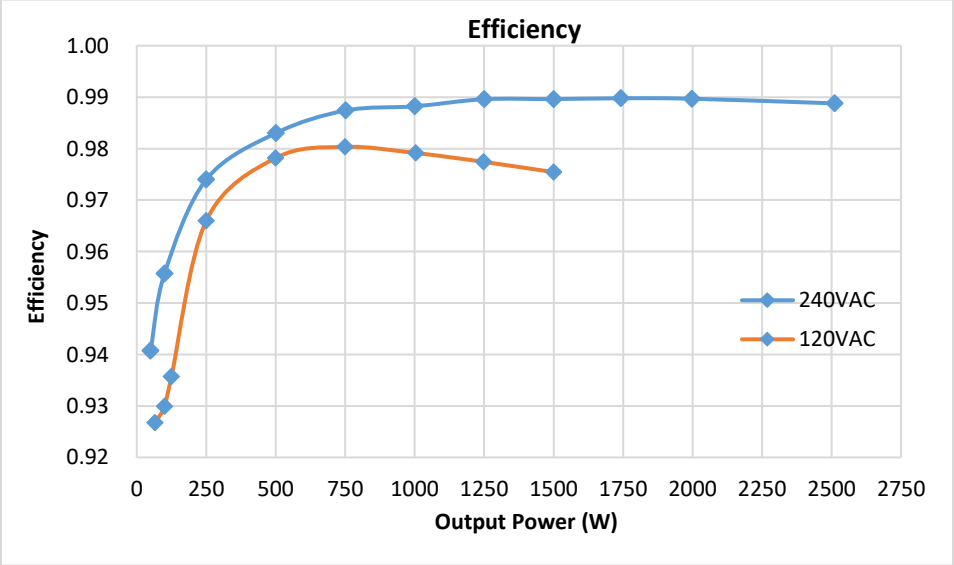
220Vac to 110Vac Drop (Bust mode off)



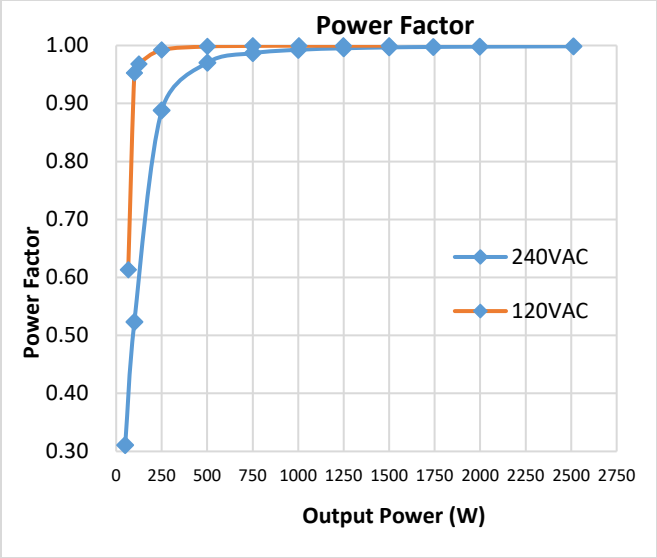
2.5kW AC Voltage and Current at High Line



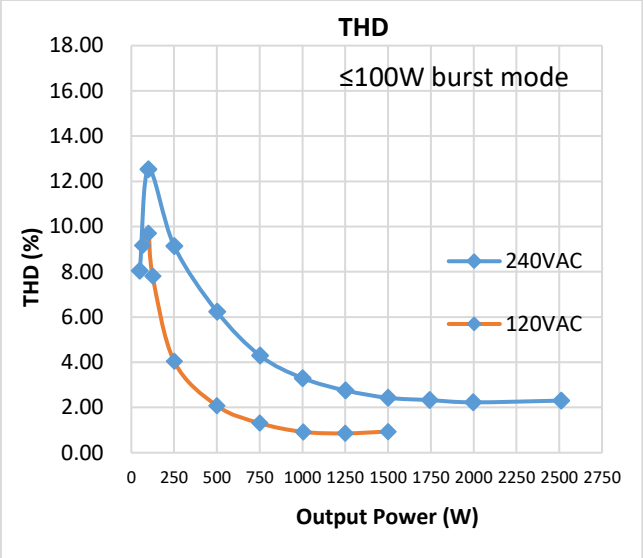
1 kW AC Voltage and Current at Low Line



Efficiency



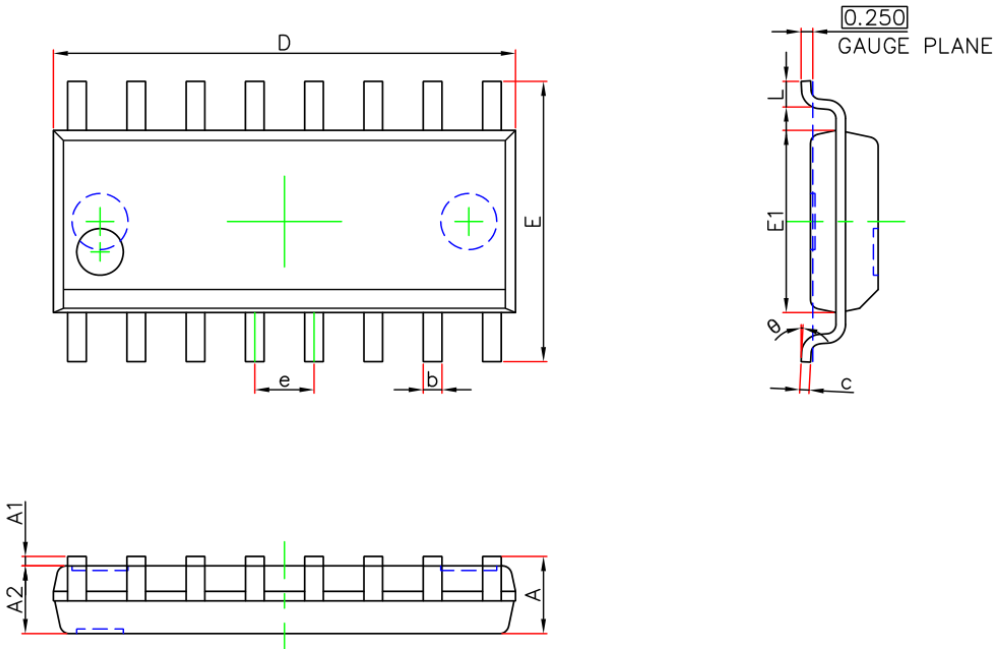
Power Factor



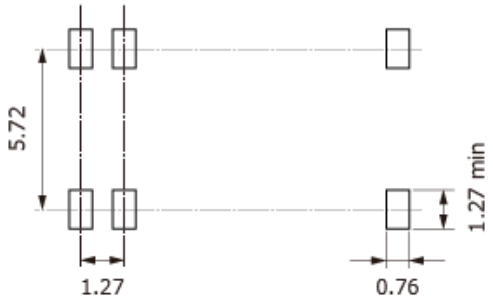
THD

9 Package Information

SOIC-16 Package Dimensions

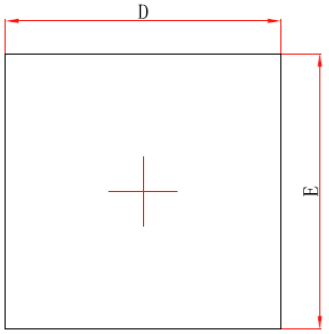


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.750	——	0.069
A1	0.150	0.250	0.006	0.010
A2	1.400	1.500	0.055	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.000	0.386	0.394
e	1.270(BSC)		0.050(BSC)	
E	5.900	6.100	0.232	0.240
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

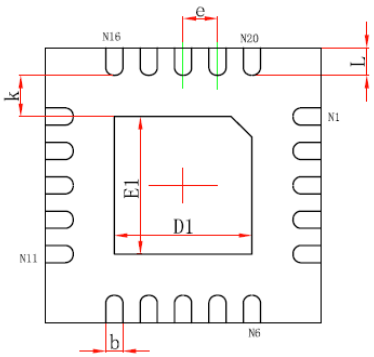


SOIC-16 PCB Layout Footprint

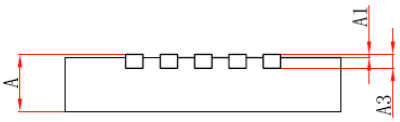
QFN 4x4 20L Package Dimensions



Top View

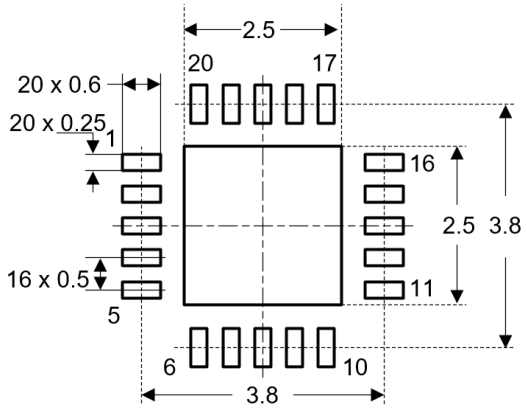


Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	1.900	2.100	0.075	0.083
E1	1.900	2.100	0.075	0.083
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019



QFN 4x4 20L PCB Layout Footprint