MP44010

Boundary Mode PFC Controller

The Future of Analog IC Technology

DESCRIPTION

The MP44010 is a boundary conduction mode PFC controller which can provide simple and high performance active power factor correction using minimum external components.

The output voltage is accurately regulated by a high performance voltage mode amplifier with an accurate internal voltage reference.

The precise adjustable output over-voltage protection greatly enhances the system reliability.

The on-chip R/C filter on the current sense pin can eliminate the external R/C filter.

The extremely low start-up current, quiescent current and the disable function can reduce the power consumption and result in excellent efficiency performance.

The MP44010 is available in SOIC-8 package.

FEATURES

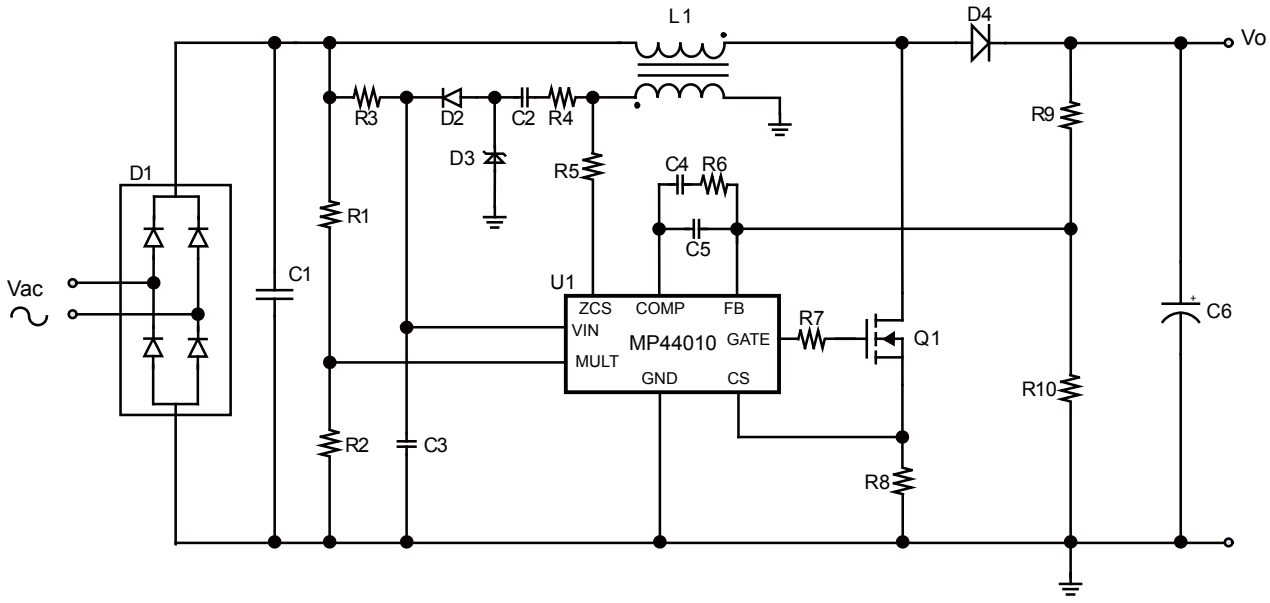
- Boundary Conduction Mode PFC Controller for Pre-regulator
- Zero-crossing Compensation to Minimum THD of AC Input Current
- Precise Adjustable Output Over-voltage Protection
- Ultra-low (15μA) Start-up Current.
- Low (0.46mA) Quiescent Current
- On-chip Filter on Current Sense Pin
- Disable Function
- -800/+1150mA Peak Gate Drive Current
- Available in SOIC-8 Package

APPLICATIONS

- Offline Adaptor
- Electronic Ballast
- LLC Front End
- Other PFC Pre-regulators

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Other Patents Pending.

TYPICAL APPLICATION



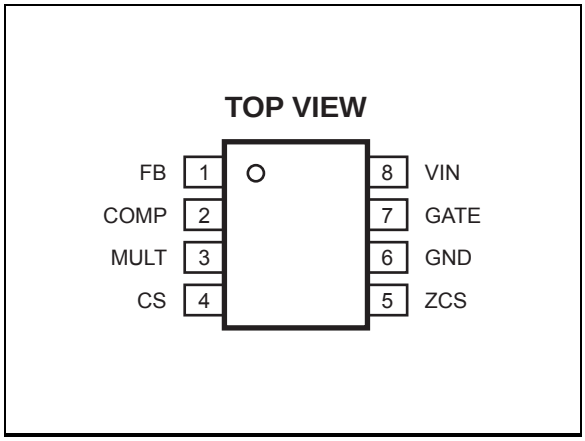
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ORDERING INFORMATION

Part Number	Package	Top Marking
MP44010HS*	SOIC-8	MP44010

* For Tape & Reel, add suffix –Z (e.g. MP44010HS–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP44010HS–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} ..... -0.5V to Self Limit
ZCS pin ..... -0.3V to Self Limit
Other Analog Inputs and Outputs ..-0.3V to 6.5V
ZCS Max. current.....-2.5mA to 10mA
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC-8 ..... 1.4W
Junction Temperature…… …..150°C
Lead Temperature (Solder).....260°C
Storage Temperature..... -55°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 13.4V to 22V
Analog inputs and outputs .....-0.3V to 6.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8 .....90 ..... 45 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, T_A = T_J = -40°C to +125°C, unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Operating Range	V_{IN}	After turn on	10.7		22	V
Turn On Threshold	V_{IN_on}		11	12.4	13.5	V
Turn Off Threshold	V_{IN_off}		8.7	9.8	10.7	V
Hysteresis	V_{IN_hys}		2.1		3	V
Zener Voltage	V_z	I_{IN}=20mA	22	25	28	V
Supply Current						
Start-up Current	$I_{startup}$	V_{IN}=11V		15	40	μA
Quiescent Current	I_q	No switch		0.46	0.65	mA
Quiescent Current	I_q	During OVP(either static or dymanic) or V_{IN}≤150mV		0.42		mA
Operating Current	I_{cc}	F_s =70kHz, C_{LOAD}=1nF		1.6	2.5	mA
Multiplier						
Input Bias Current	I_{MULT}				-1	μA
Linear Operation Range	V_{MULT}		0 to 3			V
Output Max. Slope	$\Delta V_{CS}/\Delta V_{MULT}$	V_{MULT}=0 to 1V , V_{COMP}=upper clamp, T_J = 25°C	1.5	1.73		V/V
Gain[5]	K	V_{MULT}=1V, V_{COMP}=4V	0.45	0.64	0.8	1/V
Error Amplifier						
Feedback Voltage	V_{FB}	T_J = 25°C	2.465	2.5	2.535	V
		V_{IN} =10.7V to 22V T_J = -40°C to +125°C	2.44		2.56	
Feedback Voltage Line Regulation	V_{FB_LR}	V_{IN} =10.7V to 22V		2	5	mV
Feedback Bias Current	I_{FB}				0.2	μA
Open Loop Voltage Gain	G_V		60	80		dB
Gain-Bandwidth Product	GB			1		MHz
Source Current	I_{COMP_source}		-5.5	-3	-1	mA
Sink Current	I_{COMP_sink}		2.5	5.5		mA
Upper Clamp Voltage	V_{COMP_H}		5.3	6	6.6	V
Lower Clamp Voltage	V_{COMP_L}		1.8	2.1	2.3	V
Current Sense Comparator						
Input Bias Current	I_{CS}				-1	μA
Delay	T_{DT}			300	450	ns
Current Sense Clamp Voltage	V_{CS_Clamp}		1.58	1.72	1.83	V
Current Sense Offset	V_{CS_Offset}	V_{MULT}=0V		30		mV
		V_{MULT}=2.5V		5		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 15V, T_A = T_J =-40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Zero Current Sensor						
Upper Clamp Voltage	$V_{ZCSclamp_H}$	I_{ZCS}=2.5mA	7.2	7.8	8.35	V
Lower Clamp Voltage	$V_{ZCSclamp_L}$	I_{ZCS}=-1.8mA	0.3	0.55	0.8	V
Zero Current Sensing Threshold	V_{ZCS_H}	V_{ZCS} rising		2.1	2.5	V
	V_{ZCS_L}	V_{ZCS} falling	0.9	1.35		V
ZCS_EN Threshold	$V_{ZCS_EN_R}$	V_{ZCS} rising		310		mV
ZCS_EN Hysteresis	$V_{ZCS_EN_hys}$			120		mV
Source Current Capability	I_{ZCS_source}			4		mA
Restart Current After Disable	I_{ZCS_res}		57	85		µA
Re-Starter						
Re-Start Time	T_{start}		80	175	280	µs
Over-Voltage						
Dynamic OVP Current	I_{OVP}		29	39	49	µA
Hysteresis	I_{OVP_Hys}			30		µA
Static OVP Threshold	V_{OVP}		1.85	2.15	2.35	V
Gate Driver						
Dropout Voltage	V_{OH}	$I_{GDsource}$=20mA		2.4	3.1	V
		$I_{GDsource}$=200mA		3.9	4.5	V
	V_{OL}	I_{GDsink}=200mA		0.5	1.5	V
Voltage Fall Time	T_f			30	70	ns
Voltage Rise Time	T_r			40	80	ns
Max Output Drive Voltage	V_{D_max}		12	13.5	14	V
Source Current Capability	I_{Gate_source}			-800		mA
Sink Current Capability	I_{Gate_sink}			1150		mA
UVLO Saturation Voltage	$V_{Saturation}$	V_{IN}=0 to V_{IN_ON}, I_{Gate_sink}=10mA			0.3	V

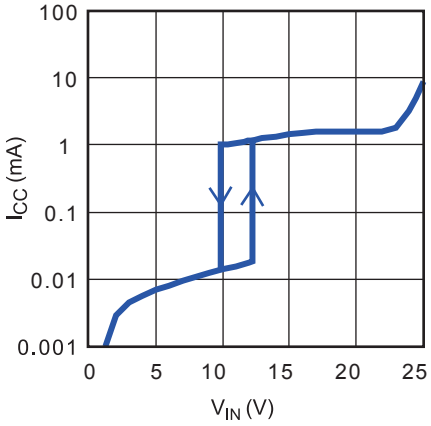
Note:

5) The multiplier Gain is calculated by: $K=V_{cs}/(V_{MUTL}\cdot(V_{COMP}-2.5))$

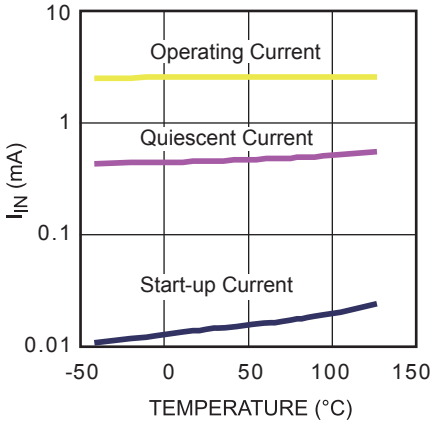
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TYPICAL PERFORMANCE CHARACTERISTICS

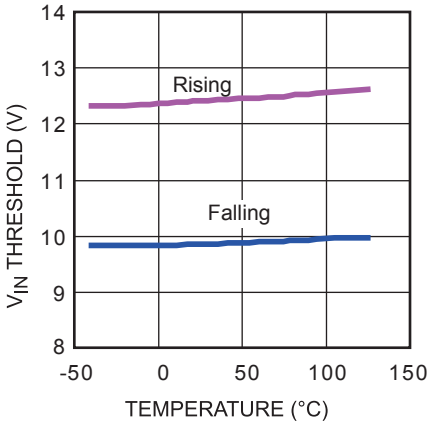
Supply Current vs. Supply Voltage



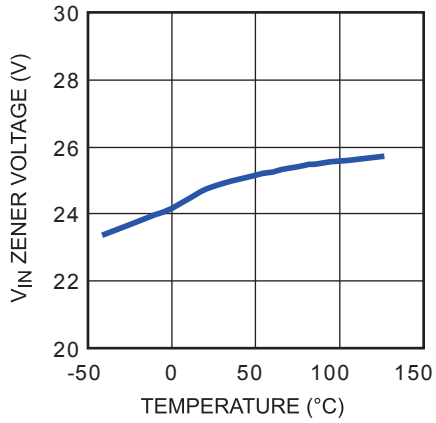
Supply Current vs. T_J



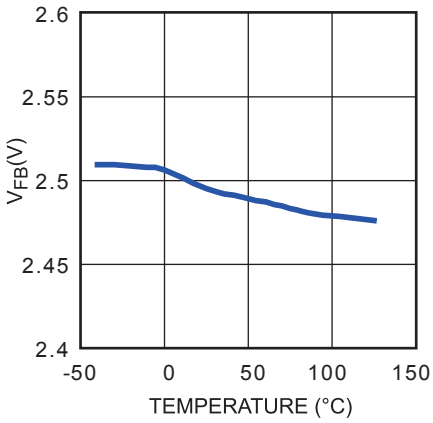
Start-up & UVLO vs. T_J



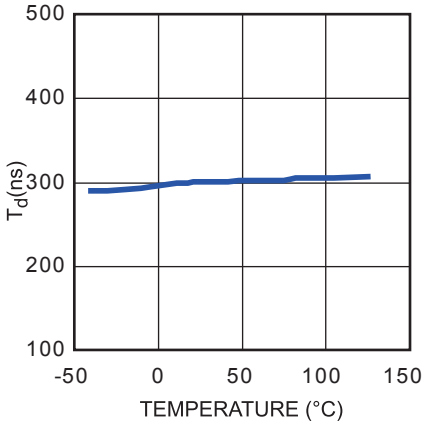
V_{IN} Zener Voltage vs. T_J



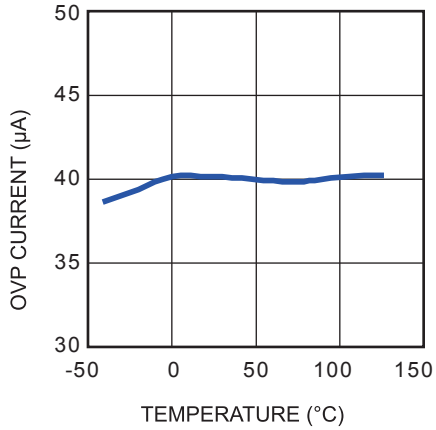
Feedback Reference vs. T_J



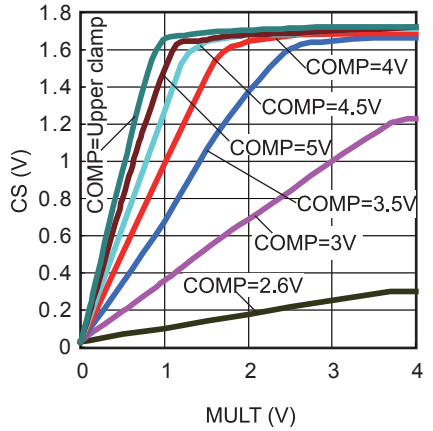
Delay-to-output vs. T_J



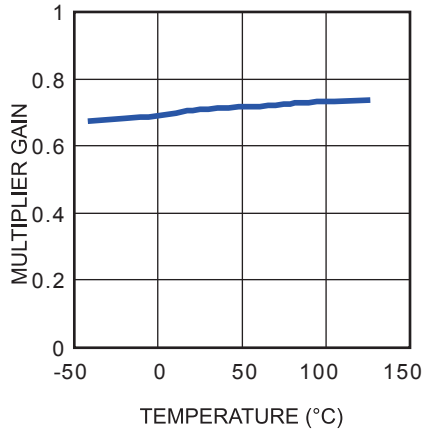
OVP Current vs. T_J



Multiplier Characteristic



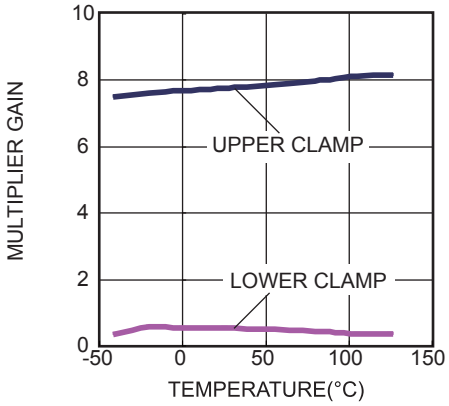
Multiplier Gain vs. T_J



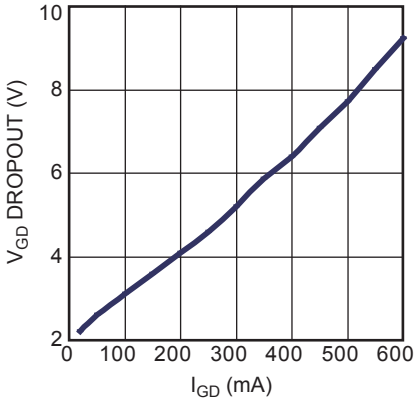
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TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

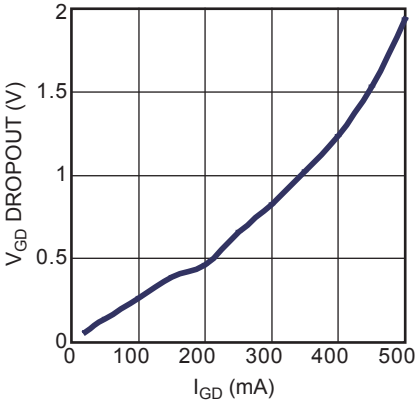
ZCS Clamp Levels vs. T_J



Gate-Drive Output High Saturation



Gate-Drive Output Low Saturation

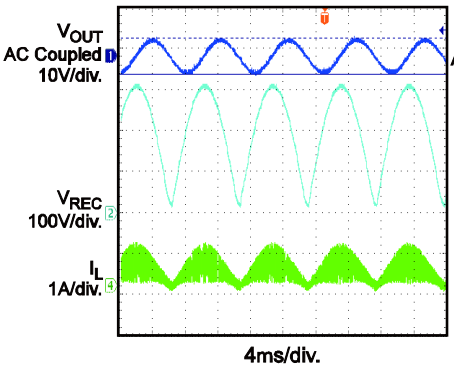


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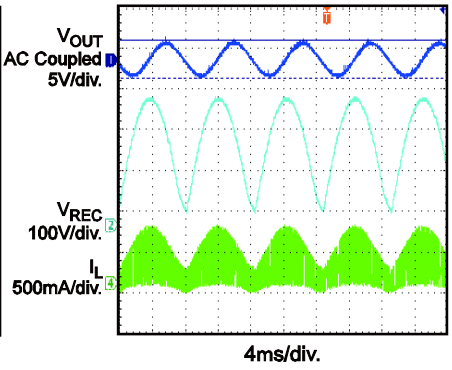
TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

Performance waveforms are generated using the evaluation board built with design example on page 11. V_{AC}=220V, V_{OUT}=400V, P_{OUT}=100W, T_A=25°C, unless otherwise noted.

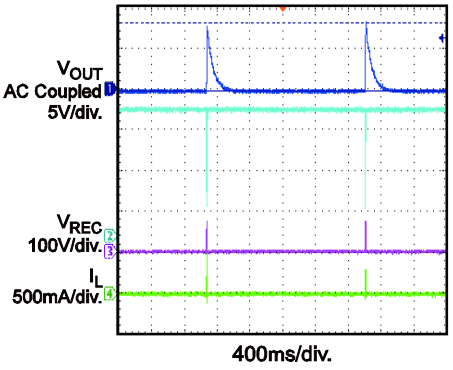
Steady State
P_{OUT} = 100W



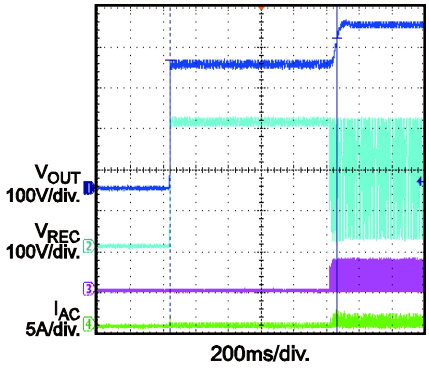
Steady State
P_{OUT} = 50W



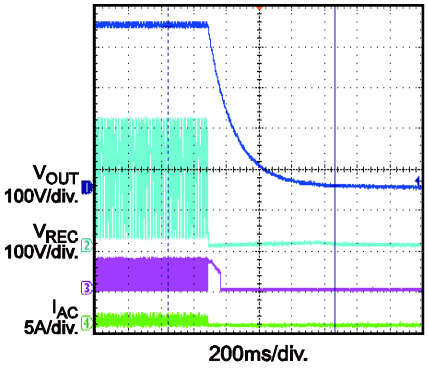
Steady State
P_{OUT} = 0W



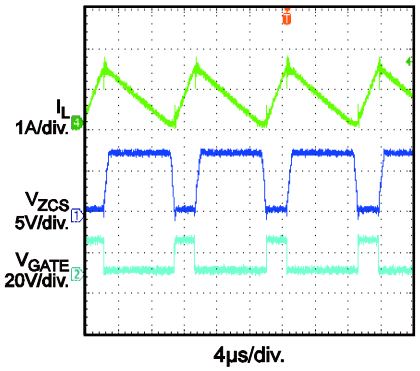
Startup



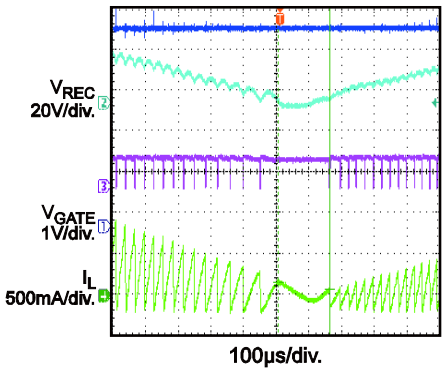
Shutdown



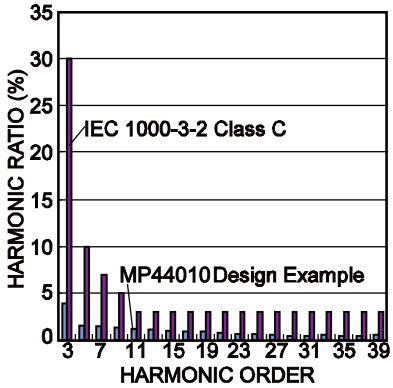
Zero-Current Sensing



Zero-Crossing Compensation
V_{AC} =85V



Harmonics



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PIN FUNCTIONS

Pin #	Name	Description
1	FB	Feedback pin. The output voltage is fed into this pin through a resistor divider.
2	COMP	Output of the error amplifier. A compensation network is connected between this pin and FB pin.
3	MULT	Input of the multiplier. Connect this pin to the rectified main voltage via a resistor divider to provide the sinusoidal reference for the current control loop.
4	CS	Current sense pin. The current through MOSFET is fed into this pin via a resistor. The resulting voltage on this pin is compared with the output of internal multiplier to get an internal sinusoidal-shaped reference, to determine MOSFET's turn-off. On-chip R/C filter can reduce high frequency noise on this pin.
5	ZCS	Inductor's zero-crossing current sensing input. A negative-transition edge triggers MOSFET's turn-on.
6	GND	Ground.
7	GATE	Gate driver output. The high output current of the gate driver is able to drive low-cost power MOSFET. The high-level voltage of this pin is clamped to 12V in case this pin is supplied with a high VIN.
8	VIN	Supply voltage of both the signal path of the IC and the gate driver. A bypass capacitor from this pin to ground is needed to reduce noise.

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BLOCK DIAGRAM

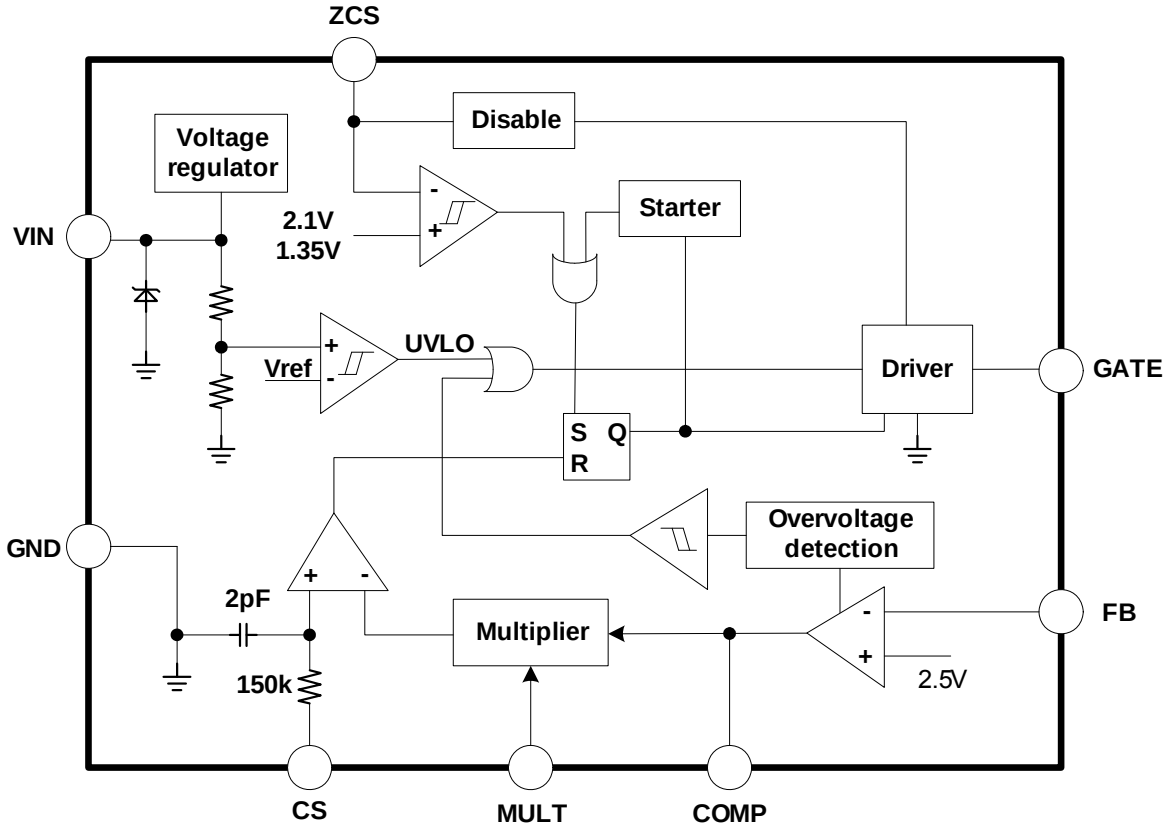


Figure 1—Functional Block Diagram

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OPERATION

The MP44010 is a boundary conduction mode PFC controller which is optimized for the PFC pre-regulator up to 300W and fully complies with the IEC1000-3-2 specification.

Output Voltage Regulation

The output voltage is sensed at the FB pin through a resistor divider from output voltage to ground. The accurate on-chip reference voltage and the high performance error amplifier regulate the output voltage accurately.

Over-Voltage Protection (OVP)

The MP44010 offers two stages of over-voltage protection: dynamic over-voltage protection and static over-voltage protection. With two-stage protection, the circuit can operate reliably.

The MP44010 achieves OVP by monitoring the current flow through the COMP pin.

At steady-state operation, the current flow through high-side feedback resistor R9 and low-side feedback resistor R10 is:

$$I_{R9} = \frac{V_O - V_{FB}}{R9} = I_{R10} = \frac{V_{FB}}{R10}$$

If there is an abrupt rise on the output (ΔV_O), and the compensation network connected between FB pin and COMP pin takes time to achieve high power factor (PF) due to the long RC time constant. The voltage on FB pin will still be kept at the reference value. The current through R10 remains equal to V_{FB}/R10, but the current through R9 will become:

$$I'_{R9} = \frac{V_O + \Delta V_O - V_{FB}}{R9}$$

This current has to flow into the COMP pin. At the same time, this current is monitored inside the chip. If it rises to 35μA, the output voltage of the multiplier will be forced to decrease and the energy delivering to output will be reduced. If this current continues to rise to about 40μA, the dynamic OVP could be triggered. Consequently, the gate driver is blocked to turn off the external power MOSFET and the device enters an idle state. This state is maintained until the current falls below 10μA, the point at which, the internal starter will be re-enabled and allows the switching to restart.

When the load is very light, the output voltage tends to stay steadily above the nominal value. In this condition, the error amplifier output will saturate low. When the error amplifier output is lower than 2.2V, static OVP will be triggered. Consequently, the gate driver will be blocked to turn off the external power MOSFET and the device enters an idle state. Normal operation is resumed once the error amplifier output goes back into the regulated region.

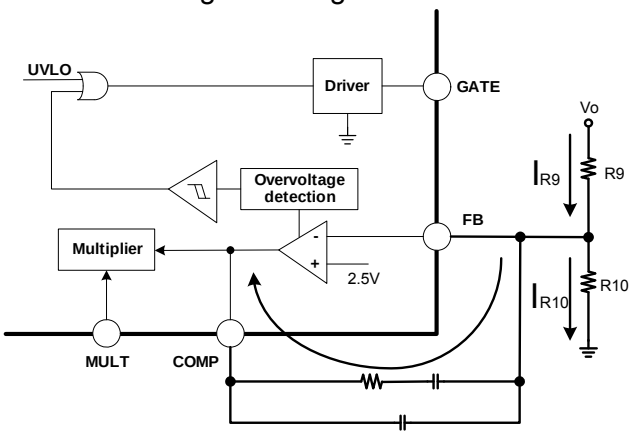


Figure 2—OVP Detector Block

Disable Function

The MP44010 can be disabled by pulling the zero current sensing (ZCS) pin lower than 190mV. This can help to further reduce quiescent current when the PFC pre-regulator needs to be shutdown. After releasing the ZCS pin, it will stay at lower clamp voltage when there is no external voltage from auxiliary winding.

Boundary Conduction Mode

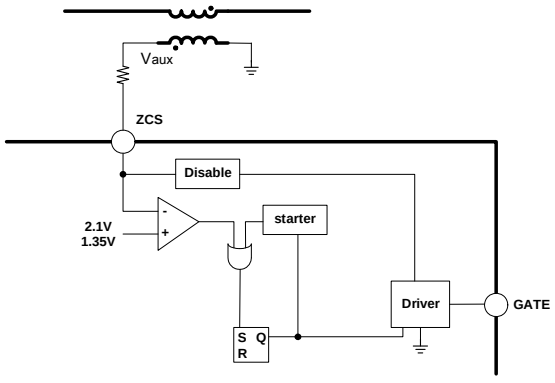


Figure 3—ZCS, Triggering and Disable Block

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When the current of the Boost inductor reaches zero, the voltage on the inductor will be reversed. Then ZCS generates the turn-on signal of the MOSFET by sensing the falling edge of the voltage on the auxiliary winding coupled with the inductor. If the voltage of the ZCS pin rises above 2.1V, the comparator waits until the voltage falls below 1.35V. Once the voltage falls below 1.35V, the MP44010 turns on the MOSFET. The 7.8V high clamp and 0.55V low clamp protect the ZCS pin. The internal 175μs timer generates a signal to turn on the MOSFET if the driver signal has been low for more than 175μs. This also allows the MOSFET to turn on during start-up period since no signal is generated from ZCD then.

Zero-crossing Compensation

The MP44010 offers 30mV voltage offset for multiplier output near the zero-crossing of the line voltage which can force the circuit to process more energy at the bottom of the line voltage. With this function, the THD of the current could be evidently reduced.

To prevent redundant energy, this offset is reduced as the instantaneous line voltage increases. Therefore the offset will be negligible near the top of the line voltage.

Power Factor Correction

The MP44010 senses the inductor current through the current sense pin and compares to the sinusoidal-shaped signal which is generated from the output of the multiplier. When the external power MOSFET turns on, the inductor current rises linearly. When the peak current hits the sinusoidal-shaped signal, the external power MOSFET begins to turn off and the diode turns on. The inductor current also begins to fall. When the inductor current reaches zero, the power MOSFET begins to turn on again, which causes the inductor current to start rising again. The power circuit works in boundary conduction mode, and the envelope of the inductor current is sinusoidal-shaped. The average input current is half of the peak current, so the average input current is also sinusoidal-shaped. A high power factor can be achieved through this control method.

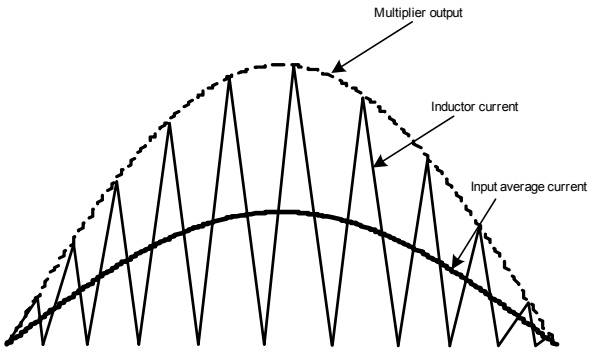


Figure 4—Inductor Current Waveform

The control flow chart of the MP44010 is shown in Figure 5.

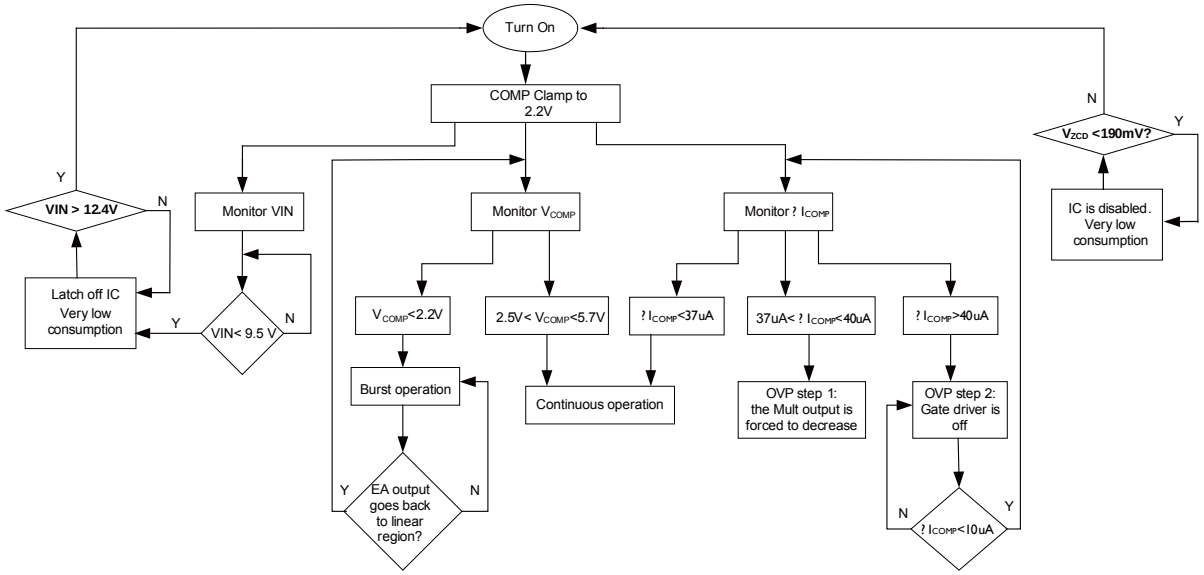


Figure 5—Control Flow Chart

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Layout Guide

For boundary mode PFC operation, the output is fed back to FB pin and is compared with the reference voltage. So a constant reference voltage is very important for output voltage accuracy. Therefore, the wire from FB pin to the feedback resistors should be as short as possible.

The envelope of the inductor current is from the multiplier output which is generated by rectified AC voltage. Therefore a good layout should keep MULT pin immune to noise. It is recommended that placing a small ceramic cap from MULT pin to GND.

For zero current sensing, R5 should be placed close to ZCS and a long connection wire should be avoided. If the long wire is necessary, a small bypass cap is needed to avoid noise.

For inductor current sensing, although there is on-chip filter on CS pin, it is still recommended that the wire from current sensing resistor to CS pin should be as short as possible to prevent falsely turning off MOSFET. If it is difficult to achieve using short wire, an external filter from sensing resistor to CS pin is recommended.

To keep the chip operating with a stable VIN voltage, a big E-cap and a small ceramic cap are good combination as VIN caps. In addition, the VIN caps should be close to VIN pin to prevent VIN voltage fluctuation.

Please see the MP44010 demo board for recommended layout.

Design Example

Case 1:

Below is a design example following the application guideline for the specifications:

V_{AC}	85~265V
V_{OUT}	400V
P_{OUT}	100W

The detailed application schematic is shown in Figure 6. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Datasheets.

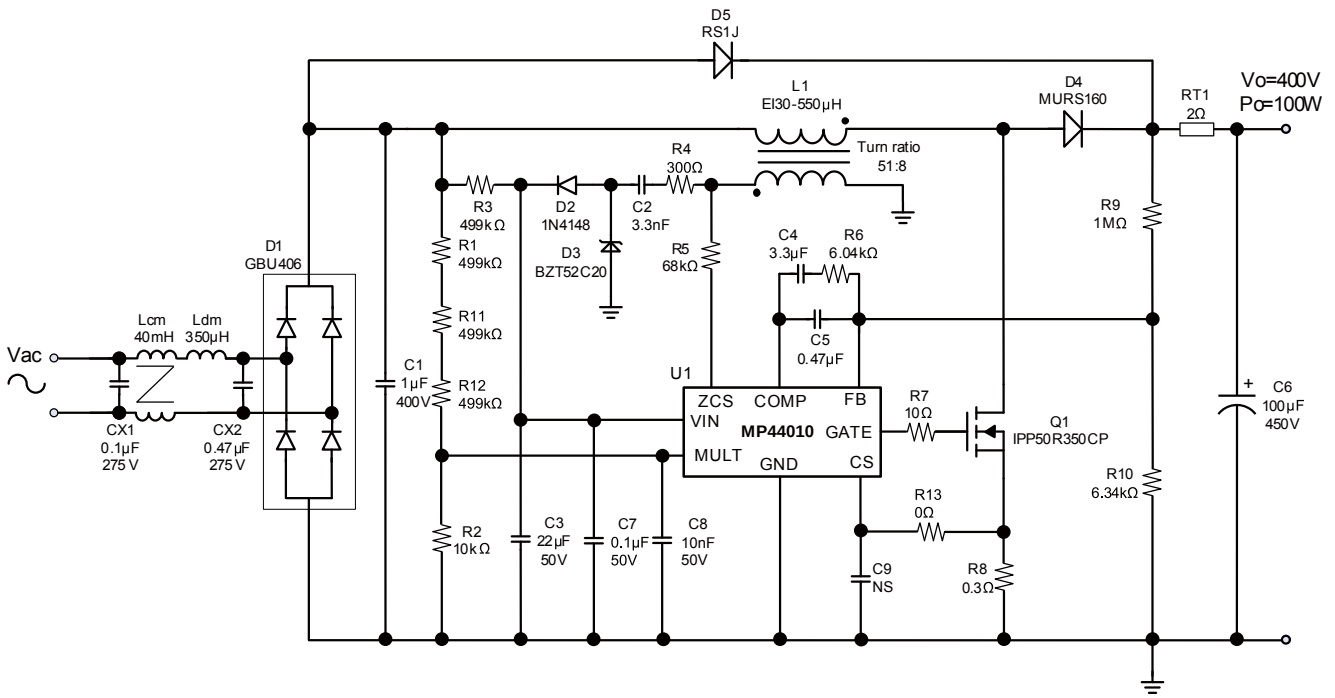


Figure 6—100W MP44010 Design Example

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Case 2:

At light load, the power loss can be saved by inserting LN60A01 to disconnect the resistor of voltage divider. The implement circuit is shown in the Figure 7.

At light load, the pin 9 of HR1000 is asserted low when it operates at burst mode, and the signal generated from pin 9 is applied to synchronize the ON/OFF of MP44010; it also can drive LN60A1 to connect or disconnect resistor of voltage divider at the same time. And the control signal of LN60A01 also can be external signal from MCU system. For more details, please refer to AN of MP44010.

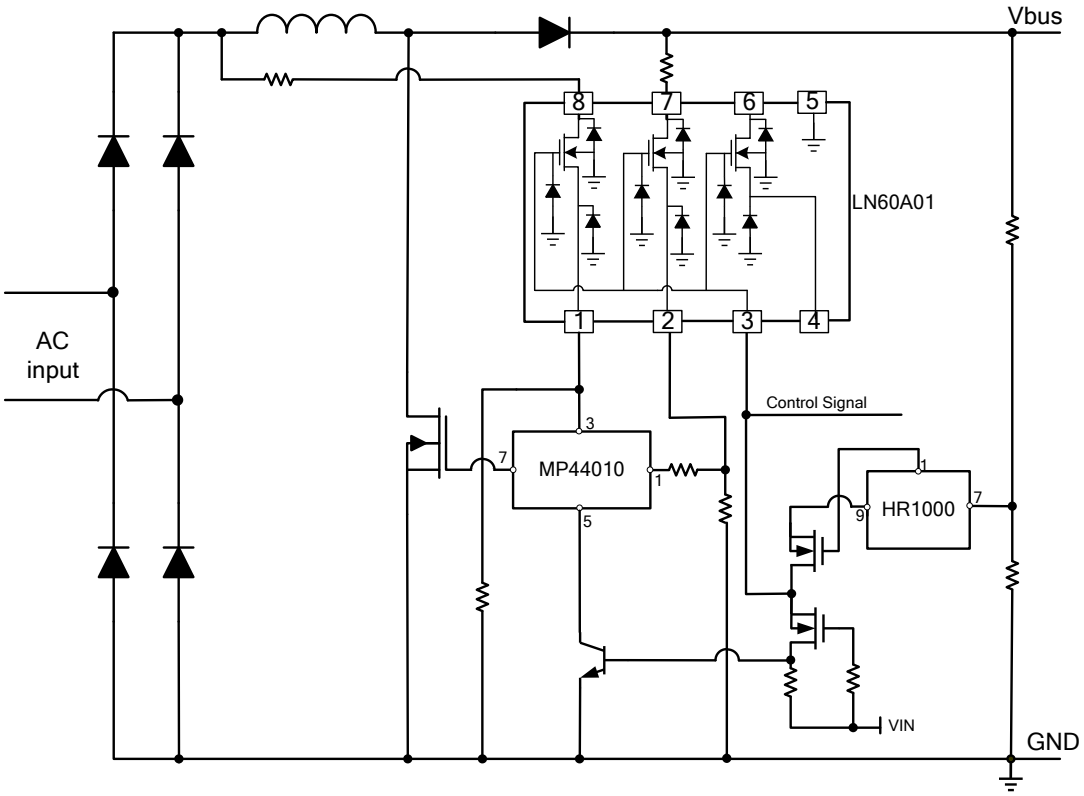
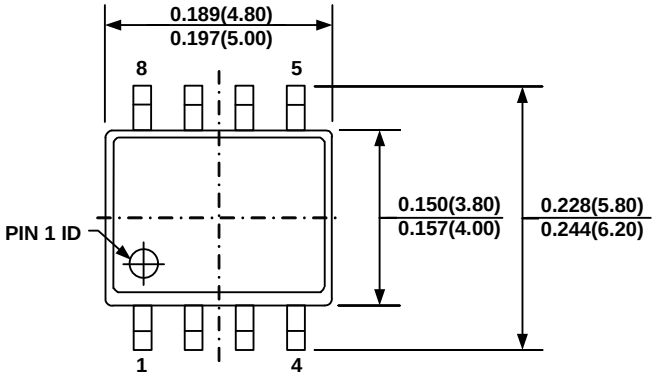


Figure 7—Power Consumption Reduction with LN60A01

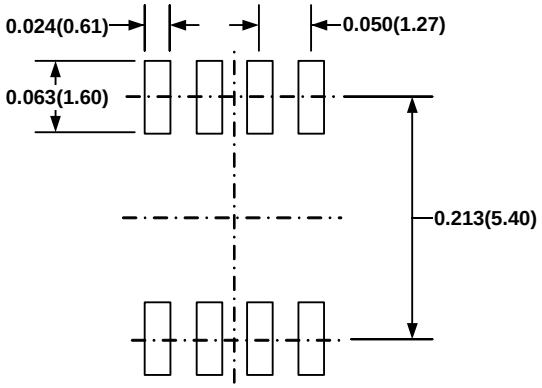
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PACKAGE INFORMATION

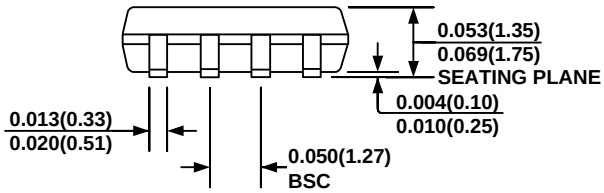
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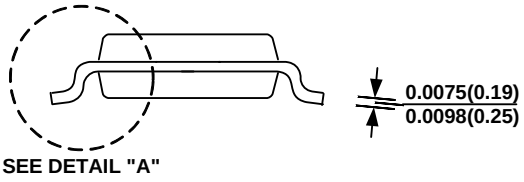
TOP VIEW



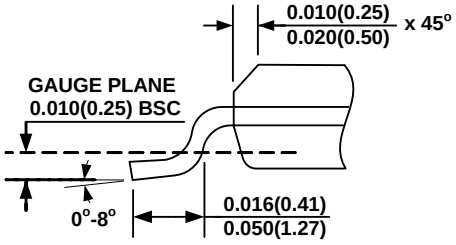
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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