EG915U-EU

Hardware Design

LTE Standard Module Series

Version: 1.0.0

Date: 2021-06-24

Status: Preliminary

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-06-24	Kexiang ZHANG/Len CHEN	Creation of the document
1.0.0	2021-06-24	Kexiang ZHANG/Len CHEN	Preliminary

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1 Introduction

This document defines the EG915U-EU module and describes its air interfaces and hardware interfaces which relate to customers' applications.

It can help customers quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, customers can use this module to design and to set up mobile applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Overview

The module is an LTE module, supports LTE-FDD, LTE-TDD and GSM network data connection. It also provides voice functionality, Bluetooth and Wi-Fi Scan for customer's specific applications. Related information and details are listed in the table below:

Table 2: Brief Introduction of the Module

Categories	
Packaging and pins number	LGA; 126
Dimensions	23.6 mm × 19.9 mm × 2.4 mm
Weight	TBD
Wireless network functions	LTE/GSM/Bluetooth/Wi-Fi Scan

NOTE

1. The Bluetooth and Wi-Fi Scan functions of the EG915U-EU are integrated, but the Bluetooth and Wi-Fi Scan functions cannot be used at the same time, and only one of them can be selected.
2. EG915U-EU supports Bluetooth and Wi-Fi functions. Because of common antenna interfaces, two functions cannot be used at the same time: Bluetooth and Wi-Fi are optional (both supported or not). It also provides models that do not support Bluetooth and Wi-Fi Scan functions. Please consult Quectel Technical Support for details.

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	EG915U-EU
LTE-FDD	B1/B3/B5/B7/B8/B20/B28
GSM	850/900/1800/1900 MHz
Bluetooth/Wi-Fi Scan [1]	2.4 GHz

[1] Optional.

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	● Supply voltage: 3.3 V-4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode. ● Point-to-point MO and MT. ● SMS cell broadcast. ● SMS storage: ME by default.
(U)SIM Interface	Supports USIM/SIM card: 1.8 V, 3.0 V
Audio Features	● Supports two analog audio interfaces: one analog audios input and one analog audios output. ● GSM: HR/FR/EFR/AMR/AMR-WB
PCM Interface	● Used for audio function with external codec ● Supports slave modes, not master mode.
SPI Interface	● Provides a duplex, synchronous and serial communication link with the peripheral devices. ● One SPI interface, only supports master mode. ● 1.8 V operation voltage with clock rates up to 25 MHz.
I2C Interface	● One I2C interface ● Comply with I2C-bus specification version
USB Interface	● Compliant with USB 2.0 specification (only slave), with transmission rates up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, firmware upgrade USB Serial Driver: supports USB serial driver for Windows 7/8/8.1/10, Linux 2.6/3.x/4.1–5.12 and Android 4.x–11.x systems
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission. ● Baud rate: 115200 bps by default. ● Supports RTS and CTS hardware flow control. **Debug UART:** ● Used for Linux console and log output. ● Baud rate: 921600 bps. ● Only use for debug UART, cannot use for universal UART.

	Auxiliary UART
Network Indication	NET_STATUS to indicate network connectivity status.
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands.
Antenna Interface	● ANT_MAIN ● Bluetooth and Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN) ● 50 Ω impedance.
Transmitting Power	● GSM850/EGSM900：Class 4 (33 dBm ±2 dB) ● DCS1800/PCS1900：Class 1 (30 dBm ±2 dB) ● LTE-FDD：Class 3 (23 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB)
LTE Features	● Supports up to non-CA Cat 1 FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports uplink QPSK, 16-QAM ● Supports downlink QPSK, 16-QAM and 64-QAM ● FDD: Max 10 Mbps (DL) / 5 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1-4 Max 85.6 Kbps (DL)/ 85.6 Kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING /CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS protocols. ● Supports the protocols PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol).
Firmware Upgrade	Use USB interface or FOTA to upgrade.
Temperature Range	● Operating temperature range: -35 °C to +75 °C [2] ● Extended operating temperature range: -40 °C to +85 °C [3] ● Storage temperature range: -40 °C to +95 °C
RoHS	All hardware components are fully compliant with EU RoHS directive.

[2] Within operating temperature range, the module is 3GPP compliant.
[3] Within extended operating temperature range, proper mounting, heating sinks and active cooling may be required to make certain functions of the module such as voice, SMS, data transmission to be realized. Only one or more parameters like Pout might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Radio frequency
- Peripheral interface

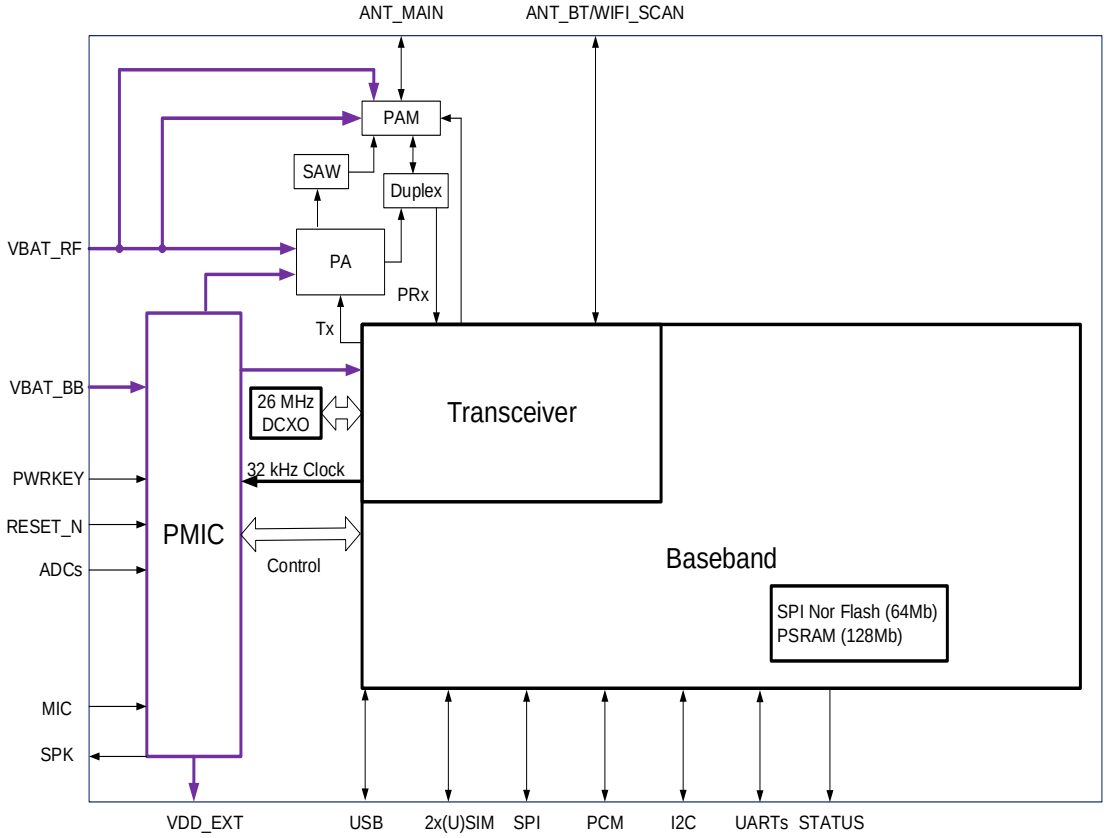


Figure 1: EG915U-EU Functional Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

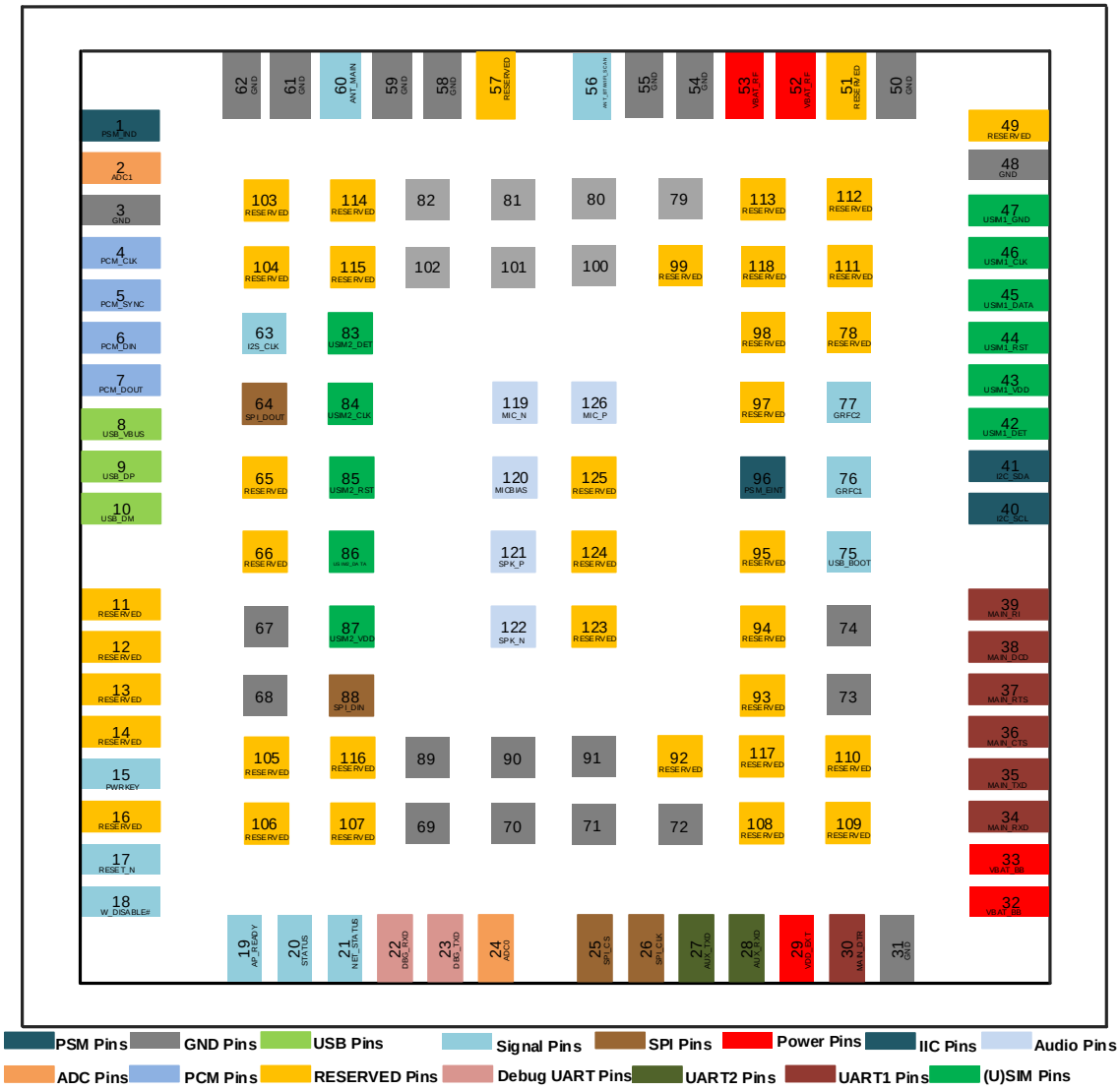


Figure 2: EG915U-EU Pin Assignment (Top View)

NOTE

1. USB_BOOT cannot be pulled up before the module startup.
2. Keep NC and RESERVED pins unconnected, all GND pins shall be connected to the ground.
3. The functions of pin 1 and pin 63 are under development and we do not recommend using them.
4. USIM2 is under development, not recommended for the time being. For details, please contact the technical support of remote communication.

2.5. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1 A
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 2.5 A
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Add 2.2 μF bypass capacitor

					when in use. If unused, keep it open.
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain.
RESET_N	17	DI	Reset the module		VBAT power domain. If unused, keep it open.
PSM_EINT*	96	DI	External interrupt pin; Wake up the module from PSM		If unused, keep it open.
Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicate the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open
NET_STATUS	21	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
PSM_IND*	1	DO	Indicate the module's power saving mode		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	Typical: 5.0 V If unused, keep it open.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Require differential impedance of 90 Ω. If unused, keep it open.
USB_DM	10	AIO	USB differential data (-)		

(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	46	DO	(U)SIM1 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_RST	44	DO	(U)SIM1 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:**	

				V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open
USIM1_GND	47				Specified ground for (U)SIM1 card
USIM2_VDD*	87	PO	(U)SIM2 card power supply	Iomax = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA*	86	DIO	(U)SIM2 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_CLK*	84	DO	(U)SIM2 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_RST*	85	DO	(U)SIM2 card reset	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_DET*	83	DI	(U)SIM2 card detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V	1.8 V power domain. If unused, keep

				V_{IH}max = 2.0 V	this pin open
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	36	DO	Main UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RTS	37	DI	Main UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_RXD	34	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_DCD	38	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_TXD	35	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_RI	39	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_DTR	30	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
AUX UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**comment**
AUX_TXD	27	DO	Auxiliary UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
AUX_RXD	28	DI	Auxiliary UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART transmit	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V	1.8 V power domain. If unused, keep it

				V_{IH}max = 2.0 V	open.
DBG_TXD	23	DO	Debug UART receive	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock (for external codec)		External pull-up resistor is required. 1.8 V only. If unused, keep it open. If the I2C interface is used to connect to external codec, it cannot connect to other external devices.
I2C_SDA	41	OD	I2C serial data (for external codec)		
I2S Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2S_CLK*	63	DO	I2S clock		If unused, keep it open. The function is under development, we do not recommend customers to use it.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	5	DI	PCM data frame sync	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open. Only support slave mode.
PCM_CLK	4	DI	PCM clock	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	

PCM_DIN	6	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
PCM_DOUT	**7**	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω impedance
ANT_BT/WIFI_SCAN	56	AIO	Wi-Fi/Bluetooth antenna interface		50 Ω impedance. If unused, keep it open
GRFC Antenna Tuner Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	76	DO	Generic RF Controller		. If unused, keep this pin open.
GRFC2	77	DO			
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	26	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Just master mode only.
SPI_CS	25	DO	SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI_DIN	88	DI	SPI master mode input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI_DOUT	64	DO	SPI master mode output	V_{OL}max = 0.45V V_{OH}min = 1.35V	
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0 V to VBAT	If unused, keep it open.
ADC1	2	AI			
Other Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	75	DI	Force the module into emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved.
W_DISABLE#	18	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep it open.
AP_READY	19	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_N	119	AI	Microphone analog input (-)		
MICBIAS	120	PO	Bias voltage output for microphone	Vo = 2.2–3.0 V Vnom = 2.2 V	
SPK_P	121	AO	Analog audio differential output (+)		
SPK_N	122	AO	Analog audio differential output (-)		
MIC_P	126	AI	Microphone analog input (+)		
GND Interfaces					
Pin Name	**Pin No.**				
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67, 68, 69, 70, 71, 72, 73, 74, 79, 80, 81, 82, 89, 90, 91, 100, 101, 102				

RESERVED Interfaces	
Pin Name	**Pin No.**
RESERVED	11, 12, 13, 14, 16, 49, 51, 57, 65, 66, 78, 92, 93, 94, 95, 97, 98, 99, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 123, 124, 125

2.6. EVB

In order to help customers to develop applications with the module conveniently, Quectel supplies an evaluation board (UMTS&LTE EVB), USB data cable, earphone, antenna, and other peripherals to control or to test the module. For more details, please refer to ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

The table below outlines operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module is registered on the network and ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN [=0]** command can set the module to a minimum functionality mode. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN [=4]** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, current consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	In this mode, the VBAT power supply is constantly turned on and the software stops working.	

3.2. Sleep Mode

EG915U-EU is able to reduce its current consumption to an ultra-low value in the sleep mode. The following section describes power saving procedures of EG915U-EU module.

3.2.1. UART Application Scenario

If the host communicates with the module via UART interface, all the following two preconditions should be met to set the module enter into sleep mode:

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Drive MAIN DTR to a high level.

The figure illustrates the connection between the module and the host.

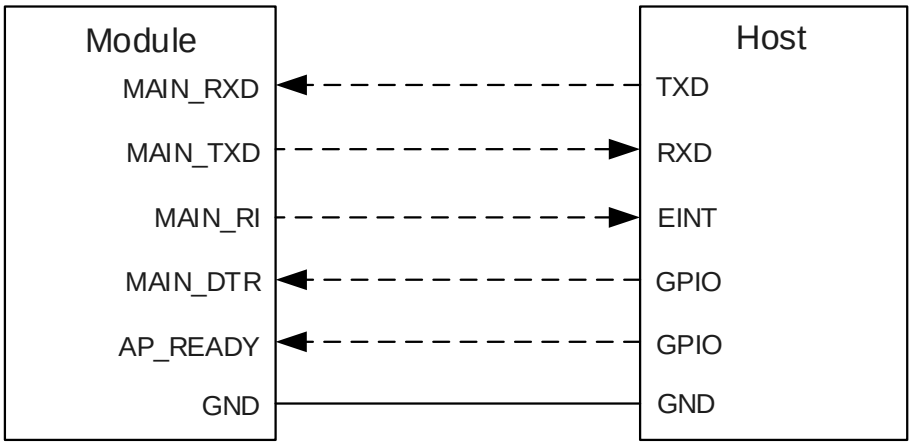


Figure 3: Sleep Mode Application via UART

- Driving the host DTR low will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin.

3.2.2. USB Application Scenario

For the two situations below, three preconditions must be met to set the module enter sleep mode:

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the DTR is held at a high level or keep it open.
- The host's USB Bus, which is connected with the module's USB interface, enters Suspend state.

3.2.2.1. USB Application with USB Remote Wakeup Function*

The host supports USB Suspend/Resume and remote wakeup function.

The figure illustrates the connection between the module and the host.

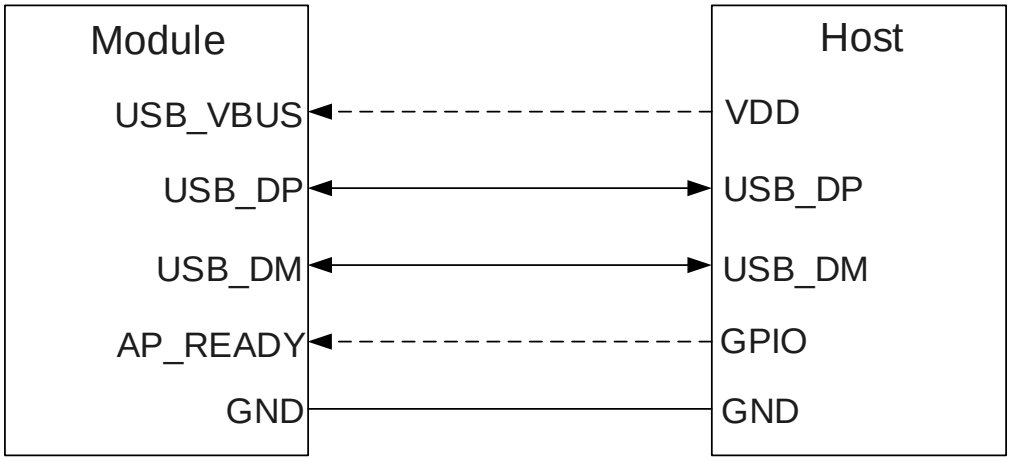


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals to USB Bus to wake up the host.

NOTE

Under Linux OS, USB support Suspend, under Windows OS nonsupport Suspend.

3.2.2.2. USB Application with USB Suspend/Resume and RI Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the RI signal is needed to wake up the host.

The following figure illustrates the connection between the module and the host.

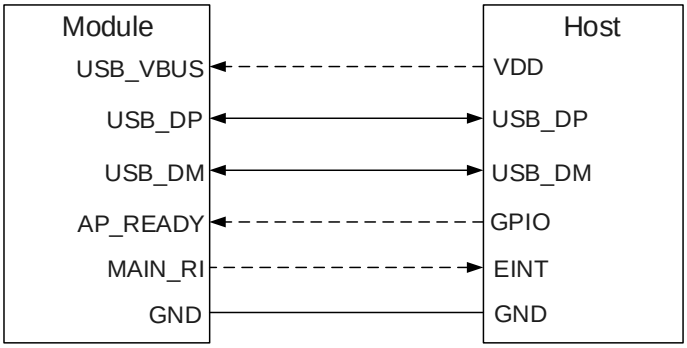


Figure 5: Sleep Mode Application with RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, RI signal will wake up the host.

NOTE

Under Linux OS USB support Suspend, under Windows OS nonsupport Suspend.

3.3. Airplane Mode

When the module enters into airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default and **AT+QCFG= "airplanecontrol", 1** can be used to enable the function. Driving it low will set the module enter airplane mode.

Software：

AT+CFUN=<fun> command provides choices of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality (disable RF function and (U)SIM function).
- **AT+CFUN=1:** Full functionality (default).
- **AT+CFUN=4:** Airplane mode (disable RF function).

3.4. Power Supply

3.4.1. Power Supply Pins

EG915U-EU power pins are used to connect an external power, supply power to the RF and BB circuits of the module.

The following table shows the details of power supply and GND pins.

- Two VBAT_RF pins for RF part.
- Two VBAT_BB pins for BB part.

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	
VBAT_RF	52, 53	PI	Power supply for the module's RF part	
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Power supply for external GPIO's pull-up circuits. Add 2.2 μF bypass capacitor when in use. If unused, keep it open.

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3.0 A at least. If the voltage drops between input and output is not too high, it is suggested that an LDO should be used to supply power to the module. If there is a big voltage difference between input and the desired output VBAT, a buck converter is preferred as the power supply.

The following figure illustrates a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

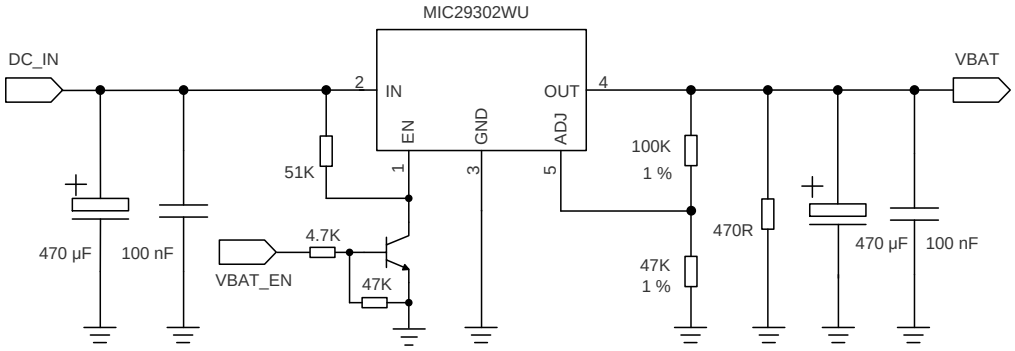


Figure 6: Reference Design of Power Supply

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage will never drop below 3.3 V.

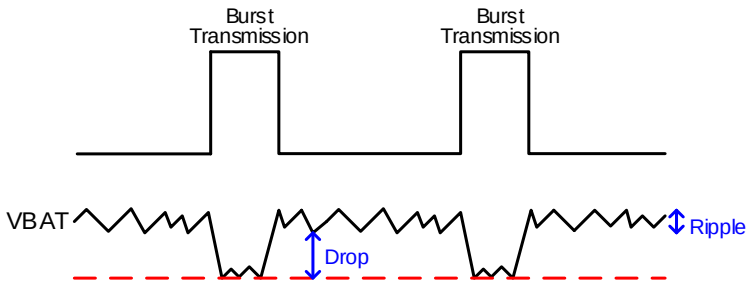


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage ‘s drop, a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single

voltage source and can be expanded to two sub paths with the star structure. The width of VBAT_BB trace should be no less than 2.0 mm. The width of VBAT_RF trace should be no less than 2.5 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The following figure shows the reference circuit with and without charging function.

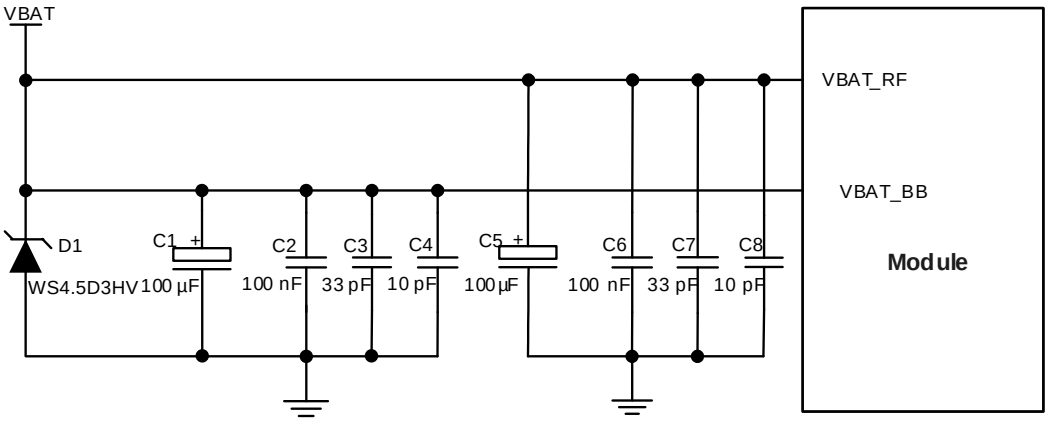


Figure 8: Star Structure of the Power Supply

3.5. Turn On

3.5.1. Turn on the Module with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	VBAT power domain.

When the module is in power off mode, it can be turned on and enter normal operation mode by driving the PWRKEY low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY.

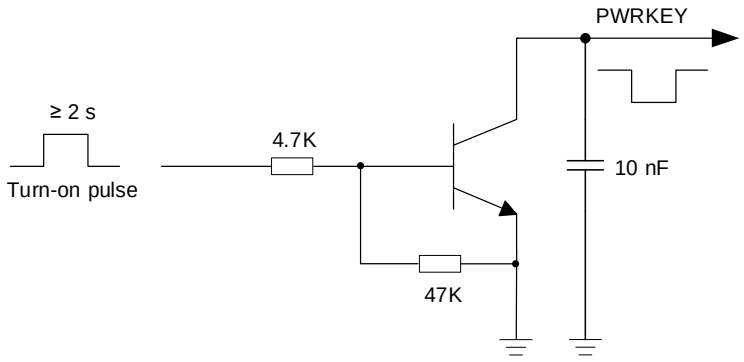


Figure 9: Reference Circuit of Turing on the Module with Driving Circuit

Another way to control the PWRKEY is by using a button directly. When pressing the button, an electrostatic strike may generate from finger. Therefore, a TVS component shall be placed near the button for ESD protection.

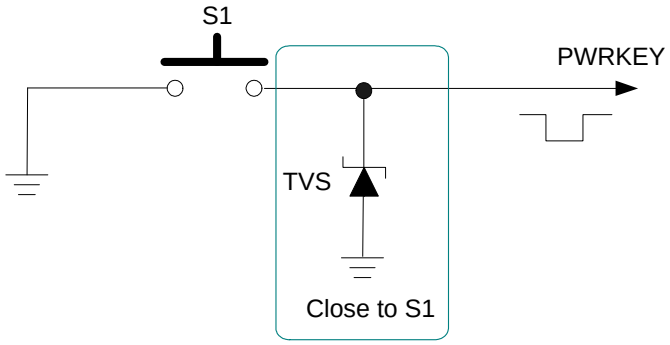


Figure 10: Reference Circuit of Turing on the Module with Keystroke

The turn on scenario is illustrated in the following figure.

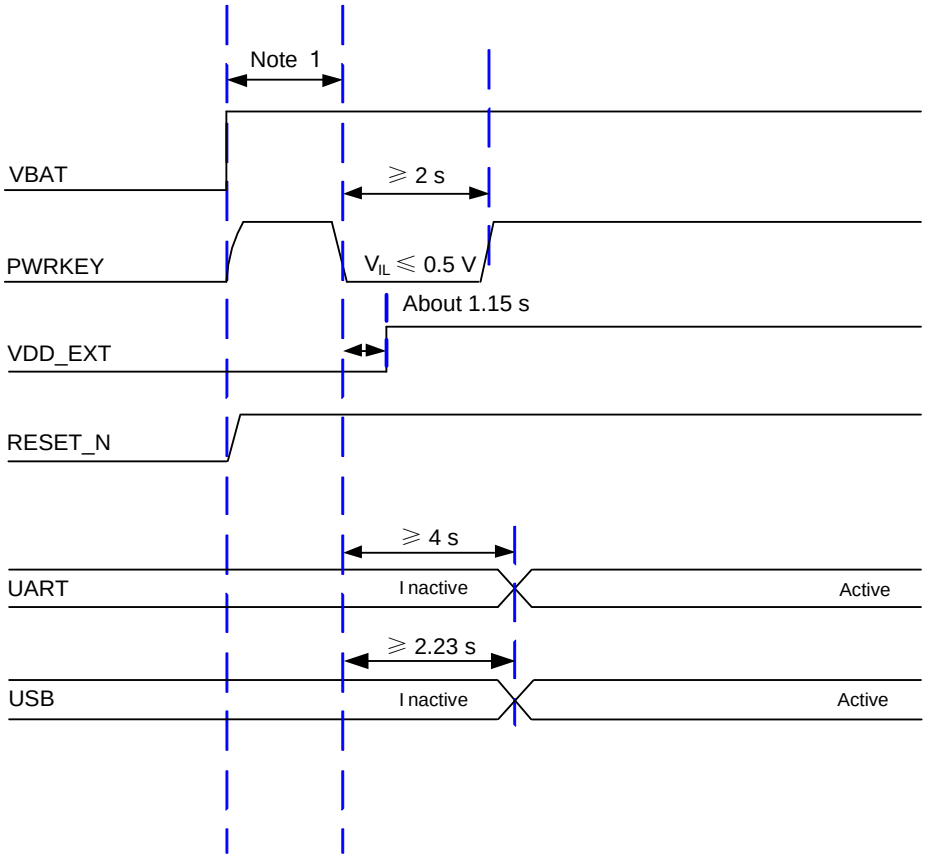


Figure 11: Power-on Timing

NOTE

1. Make sure that the VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 1 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.

3.6. Turn Off

The following procedures can be used to turn off the module:

- Using the PWRKEY pin.
- Using **AT+QPOWD** command.

3.6.1. Turn off the Module with PWRKEY

Driving the PWRKEY to a low-level voltage for at least 3 s, then the module will execute power-down procedure after the PWRKEY is released.

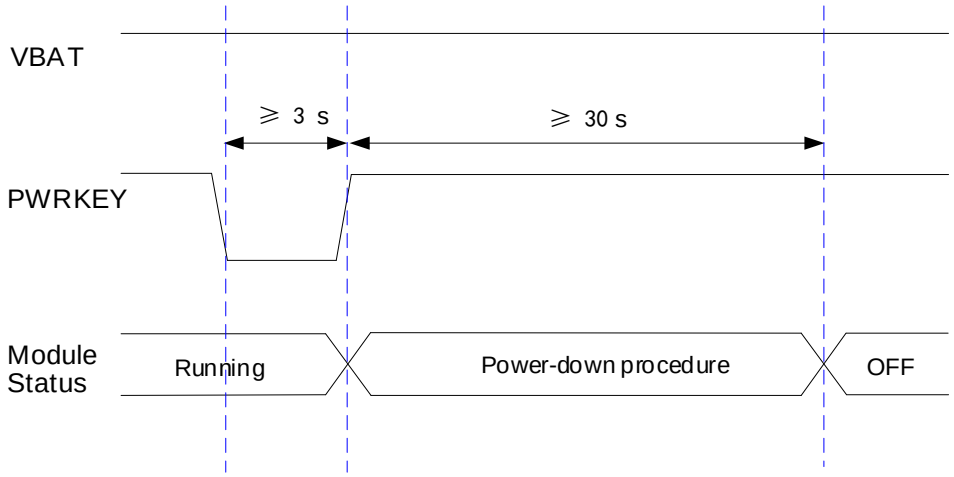


Figure 12: Power-down Timing

3.6.2. Turn off the Module with AT Command

It is safe to use **AT+QPOWD** command to turn off the module, which is equal to turn off the module via PWRKEY Pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTE

1. To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.
2. When keeping the PWRKEY to the ground and the AT command cannot be used to turn off, the module can only be forced to turn off by cutting off the VBAT power supply. Therefore, we recommend that you can turn on or turn off the module by pulling up and pulling down the PWEKEY instead of keeping the PWRKEY to the ground.

   The time for the module to log out of the network is related to the current network status, so the specific shutdown time is related to the network status, please pay attention to the shutdown time in the design.

3.7. Reset

The module can be reset by driving the RESET_N low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Definition of RESET

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	VBAT power domain. If unused, keep it open.

The recommended circuit is equal to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

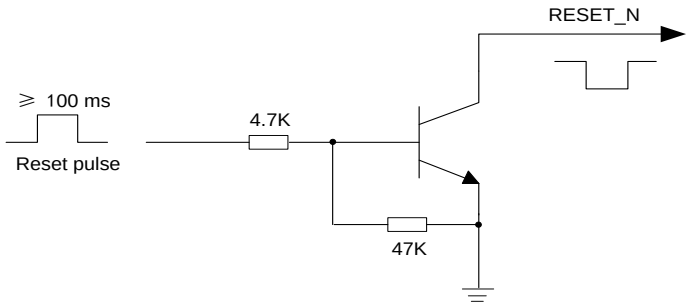


Figure 13: Reference Circuit of RESET_N with Driving Circuit

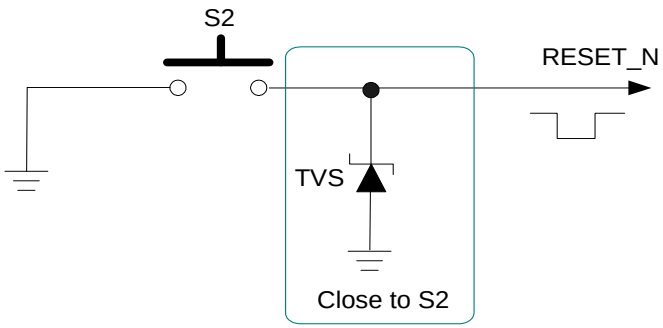


Figure 14: Reference Circuit of RESET_N with Button

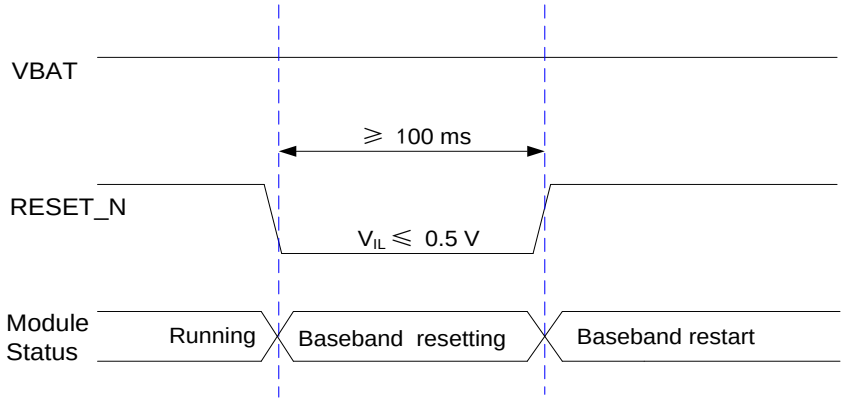


Figure 15: Reset Timing

NOTE

1. Please ensure that there is no large capacitance with the max value exceeding 10 nF on PWRKEY and RESET_N pins.
2. It is recommended to use RESET_N only when failing to turn off the module by **AT+QPOWD** command or PWRKEY pin.

4 Application Interfaces

4.1. Analog Audio Interfaces

Table 11: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description
MIC_N	119	AI	Microphone analog input (-)
MICBIAS	120	PO	Bias voltage output for microphone
SPK_P	121	AO	Analog audio differential output (+)
SPK_N	122	AO	Analog audio differential output (-)
MIC_P	126	AI	Microphone analog input (+)

- AI channels are differential output channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output receiver.

4.1.1. Audio Interfaces Design

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The filter capacitors on the PCB board should be placed as close to the audio devices or audio interfaces as possible, and the traces should be as short as possible. they should go through the filter capacitors before arriving other connection points.
In order to reduce radio or other signal interference, the radio frequency antenna should be far away from the audio interface and audio traces. The power traces should not be parallel to the audio traces, and

should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

4.1.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

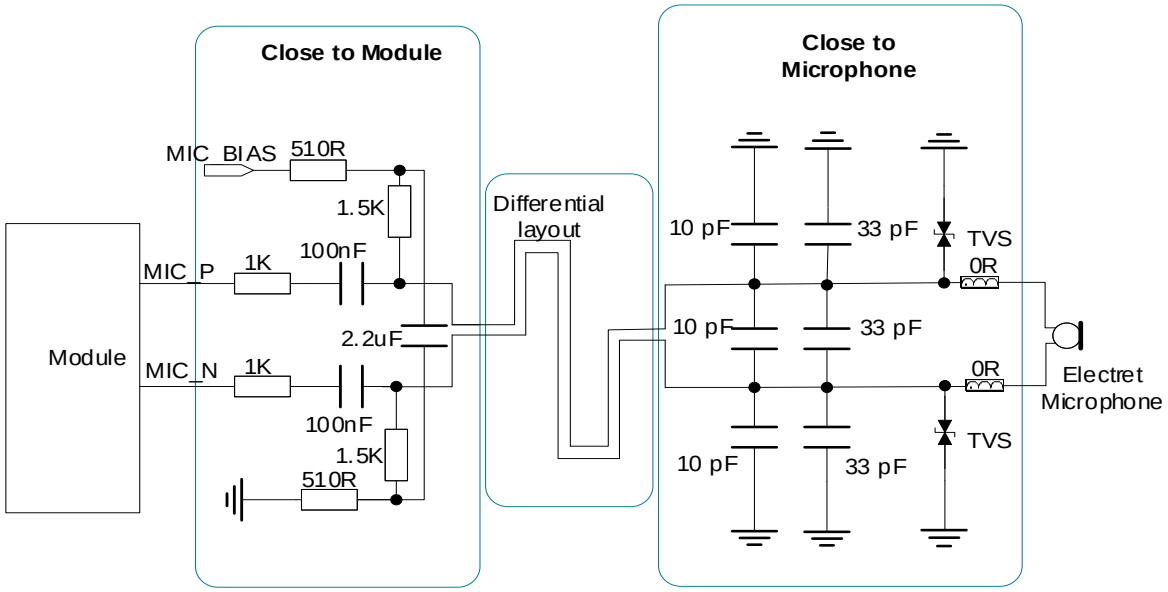


Figure 16: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

4.1.3. Receiver Interface Design

The receiver channel reference circuit is shown in the following figure:

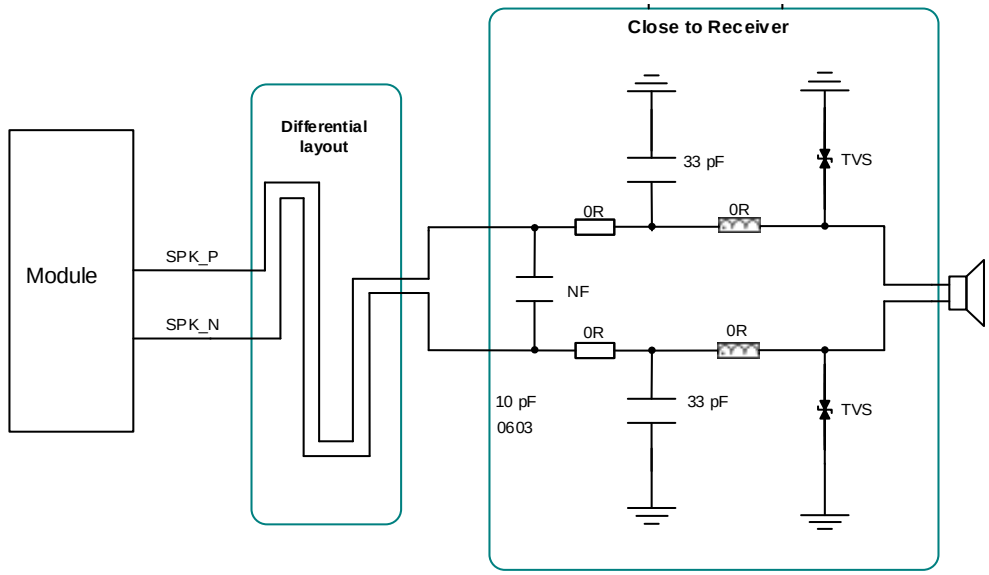


Figure 17: Reference Design for Receiver Interface

4.2. USB Interface

EG915U-EU provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 12: Functions of the USB Interface

Functions	
Data communication with external AP	Y
AT command communication	Y
Data transmission	Y
GNSS NMEA output	N
Software debugging	Y
Firmware upgrade	Y

Voice over USB	N

Pin definition of the USB interface is here as follows:

Table 13: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typical 5.0 V Minimum 3.5 V
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Require differential impedance of 90 Ω. If unused, keep it open.
USB_DM	10	AIO	USB differential data (-)	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

It is recommended to reserve test points for debugging and firmware upgrade in customers' designs. The following figure shows a reference circuit of USB interface.

It is recommended to reserve test points for debugging and firmware upgrading in customers' designs.

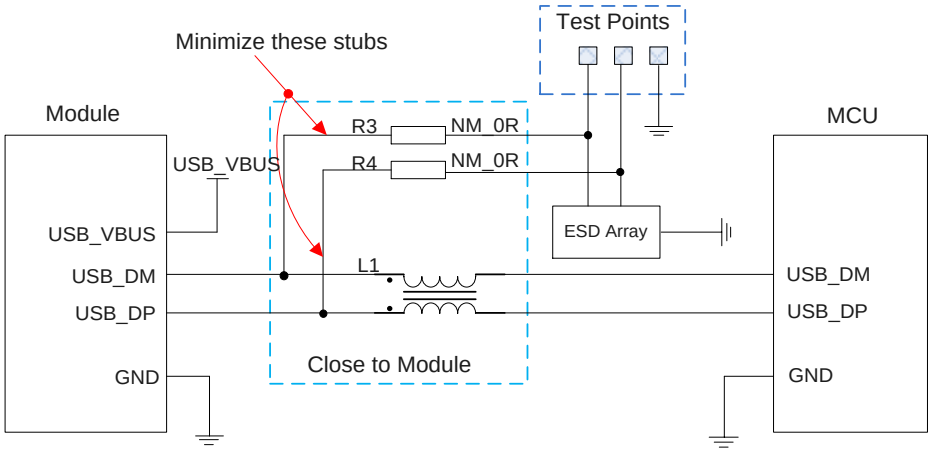


Figure 18: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R3 and R4 components must be placed close to the module, and also resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

- The following principles should be complied with when designing the USB interface, to meet USB specifications.
- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Please pay attention to the selection of the ESD component on the USB data line. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

For more details about the USB specifications, please visit http://www.usb.org/home.

4.3. USB_BOOT Interface

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before powering up, and the module will enter download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

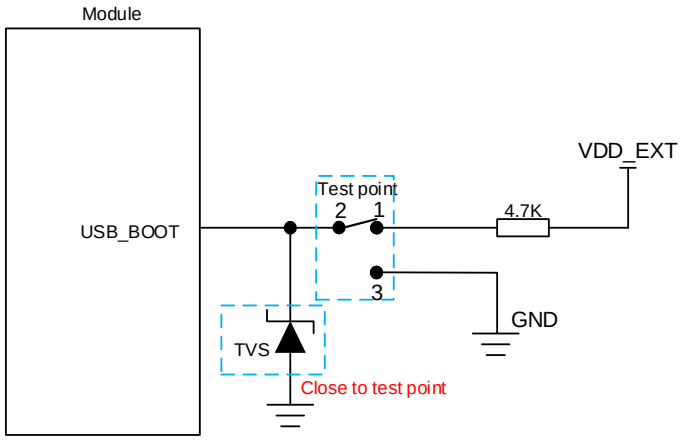


Figure 19: Reference Circuit of USB_BOOT Interface

NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.

4.4. (U)SIM Interface

The (U)SIM interface circuitry meets *ETSI* requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported. and USIM2* function is still under development.

Table 14: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep this pin open
USIM1_GND	47			Specified ground for (U)SIM1 card
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	IO	(U)SIM2 card data	
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DET	83	DI	(U)SIM2 card detect	

EG915U-EU module supports (U)SIM card hot-plug via the USIM_DET pin. The function supports rising edge and falling edge detections. By default, it is disabled, and can be configured via **AT+QSIMDET** command. Please refer to ***document [2]*** for details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

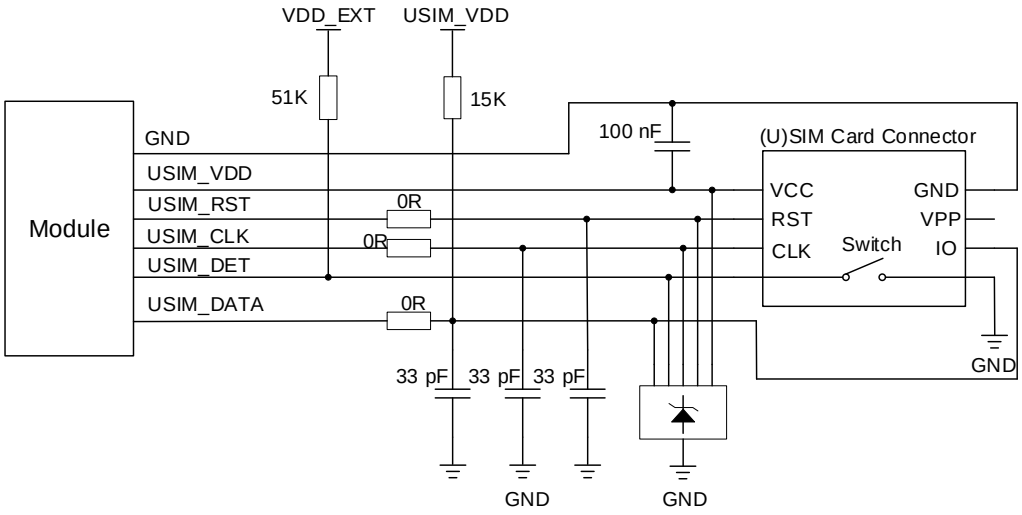


Figure 20: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

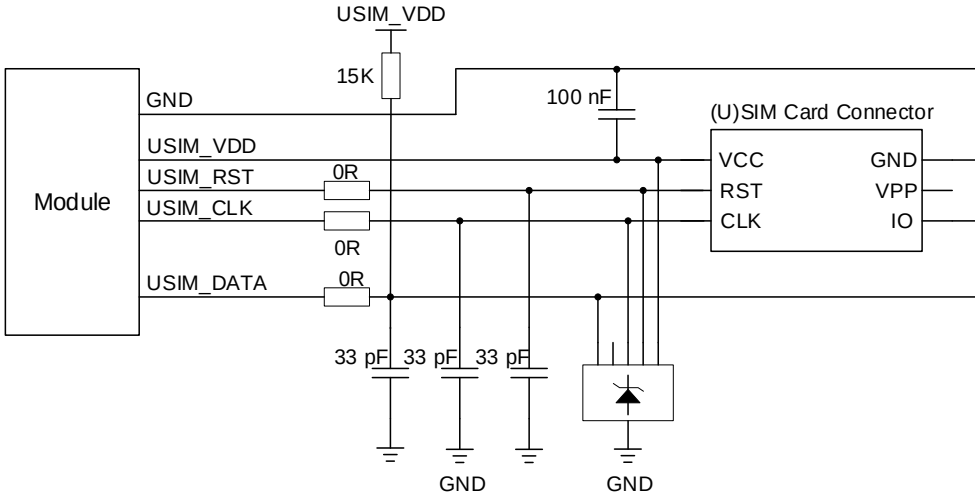


Figure 21: Reference Circuit of a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm as far as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Ensure USIM_VDD has a bypass capacitor less than 1 µF, and the capacitor should be close to the (U)SIM card connector.

- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

NOTE

USIM2 is under development, not recommended for the time being. For details, please contact the technical support of remote communication.

4.5. I2C and PCM Interfaces

EG915U-EU provides one I2C interface and one Pulse Code Modulation (PCM) interface.

The PCM interface of EG91U-EU series only supports slave mode, not master mode. Therefore, an external clock must to be provided to the codec.

The following table shows the pin definition I2C of and PCM interfaces which can be applied on audio.

Table 15: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	40	OD	I2C serial clock (for external codec)	External pull-up resistor is required. 1.8 V only. If unused, keep it open. If the I2C interface is used to connect to external codec, it cannot connect to other external devices.
I2C_SDA	41	OD	I2C serial data (for external codec)	
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PCM data output	
PCM_SYNC	5	DI	PCM data frame sync	
PCM_CLK	4	DI	PCM clock	

The following figure shows a reference design of PCM interface with external codec IC.

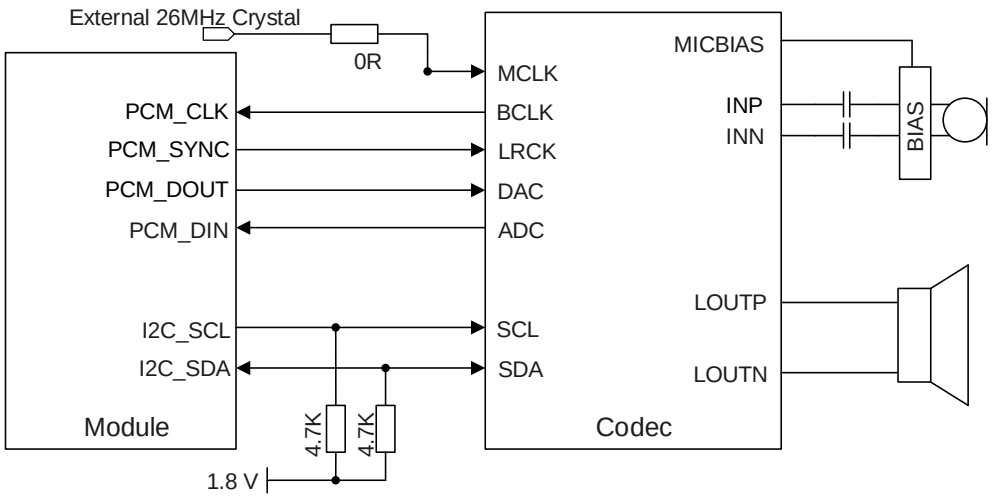


Figure 22: Reference Circuit of PCM Application with Audio Codec

4.6. UART Interface

The module provides 3 UART interfaces and the following shows their features:

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. This interface is used for data transmission and AT command communication.
- The debug UART interface supports 921600 bps baud rate. It is used for the output of partial logs.
- Auxiliary UART.

The following tables show the pin definition of main UART interface.

Pin definition of the UART interface is here as follows:

Table 16: Pin Definition of UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	Main UART clear to send	1.8 V power domain
MAIN_RTS	37	DI	Main UART request to send	
MAIN_RXD	34	DI	Main UART receive	

MAIN_DCD	38	DO	Main UART data carrier detect	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_RI	39	DO	Main UART ring indication	
MAIN_DTR	30	DI	Main UART data terminal ready	
AUX_TXD	27	DO	Auxiliary UART transmit	
AUX_RXD	28	DI	Auxiliary UART receive	
DBG_RxD	22	DI	Debug UART transmit	1.8 V power domain. If unused, keep it open.
DBG_TxD	23	DO	Debug UART receive	

The module provides 1.8 V UART interfaces. A level translator should be used if the application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

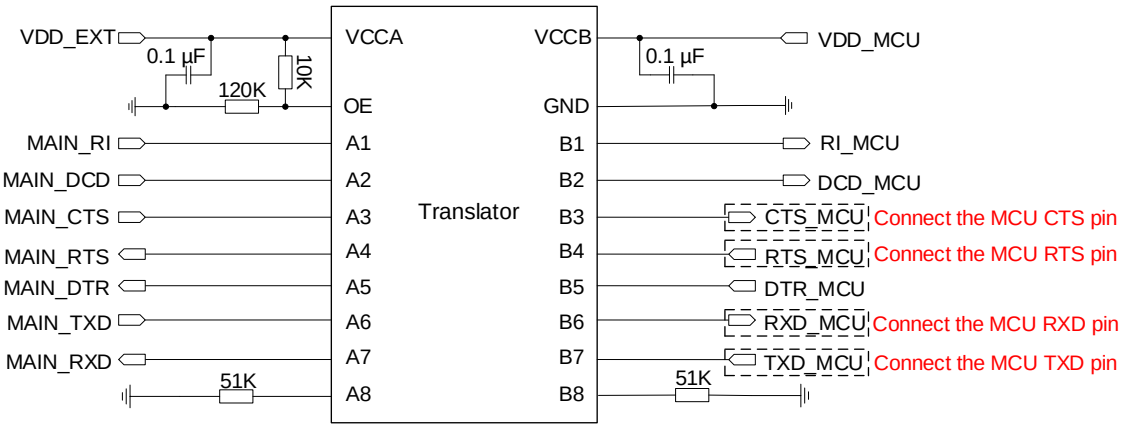


Figure 23: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, please refer to that of the circuits in solid lines, but please pay attention to the direction of connection.

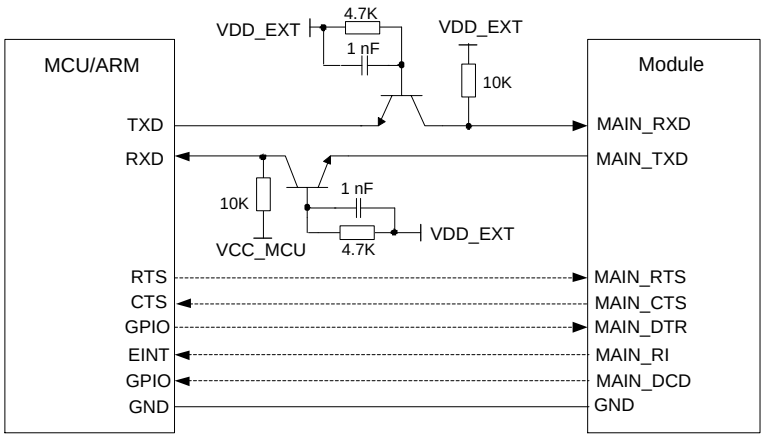


Figure 24: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Module's CTS connect to MCU's CTS, module's RTS connect to MCU's RTS. In addition, pay attention to UART's CTS and RTS input and output directions.

4.7. ADC Interface

The module provides 2 Analog-to-Digital Converter (ADC) interface. In order to improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

The module provides four analog-to-digital converter (ADC) interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. **AT+QADC=1** can be used to read the voltage value on ADC1 pin. For more details about these AT commands, please refer to ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 17: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	1 kΩ resistor must be connected in series when using.
ADC1	2	AI		

Table 18: Characteristics of ADC Interface

Name	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	VBAT	V
ADC1 Voltage Range	0	-	VBAT	V
ADC Resolution	-	12	-	bits

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.
4. If input voltage of ADC interface is designed with a resistor divider circuit, the resistance value of the external divider resistor must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be reduced significantly.

4.8. SPI Interface

The SPI interface of the EG915U-EU module only supports the master mode. It communicates with peripherals in a synchronous duplex serial manner. It has a working voltage of 1.8 V and a maximum clock frequency of 25 MHz.

Table 19: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	Just master mode only.
SPI_CS	25	DO	SPI chip select	
SPI_DIN	88	DI	SPI master mode input	
SPI_DOUT	64	DO	SPI master mode output	

NOTE

When the universal 4-wire SPI interface is used to connect Nor Flash, it supports Flash basic reading, writing, erasing etc. It needs to perform erasing and writing balanced protection by itself. It does not support the file system and can only be stored.

4.9. Control Signal

Relative interfaces' pin descriptions are here as follows:

Table 20: Pin Definition of Control Signal

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	18	DI	Airplane mode control	1.8 V power domain. Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep it open.

4.9.1. W_DISABLE#

- The module provides a W_DISABLE# pin to enable or disable airplane mode through hardware operation. W_DISABLE# is pulled up by default, and driving it low will set the module to airplane mode.
- The RF function can also be enabled or disabled through software AT commands (when **<fun>** = 0 or 4, the RF function will be disabled. When **<fun>** = 1, if W_DISABLE# is at high level, then RF function will be enabled; if it is at low level, then RF function will still be disabled.

4.10. Indication Signal

Relative interfaces' pin descriptions are here as follows:

Table 21: Pin Definition of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain
PSM_EINT*	96	DI	External interrupt pin; Wake up the module from PSM	Active High If unused, keep it open.
AP_READY	19	DI	Application processor ready	1.8 V power domain. If unused, keep it open.
NET_STATUS	21	DO	Indicate the module's network activity status	
PSM_IND*	1	DO	Indicate the module's power saving mode	

4.10.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two network indication pins: NET_MODE and NET_STATUS. The following tables describe pin definition and logic level changes in different network status.

Table 22: Working State of the Network Connection Status/Activity Indication

Pin Name	Status	Description
NET_MODE	Always High	Registered on LTE network

	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

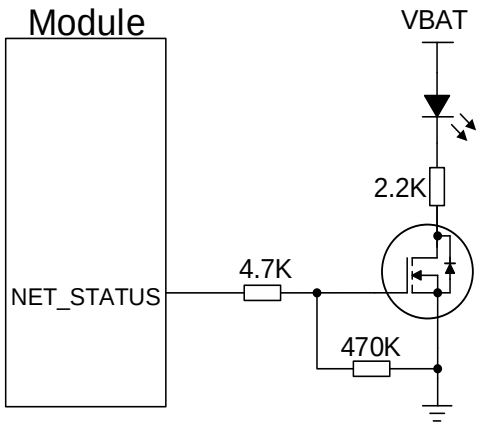


Figure 25: Reference Circuit of the Network Status Indication

4.10.2. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It will output high level when module is powered ON successfully.

A reference circuit is shown as below.

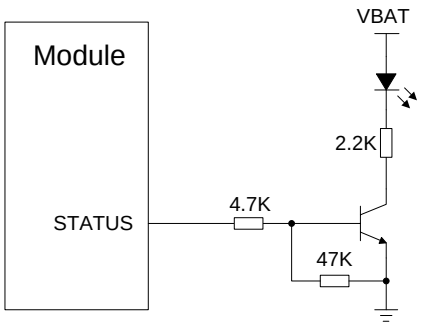


Figure 26: Reference Circuits of STATUS

4.10.3. MAIN_RI

AT+QCFG= "risignaltype", "physical" command can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG** command. The default port is USB AT port.

In addition, RI behaviors can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 23: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC return.

The MAIN_RI behavior can be changed via **AT+QCFG="urc/ri/ring"***. Please refer to ***document [2]*** for details.

5 RF Specifications

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

The pin definition is shown below:

Table 24: Pin Definition of Cellular Network Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance
ANT_BT/WIFI_SCAN	56	AI	Wi-Fi/Bluetooth antenna interface	

NOTE

Only passive antennas are supported.

Table 25: Operating Frequency of EG915U-EU

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824-849	869-894
PCS1900	1850-1910	1930-1990
EGSM900	880-915	925-960
DCS1800	1710-1785	1805-1880
LTE-B1	1920-1980	2110-2170
LTE-B3	1710-1785	1805-1880

LTE-B5	824-849	869-894
LTE-B7	2500-2570	2620-2690
LTE-B8	880-915	925-960
LTE-B20	832-862	791-821
LTE-B28	703-748	758-803

5.1.2. Tx Power

The following table shows the RF output power of the module.

Table 26: Tx Power

Frequency	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 6 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of 3GPP TS 51.010-1.

5.1.3. Receiving Sensitivity

The following table shows conducted RF receiving sensitivity of the module.

Table 27: Conducted RF Receiving Sensitivity of EG915U-EU

Frequency	Receiving Sensitivity (Typ.)	3GPP Requirement (SIMO) Primary+ Diversity
	Primary	
GSM850	TBD	-102 dBm

EGSM900	TBD	-102 dBm
DCS1800	TBD	-102 dBm
PCS1900	TBD	-102 dBm
LTE-FDD B1 (10 MHz)	TBD	-96.3 dBm
LTE-FDD B3 (10 MHz)	TBD	-96.3 dBm
LTE-FDD B5 (10 MHz)	TBD	-94.3 dBm
LTE-FDD B7 (10 MHz)	TBD	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	-93.3 dBm
LTE-FDD B20 (10 MHz)	TBD	-93.3 dBm
LTE-FDD B28 (10 MHz)	TBD	-94.8 dBm

5.1.4. Reference Design

The module provides 2 RF antenna interfaces for antenna connection.

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1, C1, C2 and R2, C3, C4) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

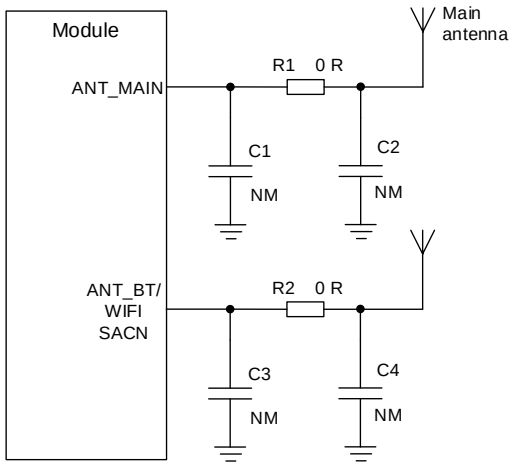


Figure 27: Reference Circuit for RF Antenna Interfaces

5.1.5. GRFC Interfaces*

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 28: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	76	DO	Generic RF Controller	1.8 V power domain. If unused, keep this pin open.
GRFC2	77	DO		

Table 29: Logic Levels of GRFC Interfaces

Parameter	Min.	Max.	Unit
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

Table 30: Truth Table of GRFC Interfaces

GRFC1 Level	GRFC2 Level	Frequency Range (MHz)	Band
Low	Low	TBD	TBD
Low	High	TBD	TBD
High	Low	TBD	TBD
High	High	TBD	TBD

5.2. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

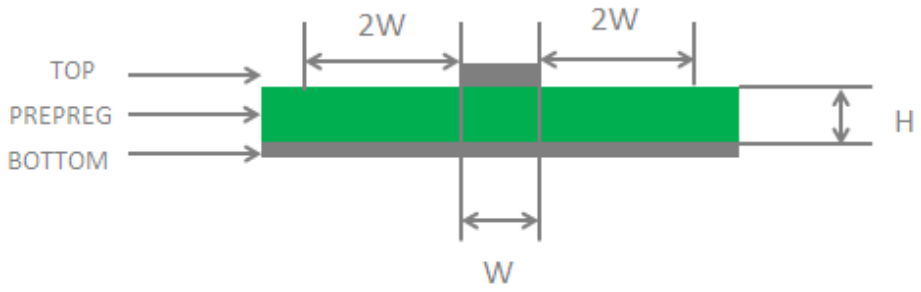


Figure 28: Microstrip Design on a 2-layer PCB

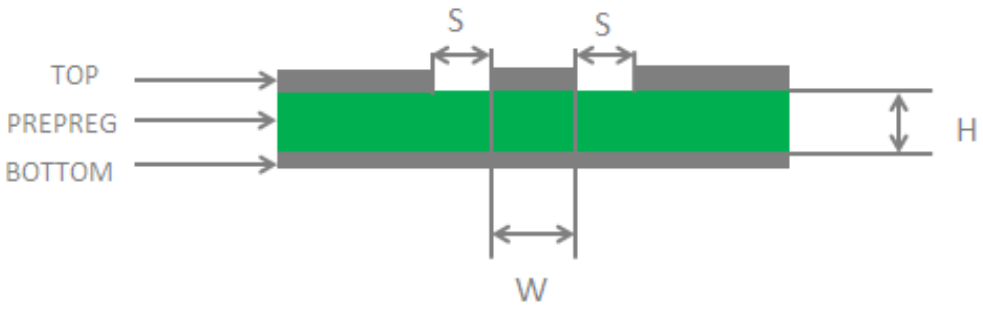


Figure 29: Coplanar Waveguide Design on a 2-layer PCB

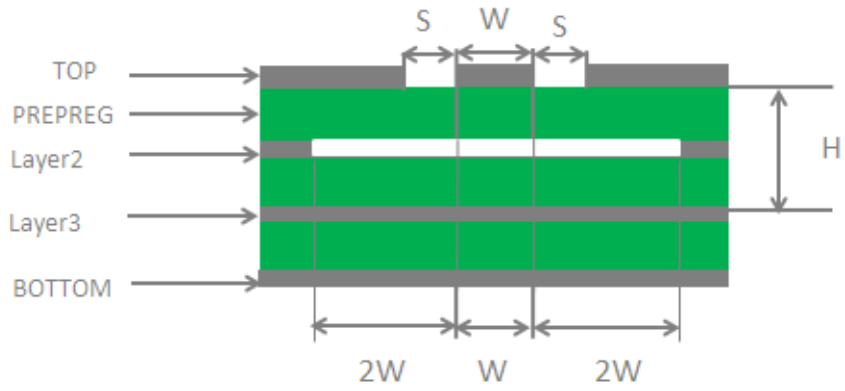


Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

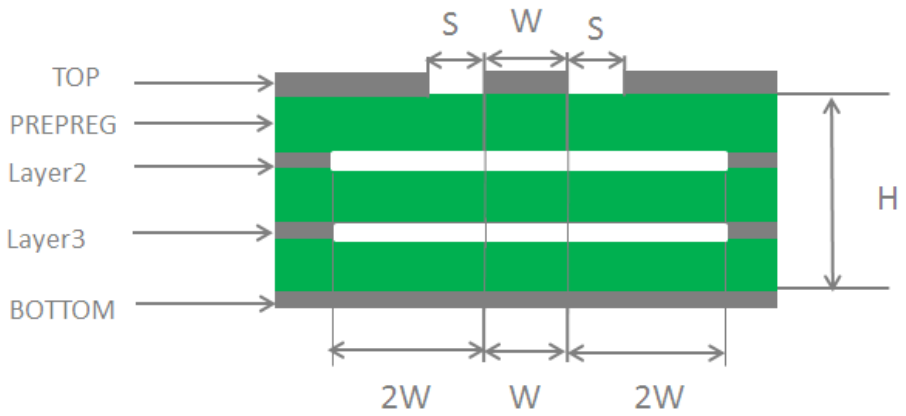


Figure 31: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, ground vias around RF traces and the reference ground improves RF performance. The distance between the ground vias and RF traces should be more than two times the width of RF signal traces (2 × W).

For more details about RF layout, please refer to ***document [3]***.

5.3. Requirements for Antenna Design

Table 31: Requirements for Antenna Design

Antenna Type	Requirements
GSM/EVDO/CDMA/UMTS/TD-SCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Polarization: Vertical Cable insertion loss: < 1 dB (< 1 GHz) Cable insertion loss: < 1.5 dB (1~2.3 GHz) Cable insertion loss: < 2 dB (2.3 GHz)

5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by *Hirose*.

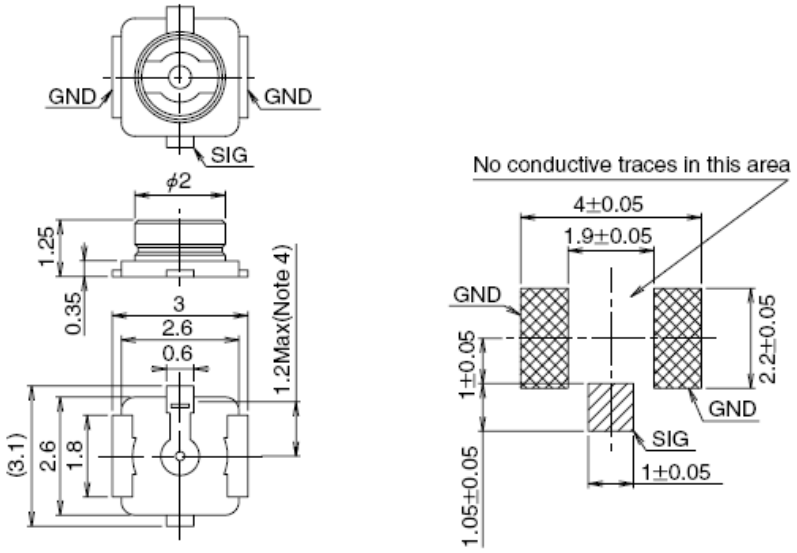


Figure 32: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

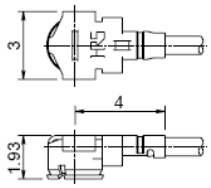
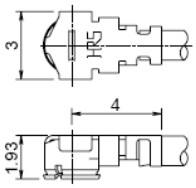
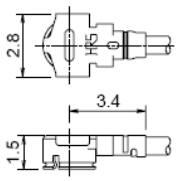
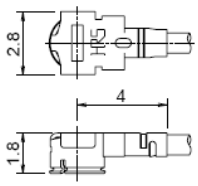
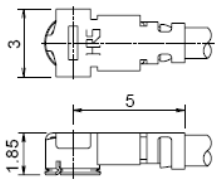
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 33: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

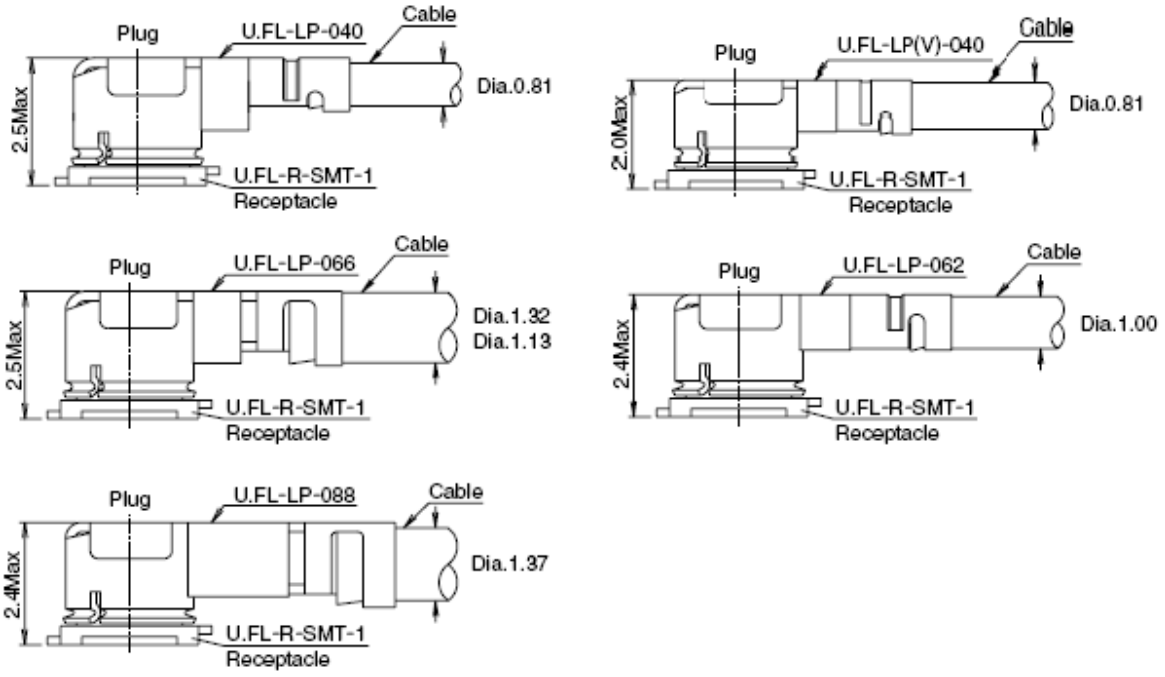


Figure 34: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 32: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	TBD	A
Peak Current of VBAT_RF	0	TBD	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT	V
Voltage at ADC1	0	VBAT	V

6.2. Power Supply Ratings

Table 33: The Module's Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM 900	-	-	400	mV
	Voltage drop during peak data rate		-	-	TBD	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM 900	-	TBD	TBD	A
USB_VBUS	USB connection detection		3.5	5.0	5.25	V

6.3. Power Consumption

Table 34: The Module Power Consumption

EG915U-EU			
Description	**Conditions**	**Typ.**	**Unit**
OFF state	Power down	TBD	uA
Sleep state	TBD	TBD	mA
Idle state	TBD	TBD	mA

LTE data transfer (GNSS OFF)	TBD	TBD	mA
GPRS data transfer	TBD	TBD	mA
LTE data transfer	TBD	TBD	mA
GSM voice call	TBD	TBD	mA
GPRS data transfer (GNSS OFF)	TBD	TBD	mA

Table 35: The Module GNSS Current Consumption

EG915U-EU			
Description	**Conditions**	**Typ.**	**Unit**
Searching **(AT+CFUN=0)**	Cold Start @ Passive Antenna	TBD	mA
	Hot Start @ Passive Antenna	TBD	mA
	Lost State @ Passive Antenna	TBD	mA
Tracking **(AT+CFUN=0)**	Open Sky @ Passive Antenna	TBD	mA

6.4. ESD

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module, for example, ESD protection should be added at the interface of circuit design and the points that are vulnerable to electrostatic discharge damage or influence; anti-static gloves should be worn during production, etc.

ESD characteristics of the module's pins are as follows:

Table 36: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)

Tested Interfaces	**Contact Discharge**	**Air Discharge**	**Unit**

VBAT, GND	±TBD	±TBD	kV
All Antenna Interfaces	±TBD	±TBD	kV
Other Interfaces	±0.5	±1	kV

6.5. Operating and Storage Temperatures

Table 37: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-35	+25	+75	°C
Extended Operating Temperature Range [5]	-40	-TBD	+85	°C
Storage temperature range	-40	-TBD	+95	°C

[4] Within operating temperature range, the module is 3GPP compliant.
[5] Within extended operating temperature range, proper mounting, heating sinks and active cooling may be required to make certain functions of the module such as voice, SMS, data transmission to be realized. Only one or more parameters like Pout might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

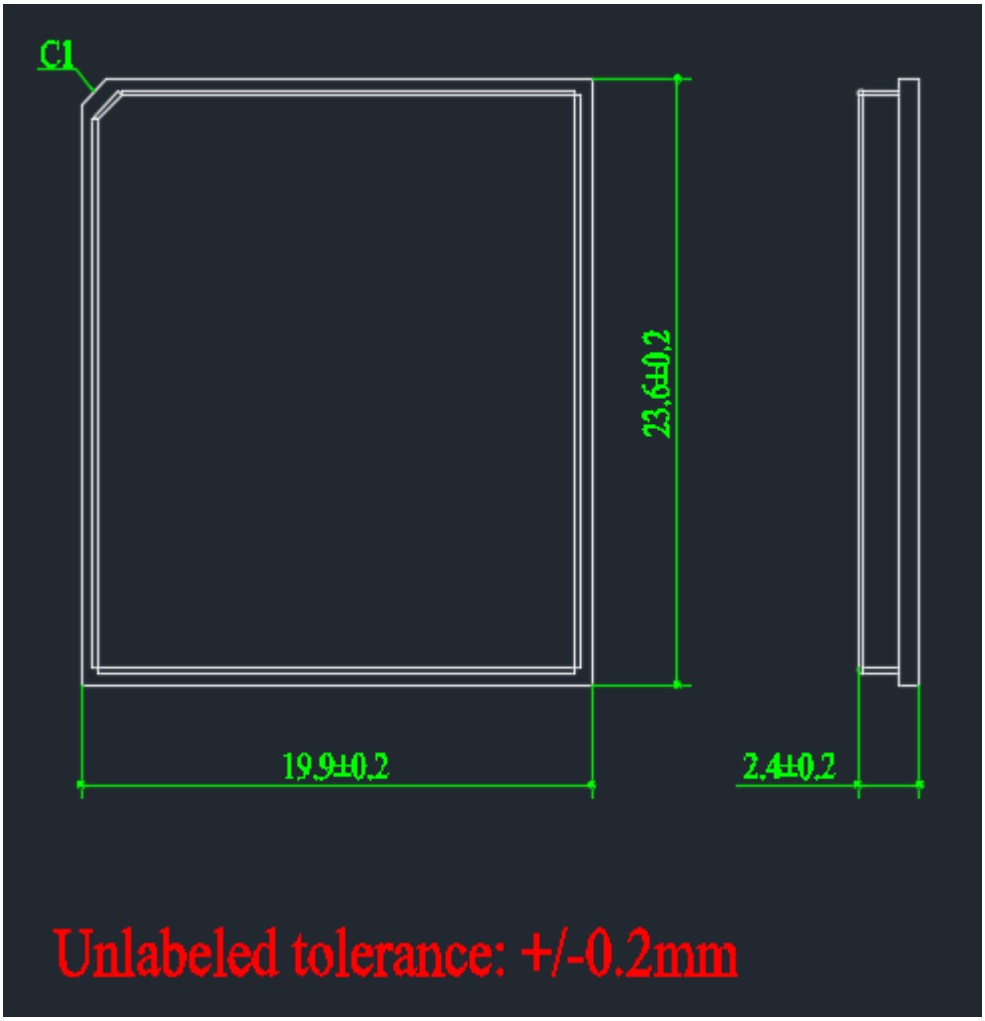


Figure 35: Module Top and Side Dimensions (Unit: mm)

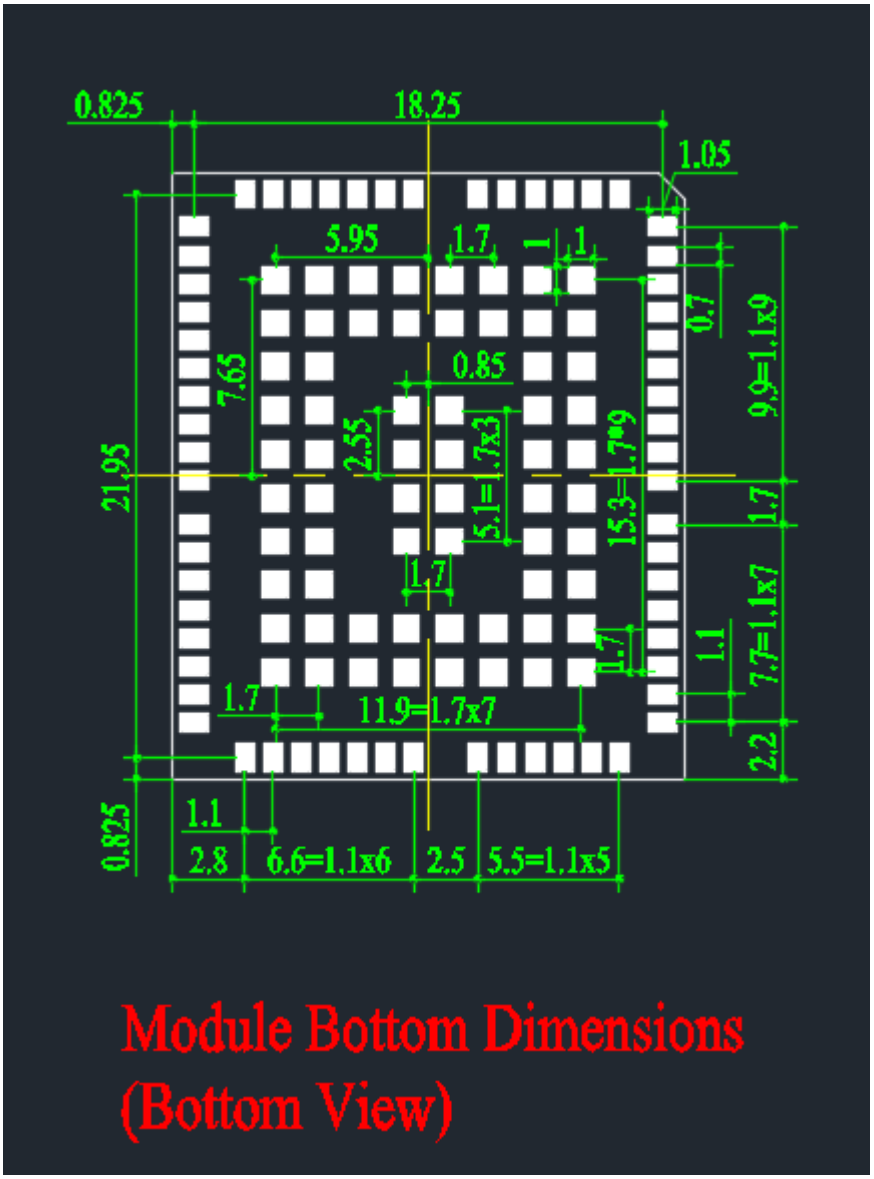


Figure 36: Module Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

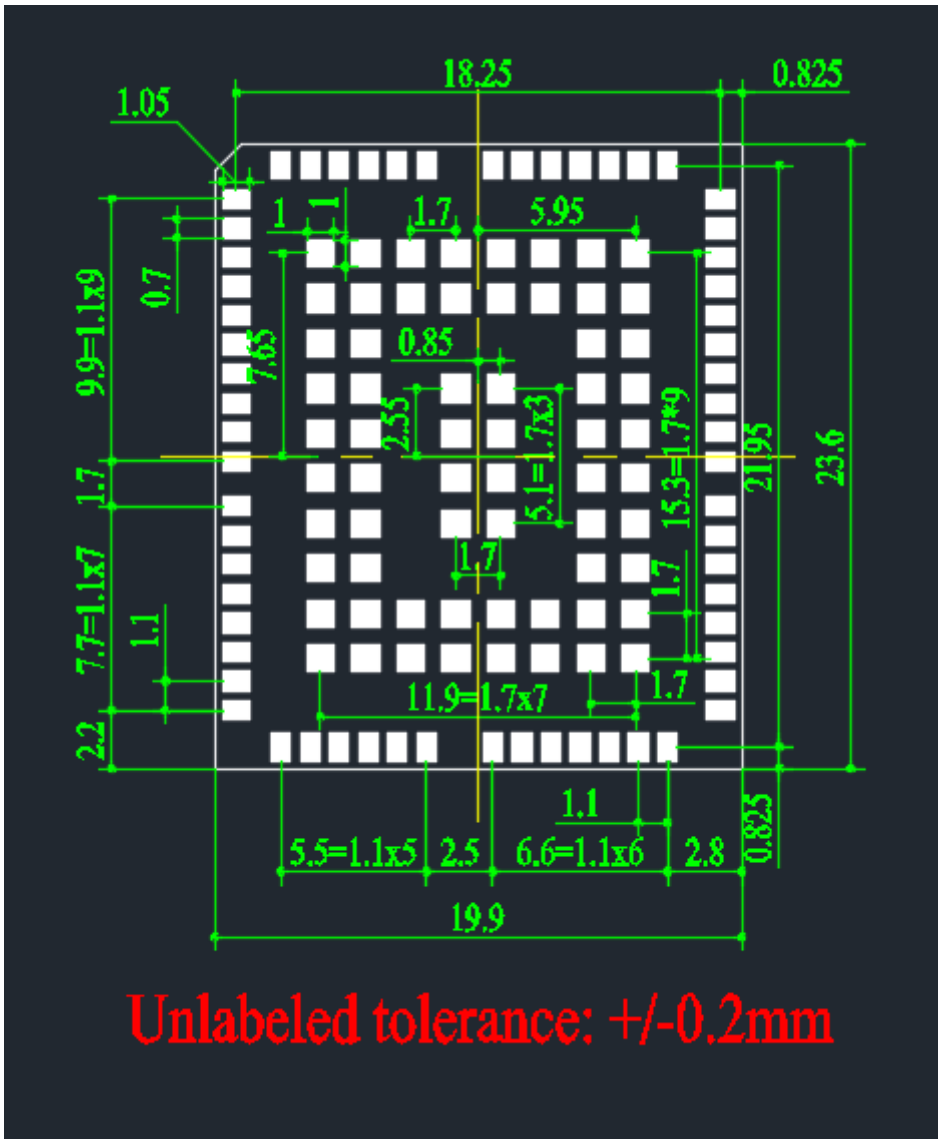


Figure 37: Recommended Footprint (TOP View)

NOTE

For convenient maintenance of the module, please keep about 3 mm between the module and other components on the host PCB.

7.3. Top and Bottom Views

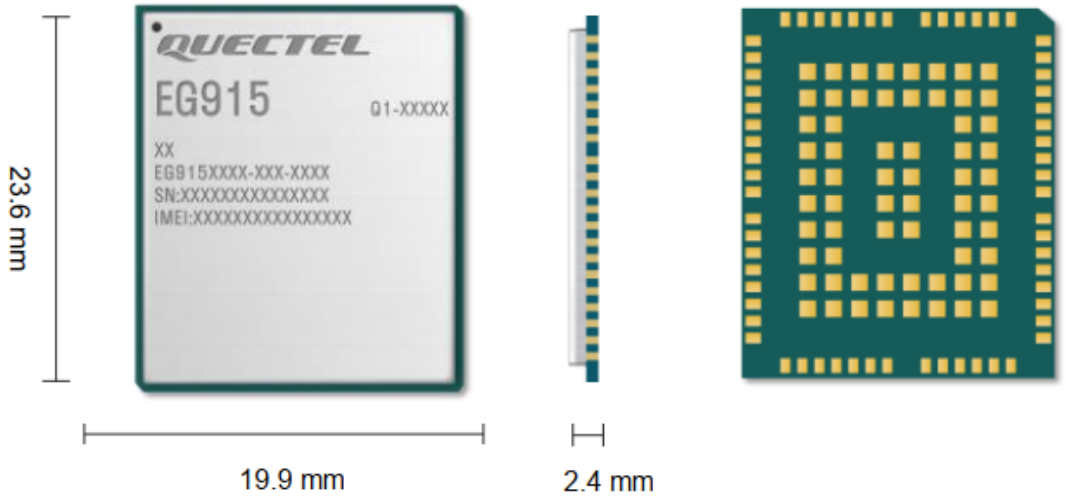


Figure 38: Top & Bottom Views of the Module

NOTE

These are renderings of the module. For authentic appearance, please refer to the module that you receive from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed package. MSL of the module is rated as 3, and its storage restrictions are shown as below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 24 hours [6] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 24 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:
   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.

NOTE

1. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60 %, it is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
2. Take the module out of the packaging and put it on high-temperature resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18 mm – 0.20 mm. For more details, please refer to ***document [4].[1]***

It is suggested that the peak reflow temperature is 238–246 °C, and the absolute maximum reflow temperature is 246 °C. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

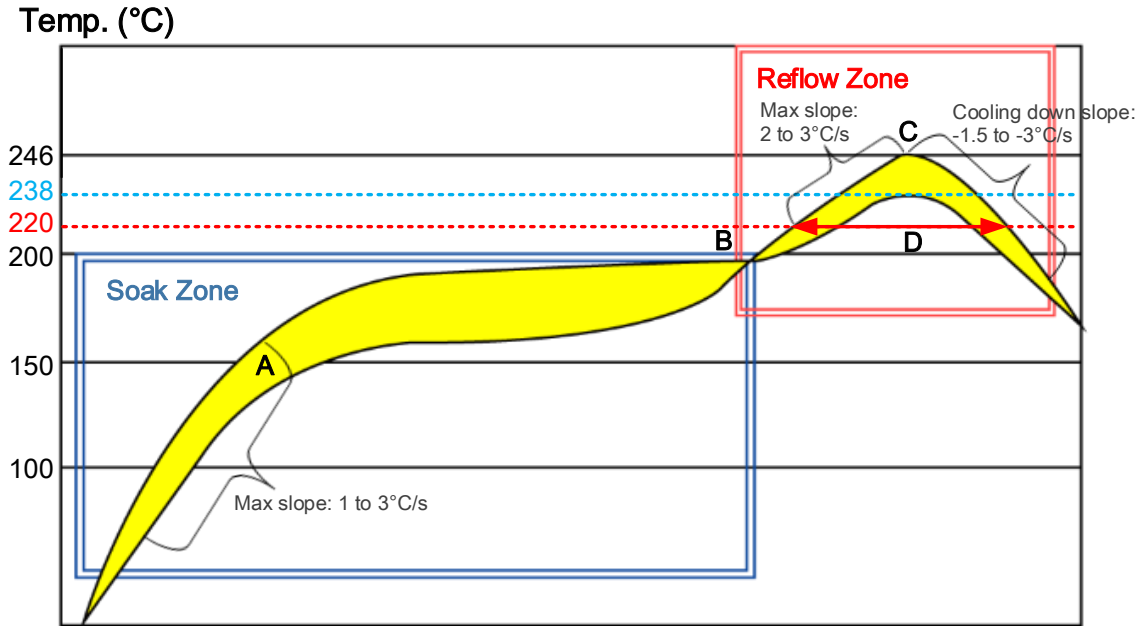


Figure 39: Recommended Reflow Soldering Thermal Profile

Table 38: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70 to 120 s

Reflow Zone	
Max slope	2 to 3 °C/s
Reflow time (D: over 220 ℃)	45 to 70 s
Max temperature	238 to 246 °C
Cooling down slope	-1 to 4 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

8.3. Packaging Specifications

The module is packaged in tape and reel carriers. One reel is 300 mm long and contains 250 modules. The figures below show the package details, measured in mm.

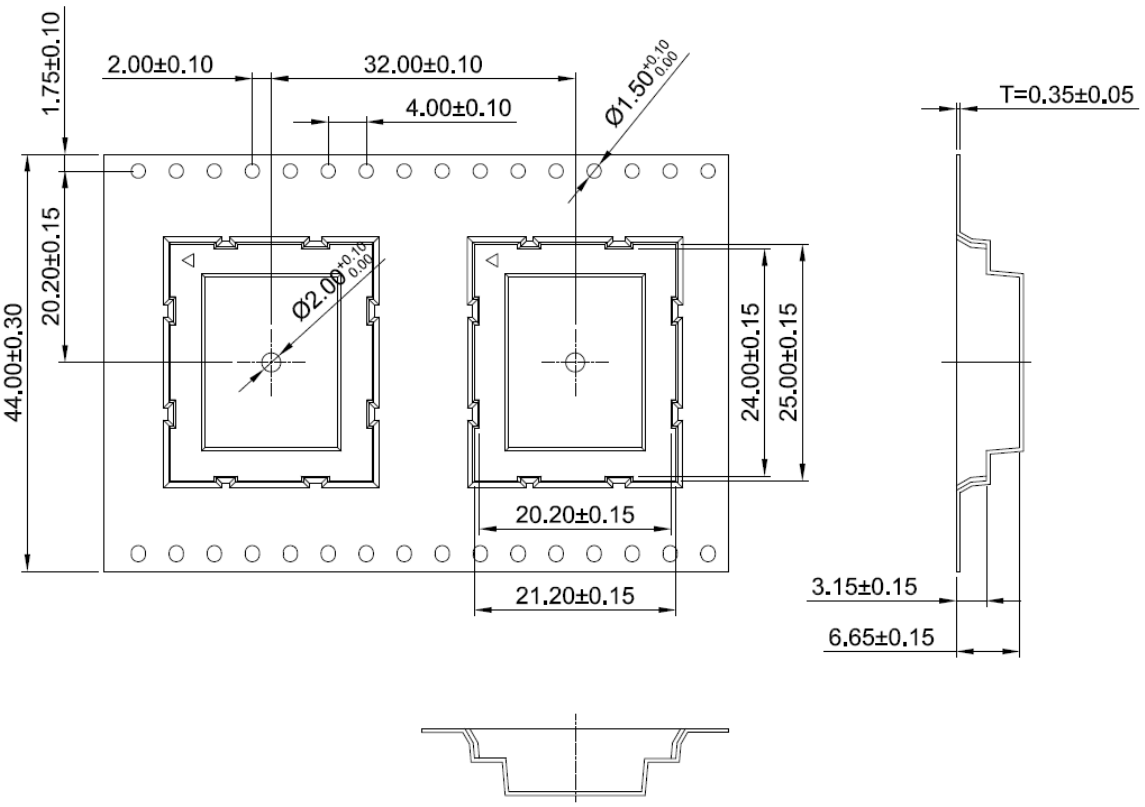


Figure 40: Tape Specifications

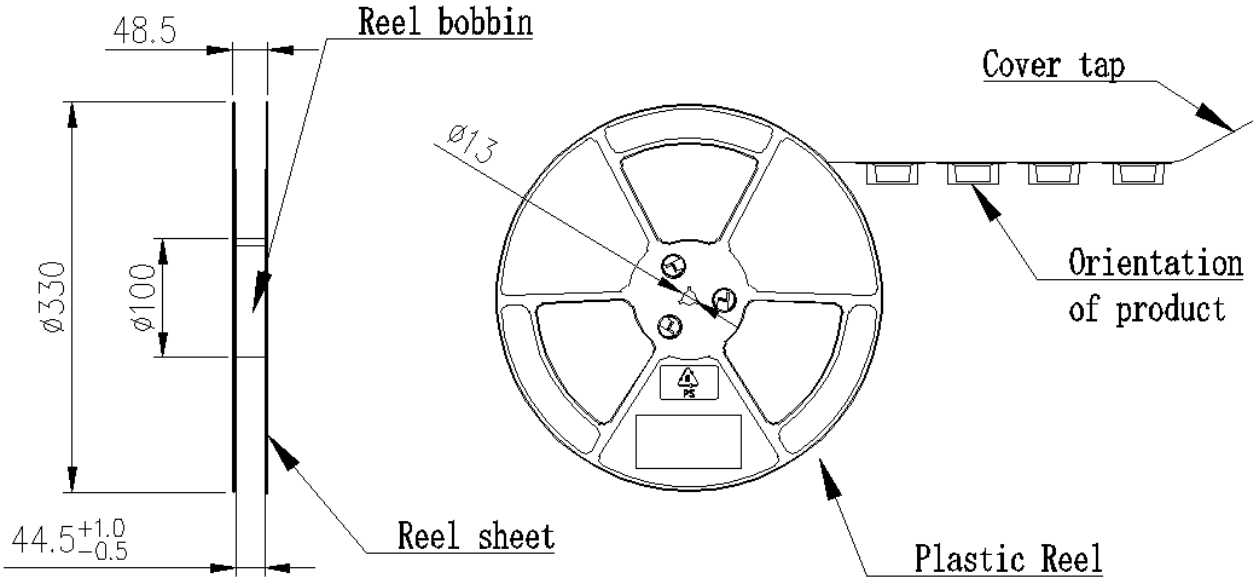


Figure 41: Reel Specifications

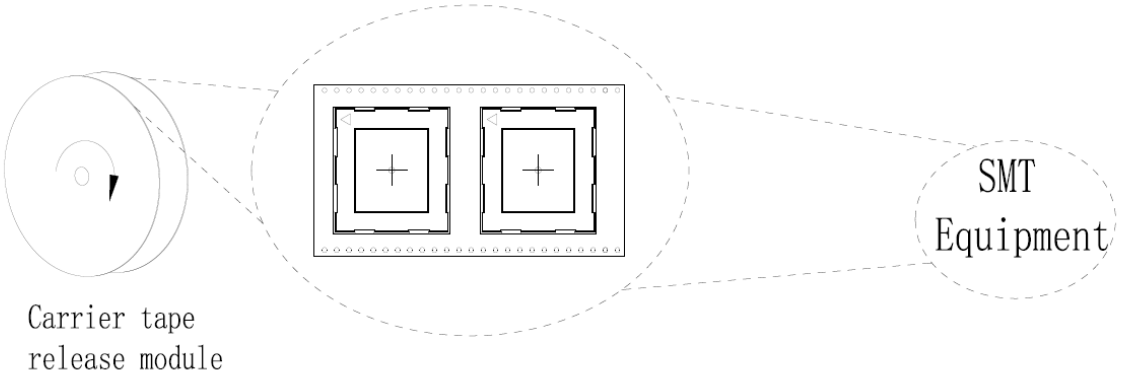


Figure 42: Tape and Reel Directions

9 Appendix References

Table 39: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EG915U-EU_Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_SMT_User_Guide

Table 40: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AON	Active Optical Network
AP	Application Processor
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CS2	Commercial Sample II

CTS	Clear To Send
DAI	Digital Audio Interface
DCE	Data Communications Equipment
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception
DRX	Diversity Receive
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FEM	Front-End Module
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Downlink Packet Access

HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
Inorm	Normal Current
LAA	License Assisted Access
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array
LMHB	Low/Middle/High Band
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control
MB	Middle Band
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/Output
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio

NSA	Non-Stand Alone
PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SCS	Sub-Carrier Space
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mount Device

SMS	Short Message Service
SoC	System on a Chip
SPI	Serial Peripheral Interface
STB	Set Top Box
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UHB	Ultra High Band
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
$V_{I}max$	Absolute Maximum Input Voltage Value

$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network