DRV2511-Q1 适用于螺线管和音圈的 8A 汽车类触觉驱动器

1 特性

- 宽工作电压范围 (4.5V - 26V)
- 能够处理 30V 电压
- 大电流驱动（峰值电流达 8A）
- 低 $R_{DS(on)}$，完整 H 桥输出
- 集成故障保护
  - 短路保护
  - 过热保护
  - 过压和欠压保护
  - 故障报告
- 模拟输入
- 专用中断引脚
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B

2 应用

- 电磁致动器驱动器
  - 音圈
  - 螺线管
- 机械按钮替代产品
- 汽车类触觉 应用
  - 信息娱乐
  - 中央控制台
  - 方向盘
  - 车门板
  - 座椅

3 说明

DRV2511-Q1 器件是一款专为感性负载（例如，螺线管和音圈）而设计的大电流触觉驱动器。

输出级含一个完整 H 桥，能够提供 8A 峰值电流。

DRV2511-Q1 器件提供欠压闭锁、过流保护和过热保护等多种保护功能。

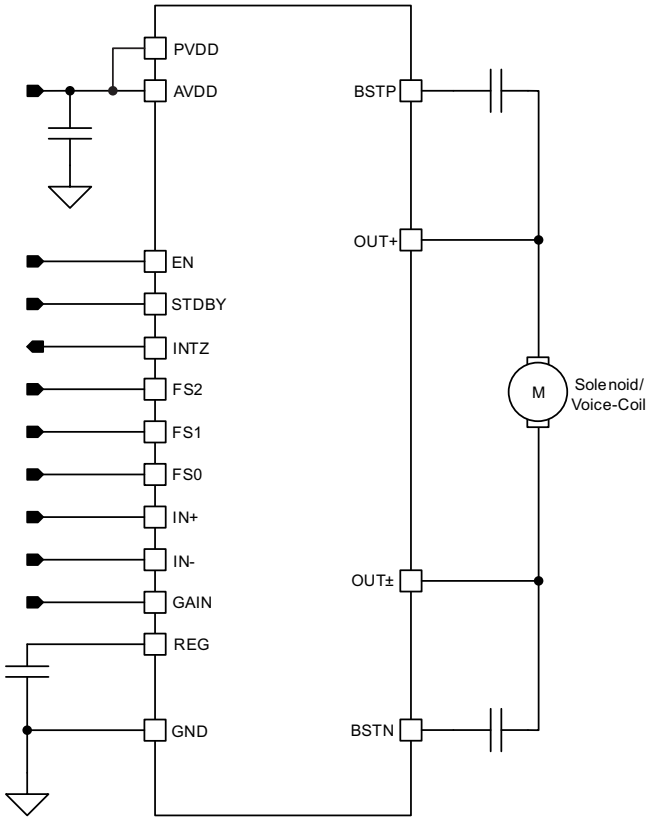
DRV2511-Q1 器件符合汽车类产品标准。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DRV2511-Q1	HTSSOP (32)	11 mm x 6.20 mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 4
6.1 Absolute Maximum Ratings 4
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 4
6.5 Electrical Characteristics 6
6.6 Switching Characteristics 6
6.7 Typical Characteristics 7
7 **Detailed Description** 8
7.1 Overview 8
7.2 Functional Block Diagram 8
7.3 Feature Description 9
7.4 Device Functional Modes 11
7.5 Programming 11
8 **Application and Implementation** 12
8.1 Application Information 12
8.2 Typical Applications 12
9 **Power Supply Recommendations** 16
10 **Layout** 16
10.1 Layout Guidelines 16
10.2 Layout Example 16
11 器件和文档支持 17
11.1 器件支持 17
11.2 商标 17
11.3 静电放电警告 17
11.4 Glossary 17
12 机械、封装和可订购信息 18

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (June 2016) to Revision A	**Page**
• 发布为量产数据。	1

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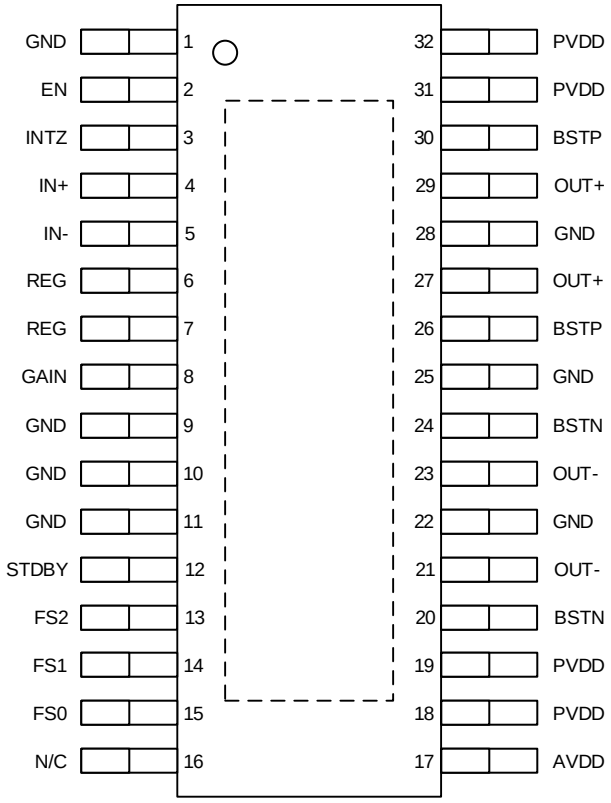
5 Pin Configuration and Functions

DAP Package
32-Pin HTSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1, 9, 10, 11, 22, 25, 28	P	Ground.
EN	2	I	Device enable pin.
INTZ	3	O	General fault reporting. Open drain. INTZ = High, normal operation INTZ = Low, fault condition
IN+	4	I	Positive differential input.
IN-	5	I	Negative differential input.
REG	6, 7	P	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the MODE resistor divider.
GAIN	8	I	Selects Gain.
STDBY	12	I	Standby pin.
FS2	13	I	Output switching frequency selection.
FS1	14	I	Output switching frequency selection.
FS0	15	I	Output switching frequency selection.
N/C	16	N/C	Pin should be left floating.
AVDD	17	P	Analog Supply, can be connected to VBAT for single power supply operation.
PVDD	18, 19, 31, 32	P	Power supply.
BSTN	20, 24	P	Boot strap for negative output, connect to 220 nF X5R, or better ceramic cap to OUT-.
OUT-	21, 23	O	Negative output.
BSTP	26, 30	P	Boot strap for positive output, connect to 220 nF X5R, or better ceramic cap to OUT+.

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUT+	27, 29	O	Positive output.
Thermal Pad or PowerPAD™		G	Connect to GND for best system performance. If not connected to GND, leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	PVDD, AVDD	–0.3	30	V
Input voltage, V_I	IN+, IN-	–0.3	6.3	V
	GAIN	–0.3	VREG + 0.3	
	EN	–0.3	PVDD + 0.3	
Current	DC current on PVDD, GND, OUT+, OUT-	–8	8	A
Operating free-air temperature, T_A		–40	125	°C
Storage temperature range, T_{stg}		–50	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–450	450	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage. PVDD, AVDD.	4.5		26	V
V_{IH}	High-level input voltage. STDBY, EN, FS0, FS1, FS2.	2			V
V_{IL}	Low-level input voltage. STDBY, EN, FS0, FS1, FS2.			0.8	V
V_{OL}	Low-level output voltage. INTZ, $R_{PULL-UP}$ = 100 kΩ, PVDD = 26 V.			0.8	V
I_{IH}	High-level input current. STDBY, EN, FS0, FS1, FS2. (V_I = 2 V, PVDD = 26 V).			50	µA
R_L	Minimum load Impedance.		1.65		Ω
L_o	Output-filter Inductance.	1			µH

6.4 Thermal Information

THERMAL METRIC (1)		DRV2511-Q1 DAP 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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Thermal Information (continued)

THERMAL METRIC(1)		DRV2511-Q1 DAP 32 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	17.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1	°C/W

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6.5 Electrical Characteristics

T_A = 25°C, AVCC = PVDD = 12 V, R_L = 5 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB		1.5	15	mV
I_{VDD}	Quiescent supply current	No load or filter		20		mA
$I_{VDD(SD)}$	Quiescent supply current in shutdown mode	No load or filter		35		µA
$I_{VDD(STDBY)}$	Quiescent supply current in standby mode	No load or filter		11		mA
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	T_J = 25°C		60		mΩ
G	Gain	R1 = open, R2 = 20 kΩ	19	20	21	dB
		R1 = 100 kΩ, R2 = 20 kΩ	25	26	27	
		R1 = 100 kΩ, R2 = 39 kΩ	31	32	33	dB
		R1 = 75 kΩ, R2 = 47 kΩ	35	36	37	
V_{REG}	Regulator voltage		6.4	6.9	7.4	V
BW	Full Power Bandwidth			60		kHz
V_O	Output voltage (measured differentially)	Measured at PVDD = 26V		50		V
PSRR	Power supply ripple rejection	200 mVpp ripple at 1 kHz, Gain = 20 dB		–70		dB
CMRR	Common-mode rejection ratio			–56		dB
f_{OSC}	Oscillator frequency (with PWM duty cycle < 96%)	FS2 = 0, FS1 = 0, FS0 = 0	376	400	424	kHz
		FS2 = 0, FS1 = 0, FS0 = 1	470	500	530	
		FS2 = 0, FS1 = 1, FS0 = 0	564	600	636	
		FS2 = 0, FS1 = 1, FS0 = 1	940	1000	1060	
		FS2 = 1, FS1 = 0, FS0 = 0	1128	1200	1278	
	Power-on threshold			4.1		V
	Power-off threshold			28		V
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C
	Over-current trip point			13		A
	Over-voltage trip point			28		V

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on-sd}	Turn-on time from shutdown to waveform	EN = Low to High, STBY = Low		10		ms
t_{OFF-sd}	Turn-off time	EN = High to Low		5		µs
$t_{on-stdby}$	Turn-on time from standby to waveform	EN = High, STBY = High to Low		6		µs

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6.7 Typical Characteristics

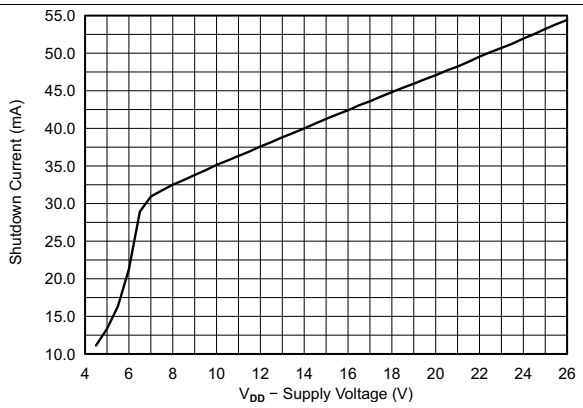


图 1. Shutdown Current vs VDD Voltage

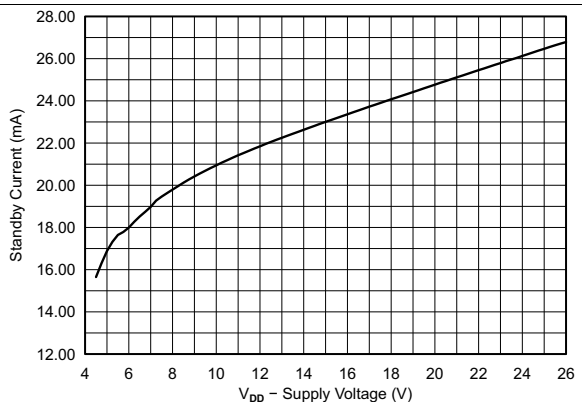


图 2. Standby Current vs VDD Voltage

7 Detailed Description

7.1 Overview

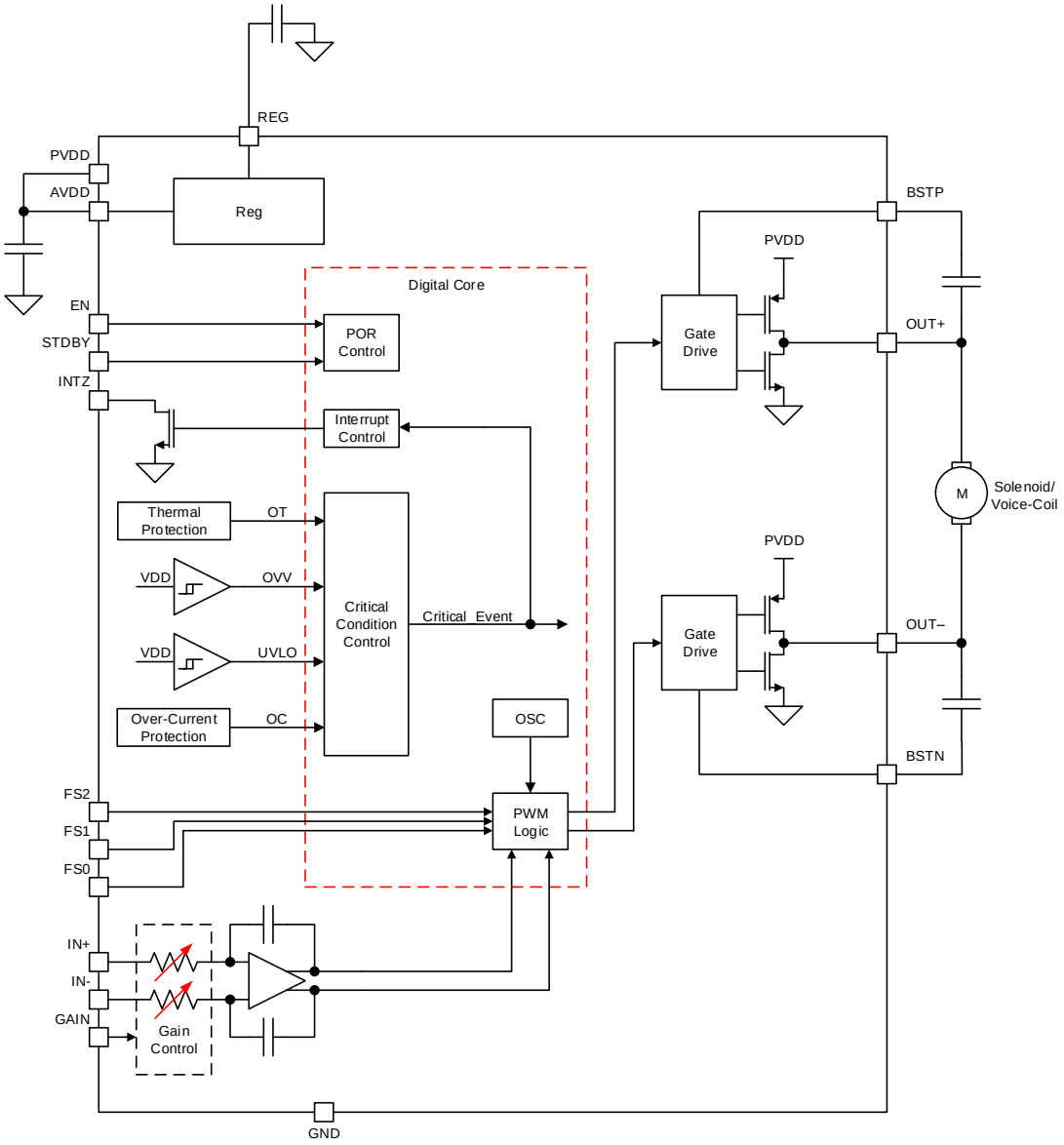
The DRV2511-Q1 device is a high current haptic driver specifically designed for inductive loads, such as solenoids and voice coils.

The output stage consists of a full H-bridge capable of delivering 8 A of peak current.

The design uses an ultra-efficient switching output technology developed by Texas Instruments, but with features added for the automotive industry. The DRV2511-Q1 device provides protection functions such as undervoltage lockout, over-current protection and over-temperature protection. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system.

The DRV2511-Q1 device is automotive qualified.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Analog Input and Configurable Pre-amplifier

The DRV2511-Q1 device features a differential input stage that cancels common-mode noise that appears on the inputs. The DRV2511-Q1 device also features four gain settings that are configurable via external resistors.

表 1. Gain Configuration Table

GAIN	R1	R2	INPUT IMPEDANCE
20 dB	5.6 kΩ	open	60 kΩ
26 dB	20 kΩ	100 kΩ	30 kΩ
32 dB	39 kΩ	100 kΩ	15 kΩ
36 dB	47 kΩ	75 kΩ	9 kΩ

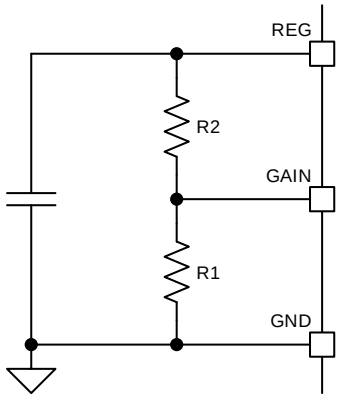

图 3. Gain Configuration

7.3.2 Pulse-Width Modulator (PWM)

The DRV2511-Q1 device features BD modulation scheme with high bandwidth, low noise, low distortion, and excellent stability.

The BD modulation scheme allows for smaller ripple currents through the load. Each output switches from 0 V to the supply voltage. With no input, the OUT+ and OUT- pins are in phase with each other so that there is little or no current in the load. For positive differential inputs, the duty cycle of OUT+ is greater than 50% and the duty cycle of OUT- is lower than 50% for a positive differential output voltage. The opposite is true for negative differential inputs. The voltage accross the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces the I^2R losses in the load.

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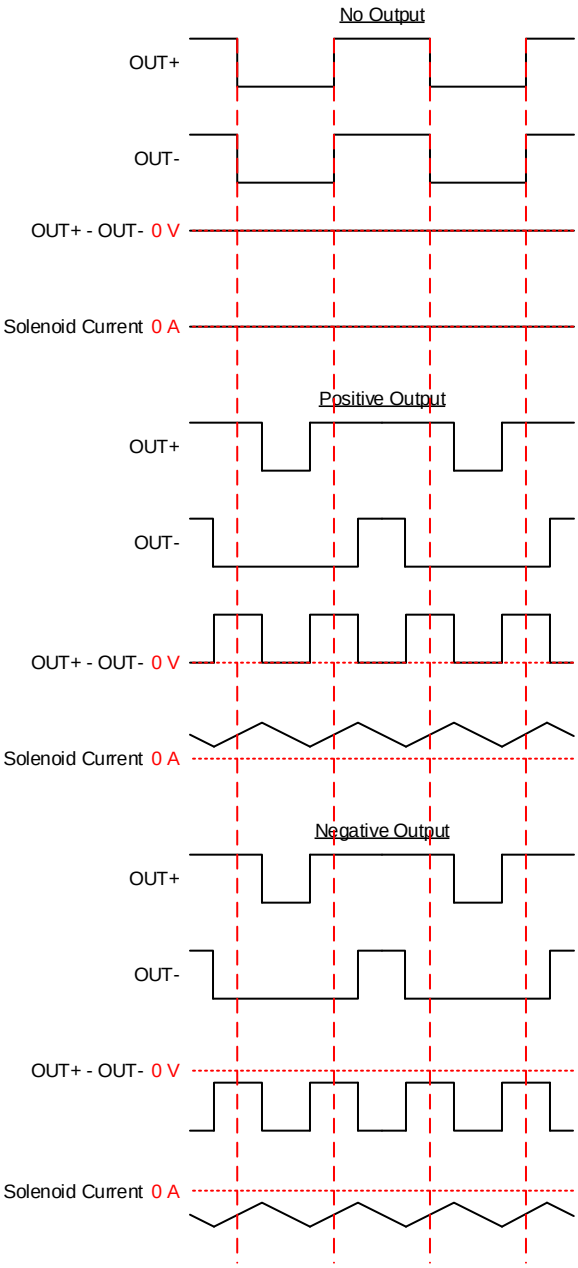

图 4. BD Mode Modulation

7.3.3 Designed for low EMI

The DRV2511-Q1 device design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces EMI that results from current passing from the die to the system PCB. The design incorporates circuitry that optimizes output transitions that causes EMI. Follow the recommended design requirements in the *Design Requirements* section.

7.3.4 Device Protection Systems

The DRV2511-Q1 device features a complete set of protection circuits carefully designed to protect the device against permanent failures due to shorts, over-temperature, over-voltage, and under-voltage scenarios. The INTZ pin signals if an error is detected.

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表 2. Fault Reporting Table

FAULT	TRIGGERING CONDITION	INTZ	ACTION	LATCH?
Over-current	Output short or short to PVDD or GND	pulled low	output in high impedance	Latched
Over-temperature	T_j > 150 ºC	pulled low	output in high impedance	Latched
Under-voltage	PVDD < 4.5 V	-	output in high impedance	Self-clearing
Over-voltage	PVDD > 27 V	-	output in high impedance	Self-clearing

When the "Latched" conditions happen, the device must be reset with the EN signal in order to clear the fault. If automatic recovery from these conditions is desired, connect the INTZ pin directly to the EN pin. This allows the INTZ pin function to automatically drive the EN pin low which clears the latched condition.

7.4 Device Functional Modes

The DRV2511-Q1 device has multiple power states to optimize power consumption.

7.4.1 Operation in Shutdown Mode

The NRST pin of the DRV2511-Q1 device puts the device in a shutdown mode. When NRST is asserted (logic low), all internal blocks of the device are off to achieve ultra low power.

7.4.2 Operation in Standby Mode

The STDBY pin of the DRV2511-Q1 device puts the device in a standby mode. When STDBY is asserted (logic high), some internal blocks of the device are off to achieve low power while preserving the ability to wake up quickly to achieve low latency waveform playback.

7.4.3 Operation in Active Mode

The DRV2511-Q1 device is in active mode when it has a valid supply, and it is not in either shutdown or standby modes. In this mode the DRV2511-Q1 device is fully on and reproducing at the output the input times the gain.

7.5 Programming

7.5.1 Gain

The DRV2511-Q1 device has a configurable gain that is controlled through external resistors. Please see the Analog Input and Configurable Pre-amplifier section for more details.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV2511-Q1 device is a high-efficiency driver for inductive loads, such as solenoids and voice-coils. The typical use of the device is on haptic applications where short, strong waveforms are desired to create a haptic event that will be coming from the application processor.

8.2 Typical Applications

8.2.1 Single-Ended Source

To use the DRV2511-Q1 with a single-ended source, apply either a voltage divider to bias INB to 3 V, tie to GND or use a 0.1-μF cap from INB to GND to have the device self bias. Apply the single-ended signal to the INA pin.

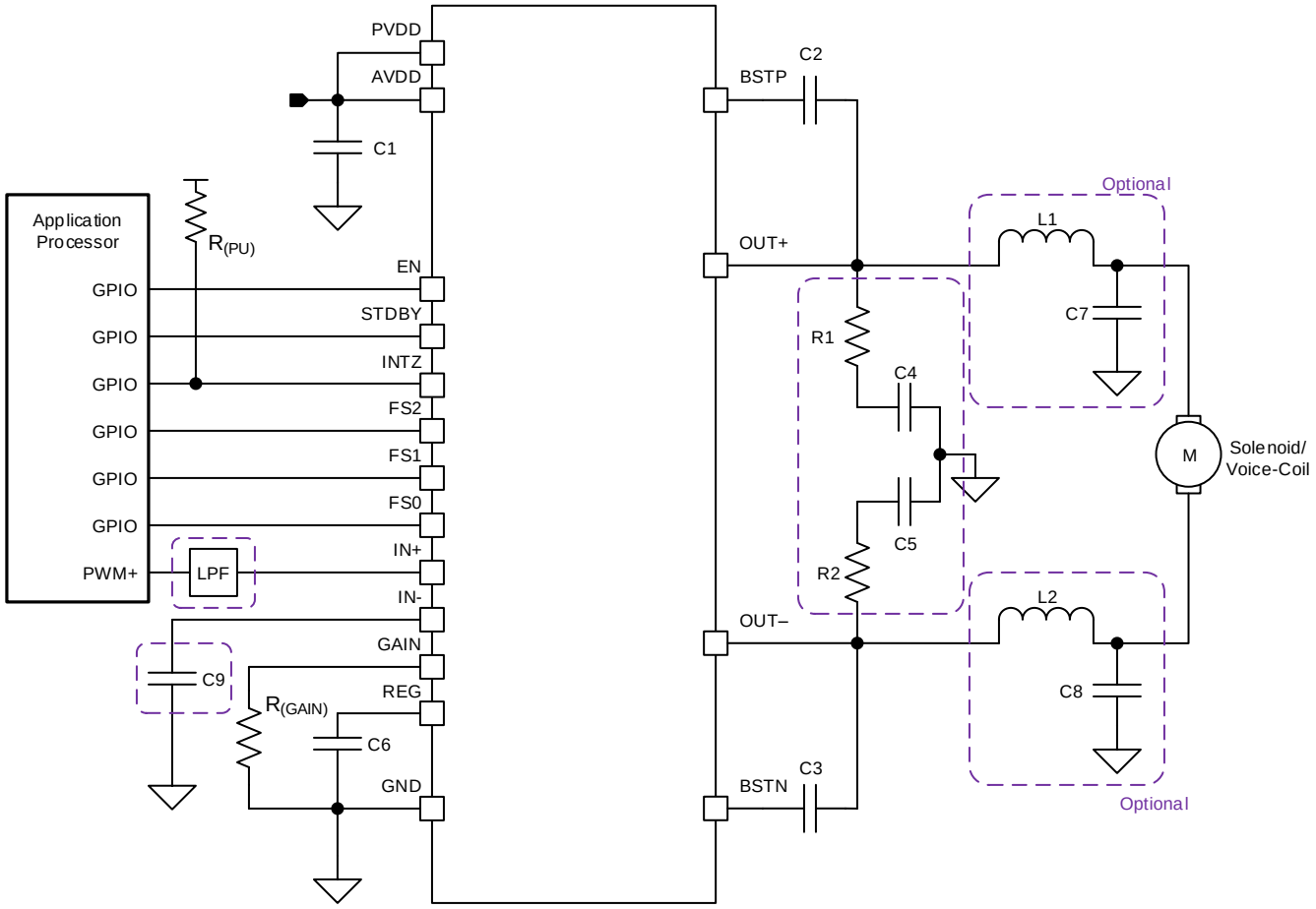

图 5. Typical Application Schematic

8.2.1.1 Design Requirements

For most applications the following component values found in 表 3 below can be used.

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Typical Applications (接下页)

表 3. Component Requirements Table

COMPONENT	DESCRIPTION	SPECIFICATION	TYPICAL VALUE
C1	Supply capacitor	Capacitance	22 µF and 0.1 µF for PVDD & AVDD
C2/C3	Boost capacitor	Capacitance	0.22 µF
C4/C5	Output snubber capacitor	Capacitance	470 pF
C6	Regulator capacitor	Capacitance	1 µF
C9	Input decoupling capacitor	Capacitance	0.1 µF
R1/R2	Output snubber resistor	Resistance	3.3 Ω
$R_{(PU)}$	Pull-up resistor	Resistance	100 kΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Optional Components

Note that in the diagrams, there are a few optional external components. These optional external components may be needed in the application to meet EMI/EMC standards and specifications by filters necessary frequency spectrums.

8.2.1.2.2 Capacitor Selection

A bulk bypass capacitor should be mounted between VBAT and GND. The capacitance needs to be >22 uF with a X5R or better rating on the power pins to GND. Also include two ceramic capacitors in the ranges of 220 pF to 1 uF and 100 nF to 1 uF. The bootstrap capacitors, BSTA and BSTB, should be 220-nF ceramic capacitors of quality X5R or better rated for at least the maximum rating of the pin.

8.2.1.2.3 Solenoid Selection

The DRV2511-Q1 solenoid driver can accommodate a variety of solenoids. Solenoids should have an equivalent resistance of 1.6 Ω or greater. Solenoids with lower resistances are prone to driving high currents. A maximum peak current of 8-A should not be exceeded. The DRV2511-Q1 will go into a shutdown mode to protect itself from overcurrent.

8.2.1.2.4 Output Filter Considerations

The output filter is optional and is mainly for limiting peak currents. A second-order Butterworth low-pass filter with the cut-off frequency set to a few kilohertz should be sufficient. See 公式 2, 公式 3, and 公式 4 for example filter design.

$$H(s) = \frac{1}{s^2 + \sqrt{2}s + 1} \quad (1)$$

$$L_x = \frac{\sqrt{2} \times R_L}{2\omega_o} \quad (2)$$

$$2 \times C_F = \frac{\sqrt{2}}{2 \times \frac{R_L}{2} \times \omega_0} \quad (3)$$

$$\omega_0 = 2\pi \times f \quad (4)$$

8.2.1.3 Application Curves

These application curves were taken using an HA200 solenoid with a 100-g mass, and the acceleration was measured using the DRV-AAC16-EVM accelerometer. The following scales apply to the graphs:

- Output Differential Voltage scale is shown on the plots at 5-V/div
- Acceleration scale is 5.85-G/div
- Current scale is 2-A/div

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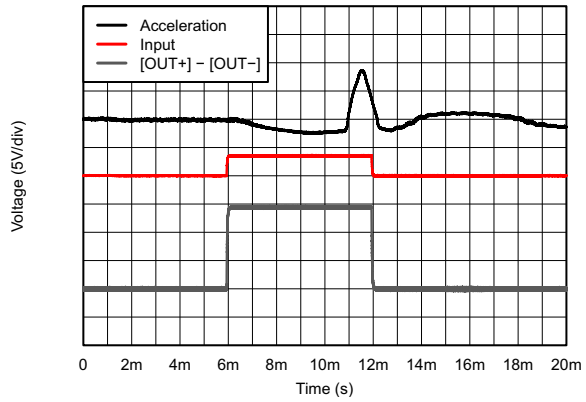

图 6. Voltage and Acceleration vs Time (Input Square Wave)

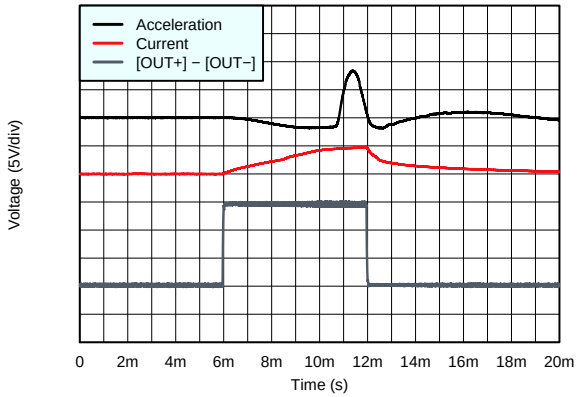

图 7. Voltage and Acceleration vs Time (Square Wave)

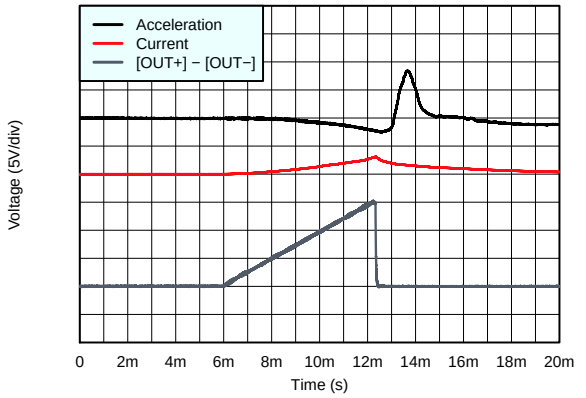

图 8. Voltage and Acceleration vs Time (Ramp Wave)

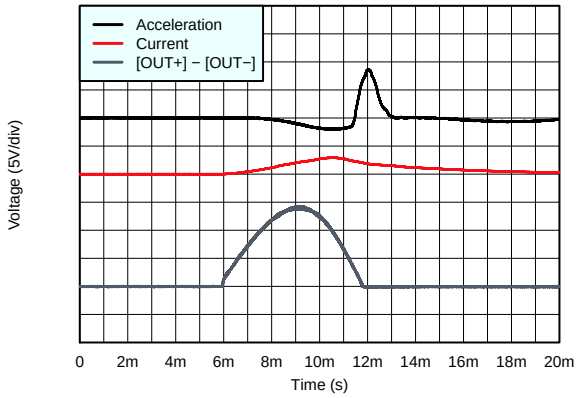

图 9. Voltage and Acceleration vs Time (1/2 Sine Wave)

8.2.1.4 Differential Input Diagram

To use the DRV2511-Q1 with a differential input source, apply both inputs differentially from a control source (GPIO, DAC, etc...).

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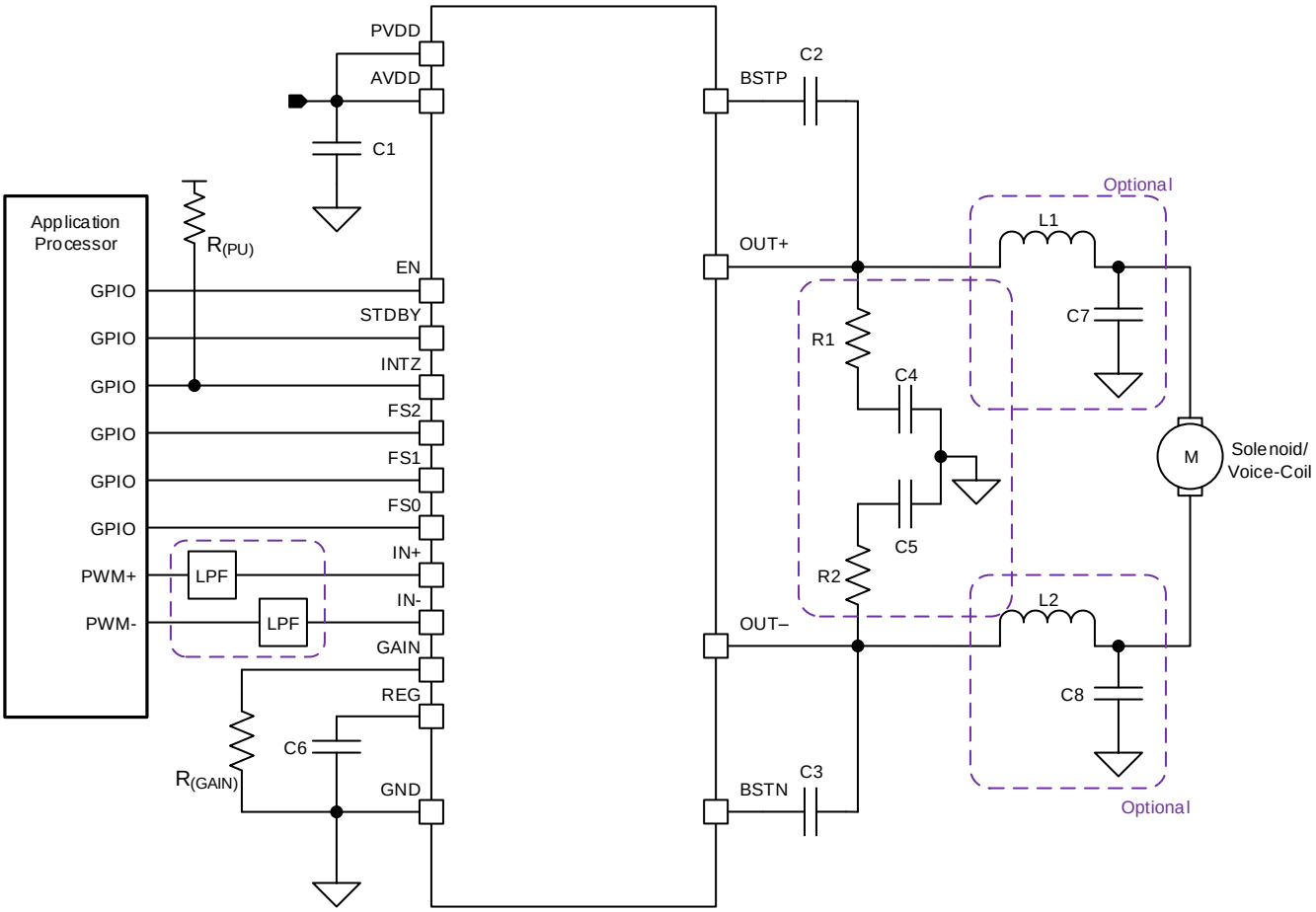

图 10. Typical Application Schematic

9 Power Supply Recommendations

The DRV2511-Q1 device operates from 4.5 V - 26 V and this supply should be able to handle high surge currents in order to meet the high currrent draws for haptics effects. Additionally the DRV2511-Q1 should have 22-µF and 0.1-µF ceramic capacitors near the PVDD & AVDD pins for additional decoupling from trace routing.

10 Layout

10.1 Layout Guidelines

The EVM layout optimizes for thermal dissipation and EMC performance. The DRV2511-Q1 device has a thermal pad down, and good thermal conduction and dissipation require adequate copper area. Layout also affects EMC performance. It is best practice to use the same/similiar layout as shown below in the DRV2511Q1EVM.

10.2 Layout Example

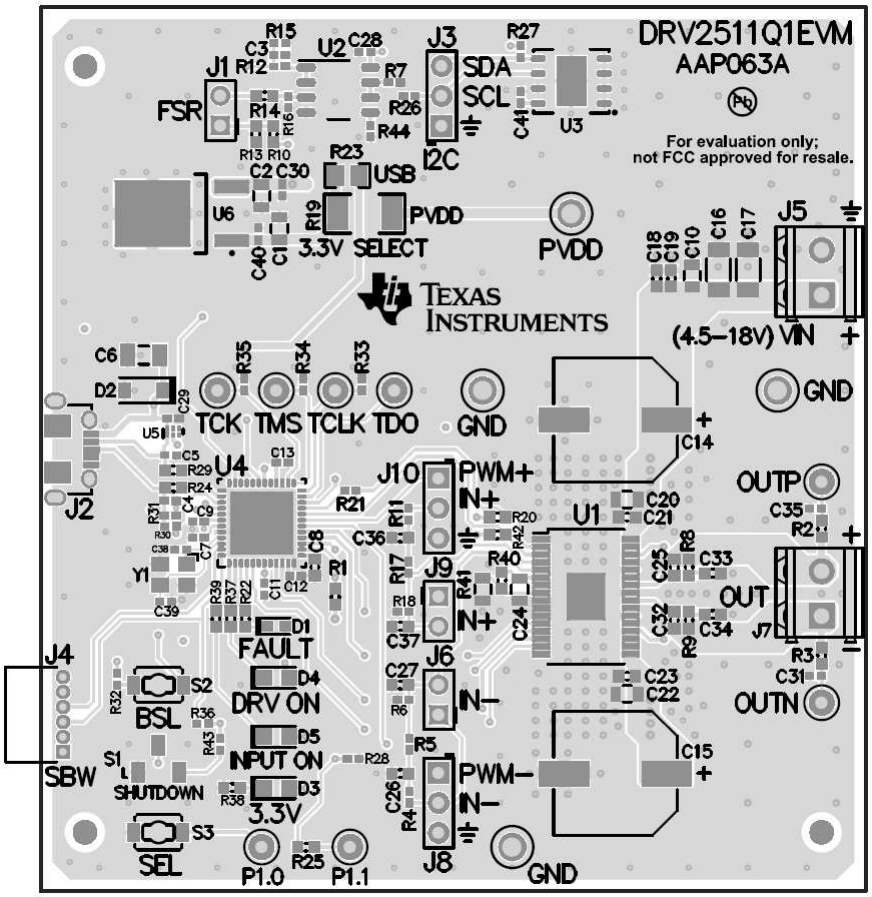

图 11. DRV2511-Q1 EVM

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11 器件和文档支持

11.1 器件支持

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11.3 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV2511QDAPRQ1	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV2511Q
DRV2511QDAPRQ1.A	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV2511Q

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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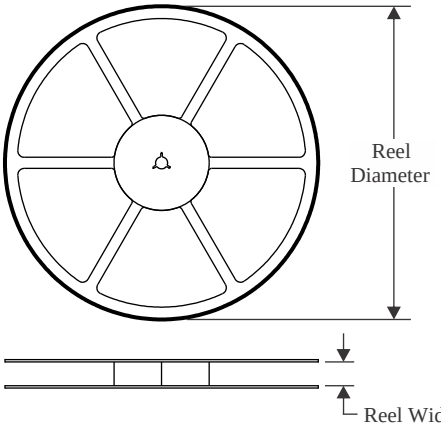
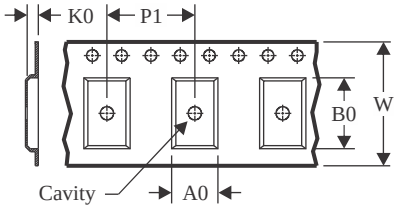
TAPE AND REEL INFORMATION

REEL DIMENSIONS

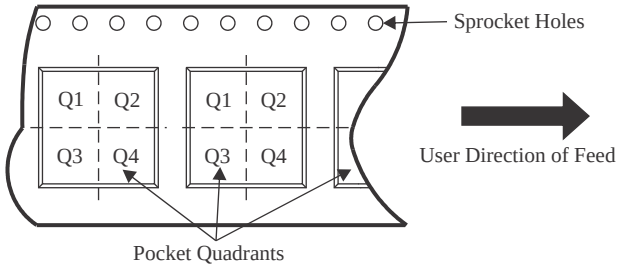


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

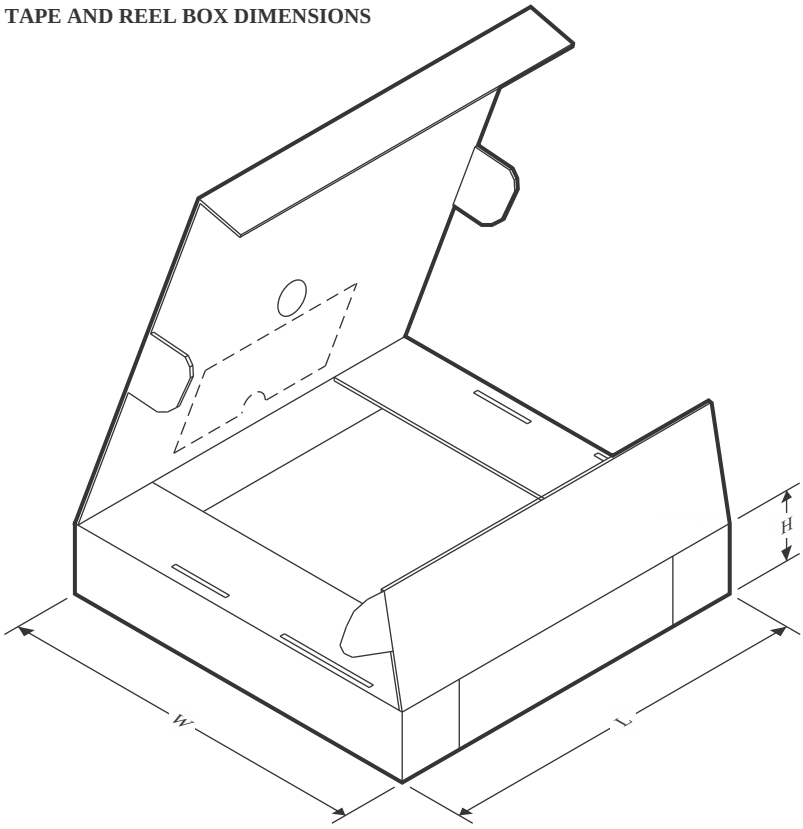
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2511QDAPRQ1	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2511QDAPRQ1	HTSSOP	DAP	32	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

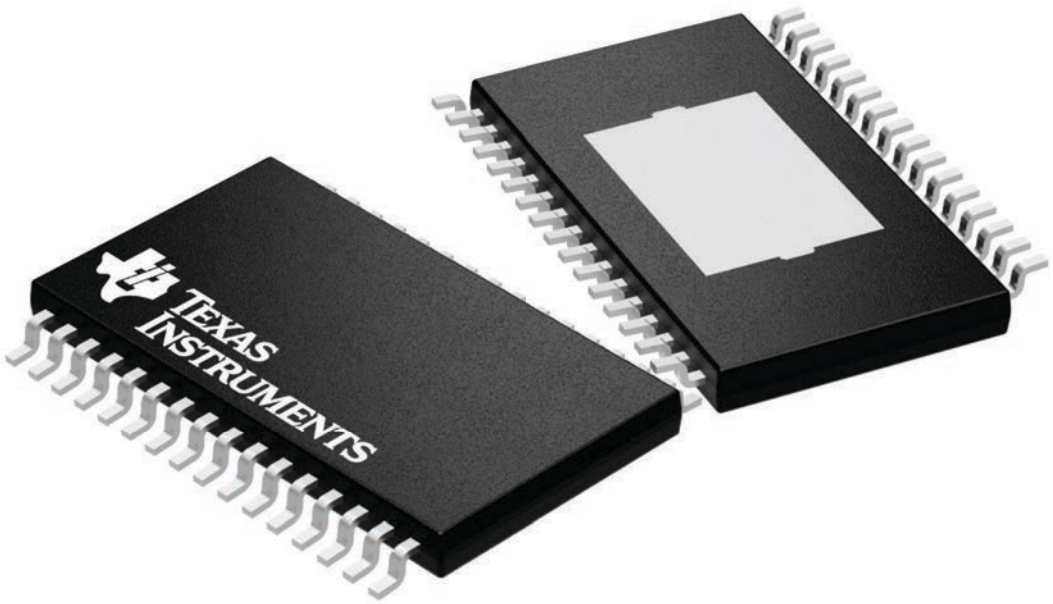
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

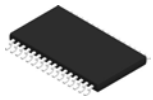
8.1 x 11, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

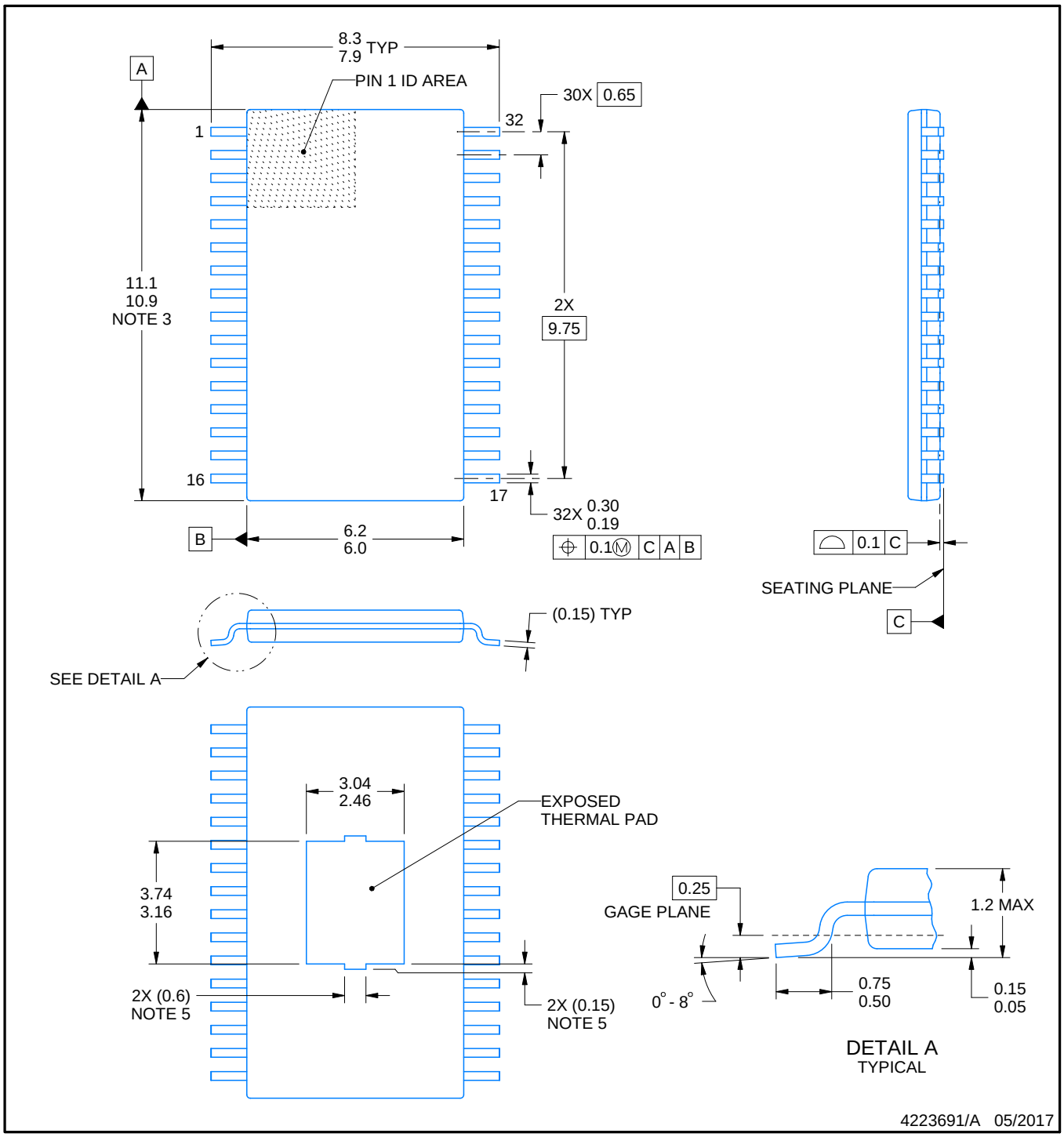


PACKAGE OUTLINE

DAP0032C

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



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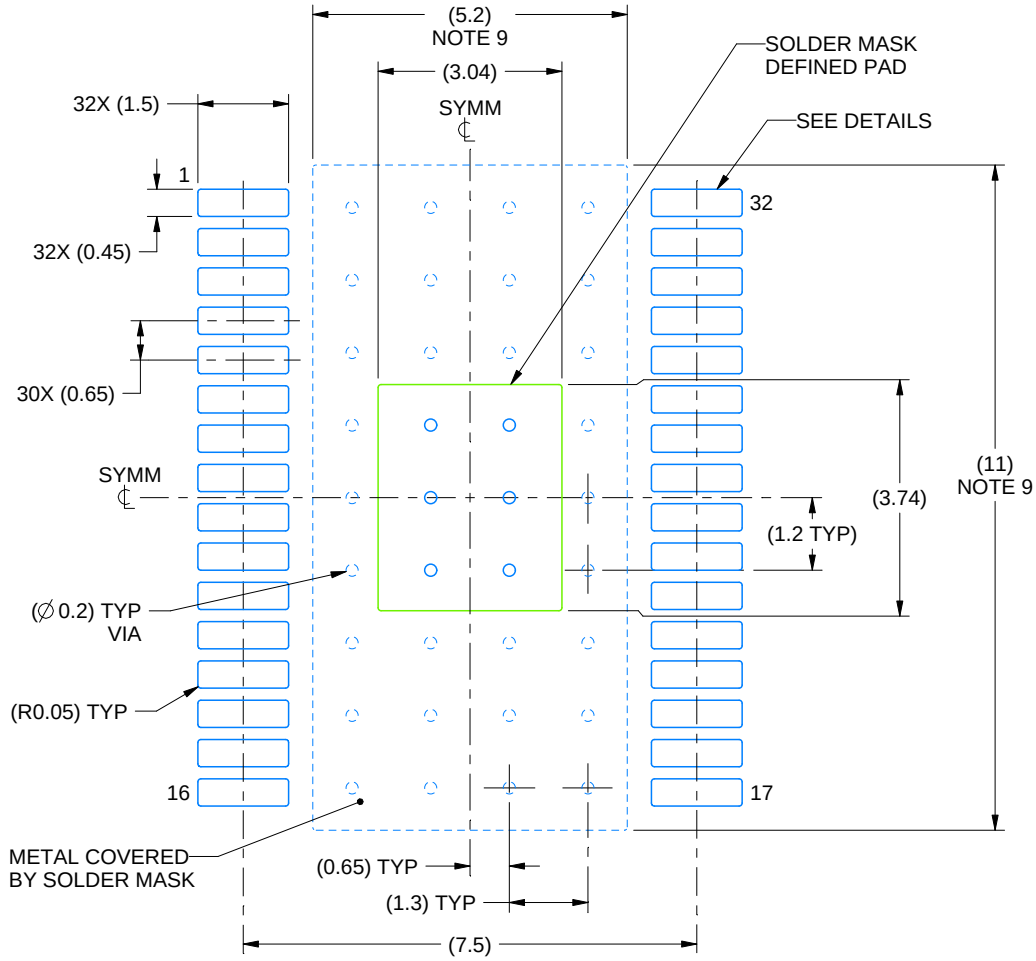
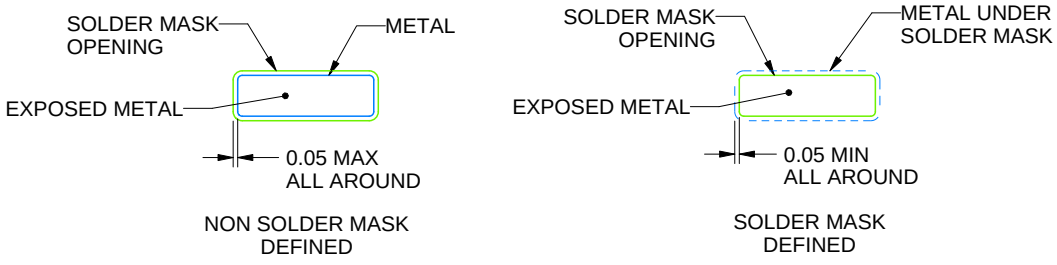
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

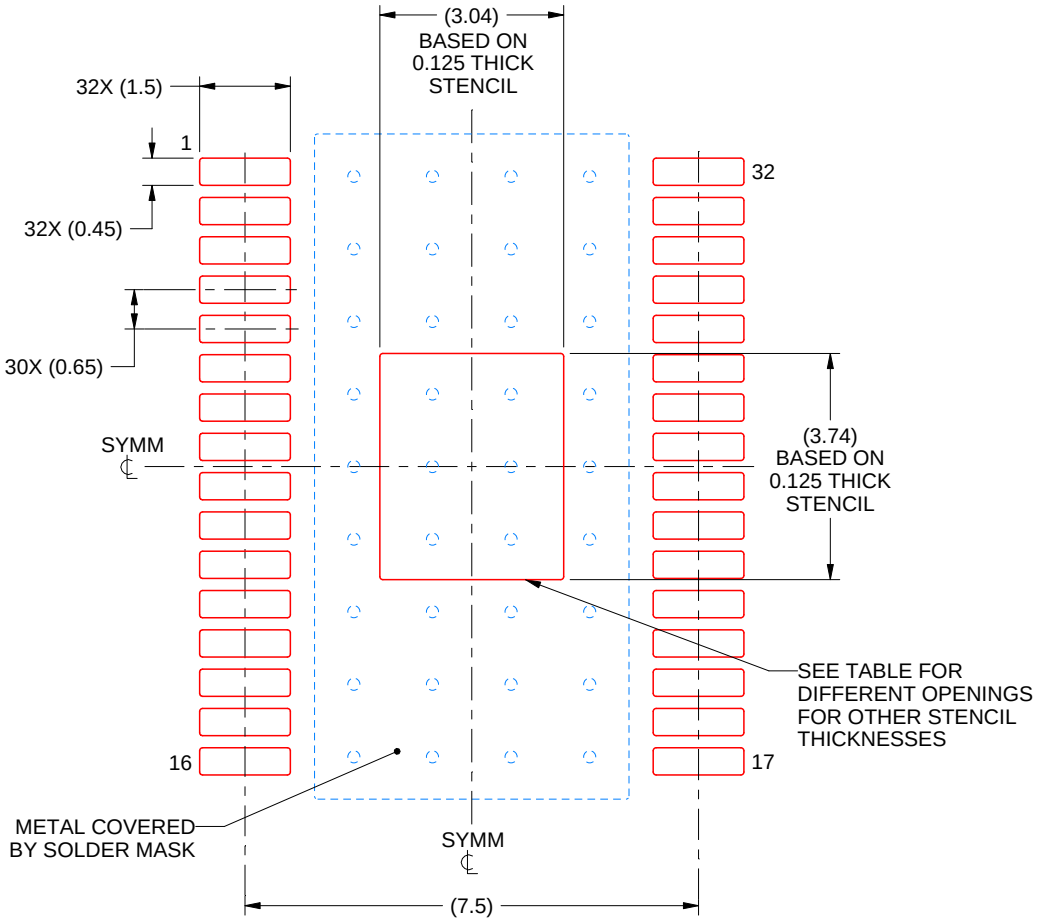


SOLDER MASK DETAILS
NOT TO SCALE

4223691/A 05/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.40 X 4.18
0.125	3.04 X 3.74 (SHOWN)
0.15	2.78 X 3.41
0.175	2.57 X 3.16

4223691/A 05/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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