PCAL9538A

Low-Voltage 8-bit I2C-Bus and SMBus Low Power I/O Port with Interrupt, Reset, and Agile I/O

Rev. 4.0 — 28 August 2026 Product data sheet

1 General description

The PCAL9538A is a low-voltage 8-bit General-Purpose Input/Output (GPIO) expander with interrupt and reset for I^2C-bus/SMBus applications. NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum. Such examples include Advanced Configuration and Power Interface (ACPI) power switches, sensors, push buttons, LEDs, and fan control.

In addition to providing a flexible set of GPIOs, the wide V_{DD} range of 1.65 V to 5.5 V allows the PCAL9538A to interface with next-generation microprocessors and microcontrollers where supply levels are dropping down to conserve power.

The PCAL9538A contains the PCA9538A register set of four 8-bit Configuration, Input, Output, and Polarity Inversion registers, and also, the PCAL9538A has Agile I/O, which are additional features designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pullup/pulldown resistors, maskable interrupt, interrupt status register, programmable open-drain, or push-pull outputs.

The PCAL9538A is a pin-to-pin replacement for the PCA9538, however, the PCAL9538A powers up with all I/O interrupts masked. This mask default allows for a board bring-up free of spurious interrupts at power up.

The PCAL9538A open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C-bus. Therefore, the PCAL9538A can remain a simple slave device.

The device outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

The Power-On Reset (POR) sets the registers to their default values and initializes the device state machine. In the PCAL9538A, the $\overline{RESET}$ pin causes the same reset/default I/O input configuration to occur without de-powering the device, holding the registers and I^2C-bus state machine in their default state until the $\overline{RESET}$ input is once again HIGH. This input requires a pullup to V_{DD}.

Two hardware pins (A0, A1) select the fixed I^2C-bus address and allow up to four devices to share I^2C-bus/SMBus.

2 Features and benefits

- I^2C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - 1.5 µA (typical at 5 V V_{DD})
  - 1.0 µA (typical at 3.3 V V_{DD})
- Schmitt trigger action allows slow input transition and better switching noise immunity at the Serial Clock Line (SCL) and Serial Data Line (SDA) inputs
  - V_{hys} = 0.10 × V_{DD} (typical)
- 5 V tolerant I/Os
- Active LOW reset input ($\overline{RESET}$)
- Open-drain active LOW interrupt output ($\overline{INT}$)
- 400 kHz Fast-mode I^2C-bus
- Internal power-on reset
- Power up with all channels configured as inputs
- No glitch on power up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ElectroStatic Discharge (ESD) protection exceeds JESD22
  - 2000 V Human Body Model (HBM) (A114-A)
  - 1000 V Charged-Device Model (CDM) (C101)
- Packages offered: TSSOP16, HVQFN16, and X2QFN16

2.1 Agile I/O features

- Pin to pin replacement for PCA9538 and PCA9538A with interrupts disabled at power up
  - Software backward-compatible with PCA9538 and PCA9538A
- Output port configuration: Bank selectable push-pull or open-drain output stages
- Interrupt status: Read-only register identifies the source of an interrupt
- Bitwise I/O programming features:
  - Output drive strength: Four programmable drive strengths to reduce rise and fall times in low capacitance applications
  - Input latch: Input Port register values changes are kept until the Input Port register is read
  - Pullup/pulldown enable: Floating input or pullup/down resistor enable
  - Pullup/pulldown selection: 100 kΩ pullup/down resistor selection
  - Interrupt mask: Prevents the generation of the interrupt when input changes state

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3 Ordering information

Table 1 describes the ordering information for PCAL9538A.

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCAL9538ABS	L3A	HVQFN16	Plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCAL9538APW	PL9538A	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCAL9538AEX1	38E	X2QFN16	Plastic, thermal enhanced super thin quad flat package; no leads; 16 terminals; body 1.6 mm × 1.6 mm × 0.35 mm	SOT1896-1

3.1 Ordering options

Table 2 describes the ordering options for PCAL9538A.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCAL9538ABS	PCAL9538ABSHP	HVQFN16	Reel 13" Q2/T3 *Standard mark SMD	6000	T_{amb} = -40 °C to +85 °C
PCAL9538APW	PCAL9538APWJ	TSSOP16	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = -40 °C to +85 °C
PCAL9538AEX1	PCAL9538AEX1Z	X2QFN16	Reel 7" Q2/T1 *Standard mark SMD	5000	T_{amb} = -40 °C to +85 °C

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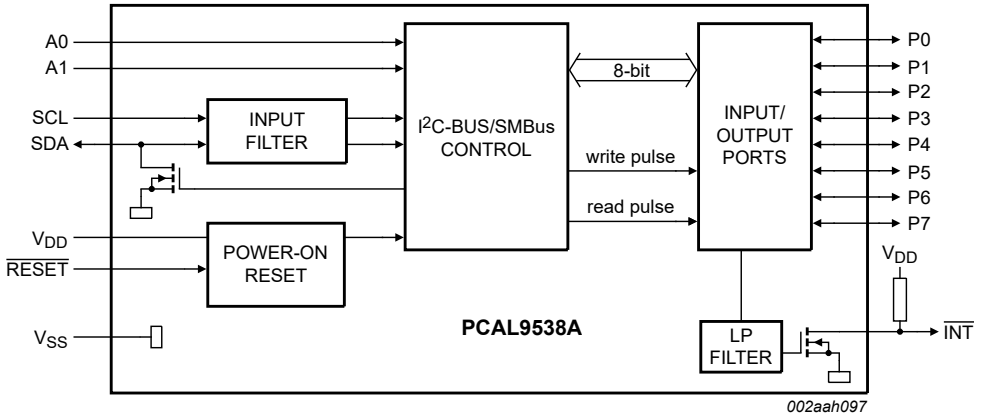
4 Block diagram

Figure 1 shows the labeled block diagram of PCAL9538A.



Remark: All I/Os are set to inputs at reset.

Figure 1. Block diagram of PCAL9538A

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5 Pinning information

This section provides the pin configuration and description for PCAL9538A.

5.1 Pinning

The figures given below show pinning for various packages of PCAL9538A.

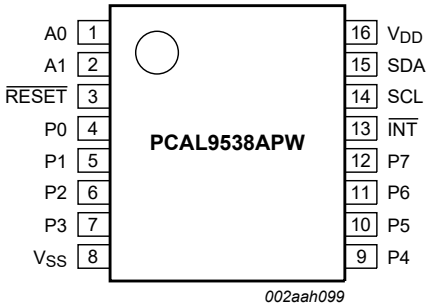

Figure 2. Pin configuration for TSSOP16

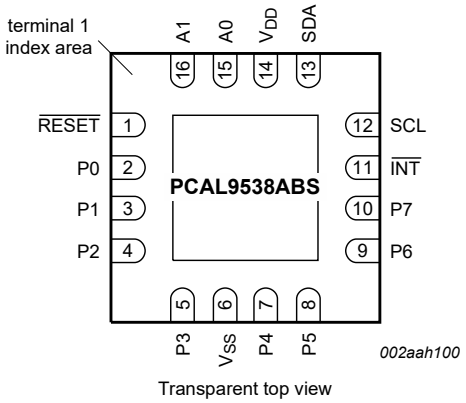

Figure 3. Pin configuration for HVQFN16

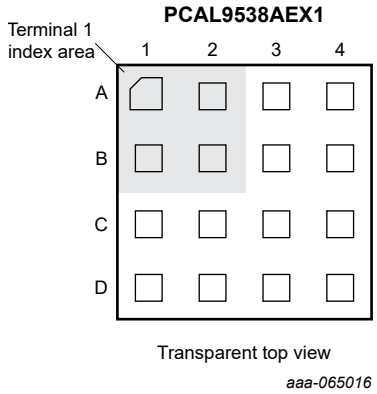

Figure 4. Pin configuration for X2QFN16

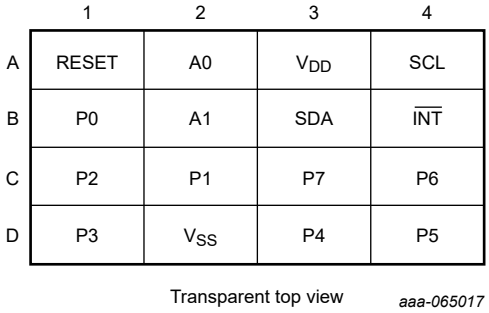

Figure 5. Ball mapping for X2QFN16

5.2 Pin description

Table 3 provides detailed description of various pins on PCAL9538A.

Table 3. Pin description

Symbol	Pin			Description
	TSSOP16	HVQFN16	X2QFN16	
A0	1	15	A2	Address input 0
A1	2	16	B2	Address input 1
$\overline{\text{RESET}}$	3	1	A1	Active LOW reset input
P0[1]	4	2	B1	Port P input/output 0
P1 [1]	5	3	C2	Port P input/output 1
P2 [1]	6	4	C1	Port P input/output 2

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Table 3. Pin description...*continued*

Symbol	Pin			Description
	TSSOP16	HVQFN16	X2QFN16	
P3 [1]	7	5	D1	Port P input/output 3
V_{SS}	8	6[2]	D2	Supply ground
P4 [1]	9	7	D3	Port P input/output 4
P5 [1]	10	8	D4	Port P input/output 5
P6 [1]	11	9	C4	Port P input/output 6
P7 [1]	12	10	C3	Port P input/output 7
$\overline{INT}$	13	11	B4	Interrupt output (open-drain)
SCL	14	12	A4	Serial clock line
SDA	15	13	B3	Serial data line
V_{DD}	16	14	A3	Supply voltage

[1] All I/O are configured as input at power on.

[2] HVQFN16 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to the supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias must be incorporated in the printed-circuit board in the thermal pad region.

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6 Functional description

Refer to Figure 1.

6.1 Device address

A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the four possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

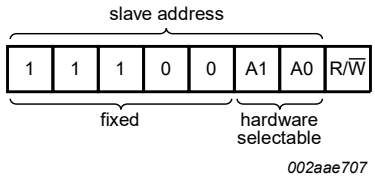

Figure 6. PCAL9538A address

6.2 Pointer register and command byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCAL9538A. Two bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that are affected. Bit 6 with the lower three bits of the Command byte are used to point to the extended features of the device (Agile I/O). This register is write only.

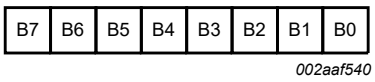

Figure 7. Pointer register bits

Table 4. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port	Read byte	xxxx xxxx[1]
0	0	0	0	0	0	0	1	01h	Output port	Read/write byte	1111 1111
0	0	0	0	0	0	1	0	02h	Polarity Inversion	Read/write byte	0000 0000
0	0	0	0	0	0	1	1	03h	Configuration	Read/write byte	1111 1111
0	1	0	0	0	0	0	0	40h	Output drive strength 0	Read/write byte	1111 1111
0	1	0	0	0	0	0	1	41h	Output drive strength 1	Read/write byte	1111 1111
0	1	0	0	0	0	1	0	42h	Input latch	Read/write byte	0000 0000
0	1	0	0	0	0	1	1	43h	Pullup/pulldown enable	Read/write byte	0000 0000
0	1	0	0	0	1	0	0	44h	Pullup/pulldown selection	Read/write byte	1111 1111
0	1	0	0	0	1	0	1	45h	Interrupt mask	Read/write byte	1111 1111
0	1	0	0	0	1	1	0	46h	Interrupt status	Read byte	0000 0000

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Table 4. Command byte*...continued*

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	1	0	0	1	1	1	1	4Fh	Output port configuration	Read/write byte	0000 0000

[1] Undefined.

6.3 Interface definition

Table 5 describes the interface definition for PCAL9538A.

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C-bus slave address	H	H	H	L	L	A1	A0	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

6.4 Register descriptions

This section describes the PCAL9538A registers. It is further divided into the following subsections:

6.4.1 Input port register (00h)

The Input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port register is read only; writes to this register have no effect. The externally applied logic level determines the default value 'X'. An Input port register-read operation is performed as described in Section 7.2.

Table 6. Input port register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	X	X	X	X	X	X	X	X

6.4.2 Output port register (01h)

The Output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from this register reflect the value that was written to this register, **not** the actual pin value.

Table 7. Output port register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

6.4.3 Polarity inversion register (02h)

The Polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

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Table 8. Polarity inversion register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

6.4.4 Configuration register (03h)

The Configuration register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 9. Configuration register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

6.4.5 Output drive strength registers (40h, 41h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example, register 41 CC7 (bits [7:6]) controls port 7 and register 41 CC6 (bits [5:4]) controls port 6. The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.5×, 10b = 0.75×, or 11b = 1× of the drive capability of the I/O. See Section 8.2 for more details.

Table 10. Current control register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC3		CC2		CC1		CC0	
Default	1	1	1	1	1	1	1	1

Table 11. Current control register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC7		CC6		CC5		CC4	
Default	1	1	1	1	1	1	1	1

6.4.6 Input latch register (42h)

The Input latch register enables and disables the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input port register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt. The input logic value is loaded into the corresponding bit of the input port register (registers 0). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register are read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See Figure 13. For example, if the P4 input was as logic 0 and the input goes to logic 1 and then back to logic 0, the input port register captures this change and

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an interrupt is generated (if unmasked). When the read is performed on the input port register, the interrupt is cleared, assuming there were no additional inputs that have changed, and bit 4 of the input port register reads '1'. The next read of the input port register bit 4 must now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input port register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is not cleared if the input latch register changes from latched to non-latched configuration.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input port register reflects the latched logic level.

Table 12. Input latch register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	L7	L6	L5	L4	L3	L2	L1	L0
Default	0	0	0	0	0	0	0	0

6.4.7 Pullup/pulldown enable register (43h)

This register allows the user to enable or disable pullup/pulldown resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pullup/pulldown resistors. Setting the bit to logic 0 disconnects the pullup/pulldown resistors from the I/O pins. Use the pullup/pulldown registers to select either a pullup or pulldown resistor.

Table 13. Pullup/pulldown enable register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	0	0	0	0	0	0	0	0

6.4.8 Pullup/pulldown selection register (44h)

The I/O port can be configured to have a pullup or pulldown resistor by programming the pullup/pulldown selection register. Setting a bit to logic 1 selects a 100 kΩ pullup resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pulldown resistor for that I/O pin. If the pullup/pulldown feature is disconnected, writing to this register has no effect on the I/O pin. The typical value is 100 kΩ with a minimum of 50 kΩ and a maximum of 150 kΩ.

Table 14. Pullup/pulldown selection register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD7	PUD6	PUD5	PUD4	PUD3	PUD2	PUD1	PUD0
Default	1	1	1	1	1	1	1	1

6.4.9 Interrupt mask register (45h)

This register is set to logic 1 upon power on, disabling interrupts during system startup. Interrupts can be enabled by setting the corresponding mask bits to logic 0. If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin ($\overline{INT}$) is not asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin is asserted.

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When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 causes the interrupt pin to be asserted. If the interrupt mask bit of an input that is the source of an interrupt is set to 1, the interrupt pin is de-asserted.

Table 15. Interrupt mask register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	M7	M6	M5	M4	M3	M2	M1	M0
Default	1	1	1	1	1	1	1	1

6.4.10 Interrupt status register (46h)

This read-only register is used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit returns logic 0.

Table 16. Interrupt status register (address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	S7	S6	S5	S4	S3	S2	S1	S0
Default	0	0	0	0	0	0	0	0

6.4.11 Output port configuration register (4Fh)

The Output port configuration register selects a port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 8). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active). The recommended command sequence is to program this register (4Fh) before the Configuration register (03h) sets the port pins as outputs.

Table 17. Output port configuration register (address 4Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved							ODEN0
Default	0	0	0	0	0	0	0	0

6.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage can be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V_{DD} or V_{SS}. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

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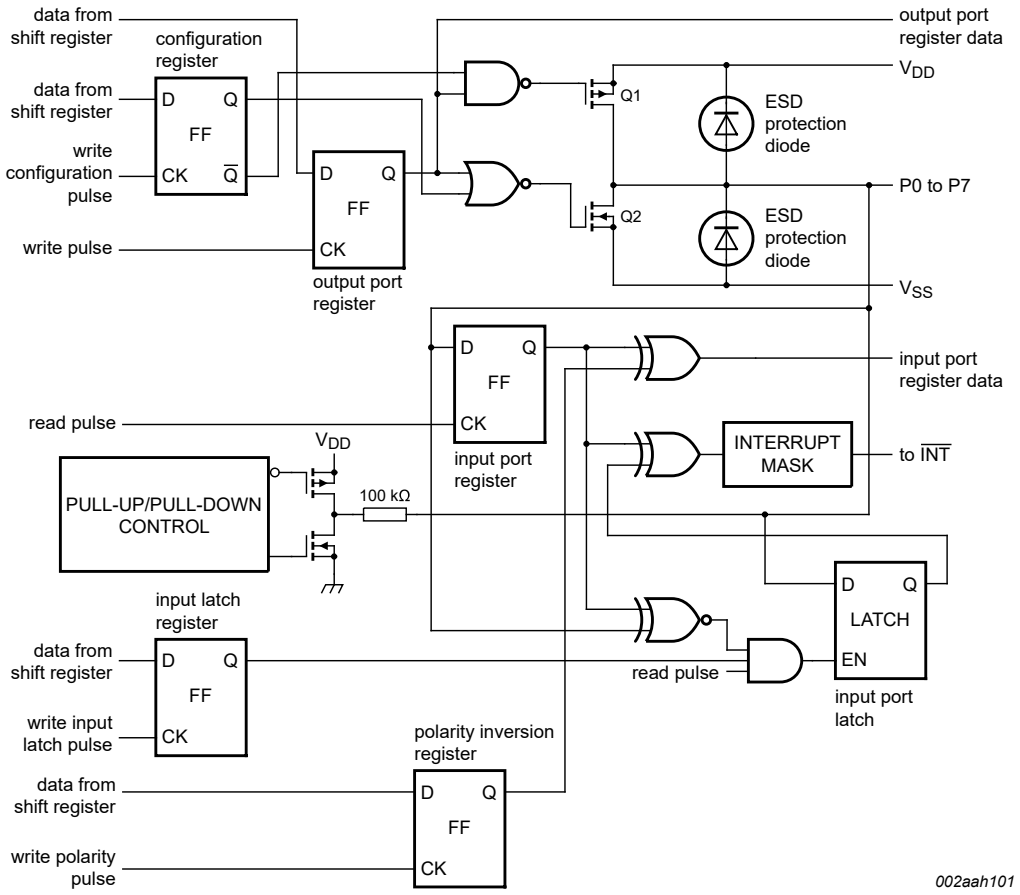

On power up or reset, all registers return to default values.

Figure 8. Simplified schematic of the I/Os (P0 to P7)

6.6 Power-On Reset (POR)

When power (from 0 V) is applied to V_{DD}, an internal power-on reset holds the PCAL9538A in a reset condition until V_{DD} has reached V_{POR}. Then, the reset condition is released and the PCAL9538A registers and I^2C-bus/SMBus state machine initialize to their default states. After that, V_{DD} must be lowered to below V_{POR} and back up to the operating voltage for a power-reset cycle. For details, see Section 8.4.

6.7 Reset input

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the V_{DD} at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin LOW for a minimum of $t_{w(rst)}$. The PCAL9538A registers and I^2C-bus/SMBus state machine are changed to their default state once $\overline{RESET}$ is LOW (0). When $\overline{RESET}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pullup resistor to V_{DD} if no active connection is used.

6.8 Interrupt output

Any rising or falling edge of the port inputs in the Input mode generates an interrupt. After time $t_{v(INT)}$, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt (see Figure 12). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that

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occur during ACK or NACK clock pulse can be lost (or be short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input can cause a false interrupt to occur, if the state of the pin does not match the contents of the Input port register.

The $\overline{INT}$ output has an open-drain structure and requires a pullup resistor to V_{DD}. $\overline{INT}$ must be connected to the voltage source of the device that requires the interrupt information. When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

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7 Bus transactions

The PCAL9538A is an I^2C-bus slave device. Data is exchanged between the master and PCAL9538A through write and read commands using the I^2C-bus. The two communication lines are SDA and SCL. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

7.1 Write commands

Data is transmitted to PCAL9538A by sending the device address and setting the LSB to a logic 0 (refer Figure 6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

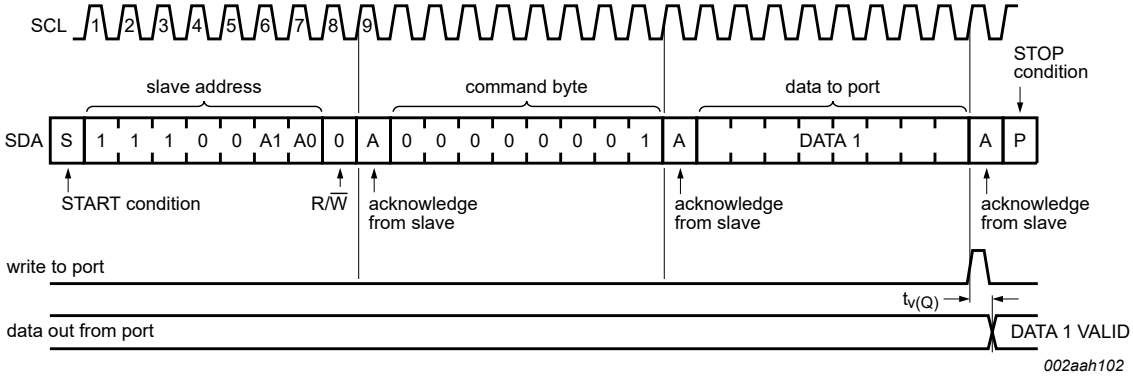

Figure 9. Write to Output port register

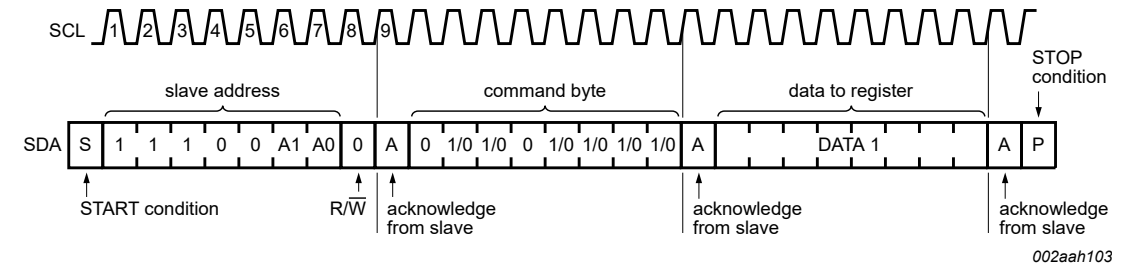

Figure 10. Write to Configuration or Polarity inversion registers

7.2 Read commands

To read data from the PCAL9538A, the bus master must first send the PCAL9538A address with LSB set to a logic 0 (refer Figure 6 for device address). The command byte is sent after the address and determines which register is to be accessed.

After a restart the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCAL9538A (see Figure 11 and Figure 12).

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limit on the number of data bytes received in one read transmission. But on the final byte received, the bus master must not acknowledge the data.

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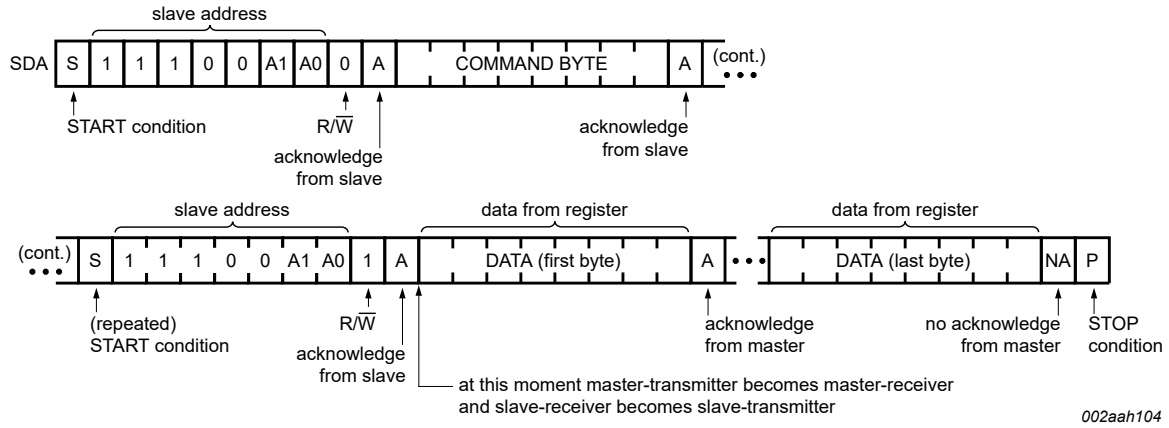
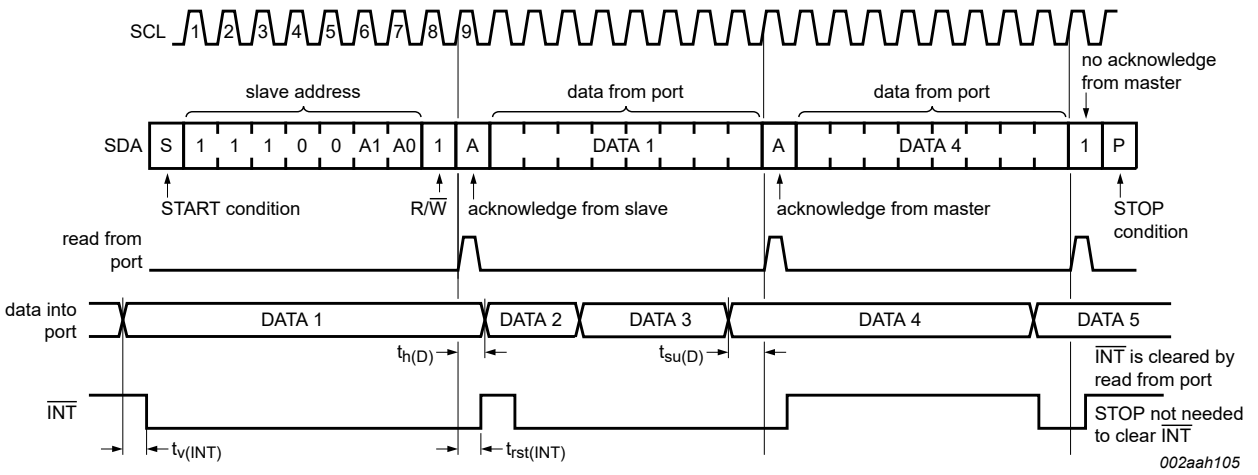


Figure 11. Read from register



Transfer of data can be stopped at any time by a STOP condition. When this situation occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

This figure eliminates the command byte transfer, a restart, and slave address call between initial slave address call and actual data transfer from P port (see Figure 11).

Figure 12. Read Input port register (non-latched)

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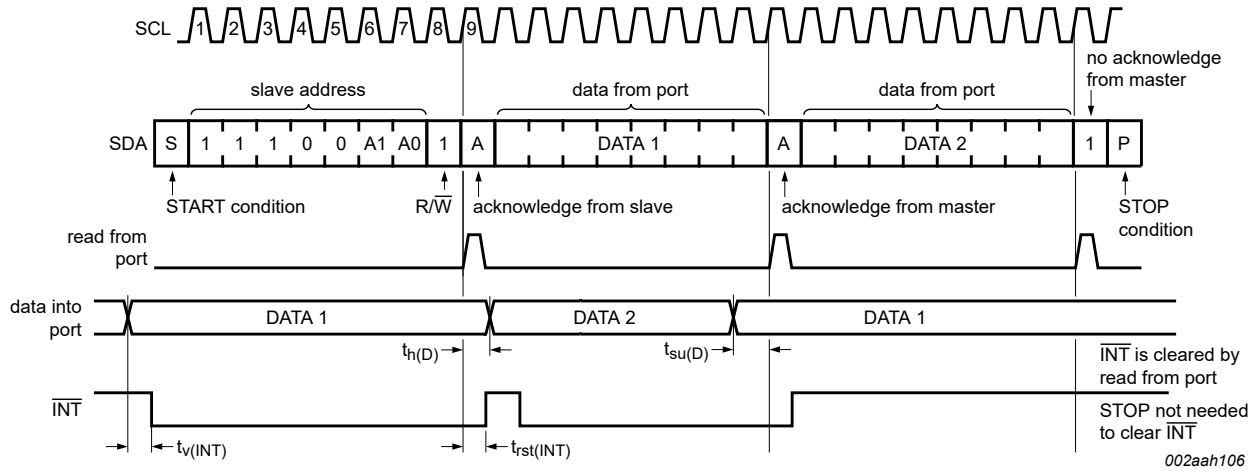

Transfer of data can be stopped at any time by a STOP condition. When this situation occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

This figure eliminates the command byte transfer, a restart, and slave address call between initial slave address call and actual data transfer from P port (see Figure 11).

Figure 13. Read Input port register (latch enabled)

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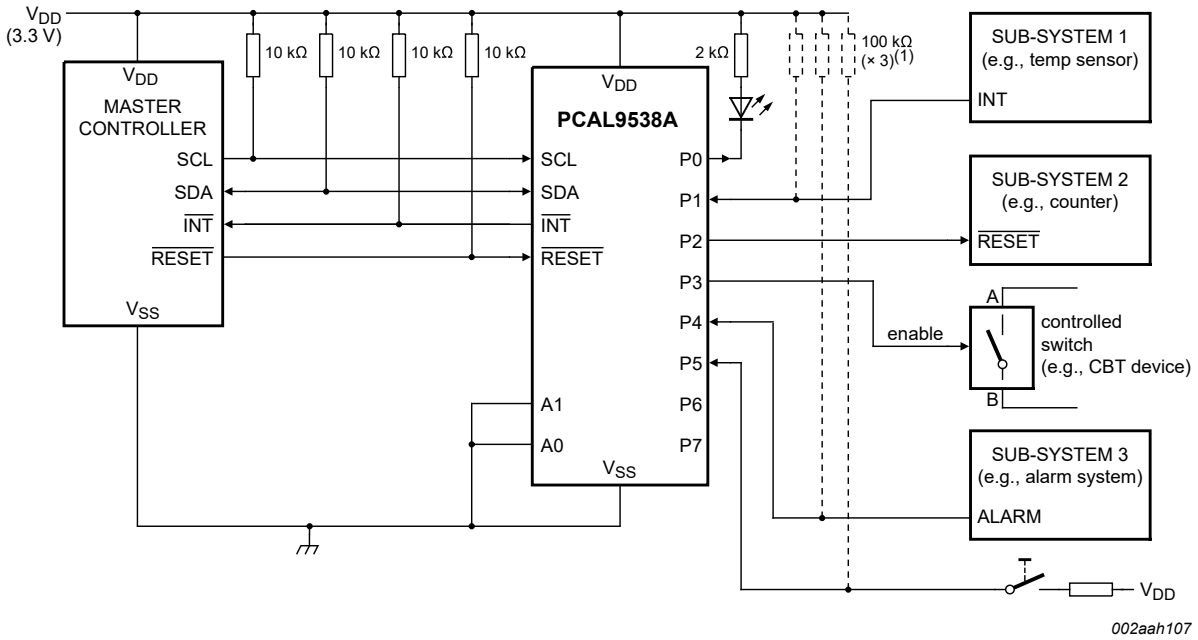
8 Application design-in information

Figure 14 shows the typical application of PCAL9538A.



The device address is 1110 000x for this example.

P0, P2, P3 configured as outputs.

P1, P4, P5 configured as inputs.

P6 and P7 are not used and need 100 kΩ pullup resistors to protect them from floating or the internal pullup or pulldown selected.

(1) Resistors are required for inputs (on P port) that can float. If a driver to an input never lets the input float, a resistor is not needed. Outputs (in the P port) do not need pullup resistors.

Figure 14. Typical application

8.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 14. Since the Light Emitting Diode (LED) acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, must consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 15 shows a high-value resistor in parallel with the LED. Figure 16 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.

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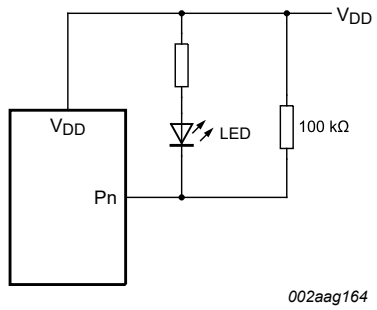

Figure 15. High-value resistor in parallel with the LED

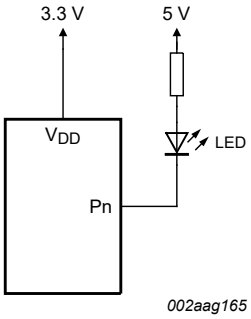

Figure 16. Device supplied by a lower voltage

8.2 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits, the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

Figure 17 shows a simplified output stage. The Configuration register, the Output port data, and the Current Control register affect the behavior of the pad. When the Current Control register bits are programmed to 10b, then only two of the fingers are active, reducing the current drive capability by 50 %.

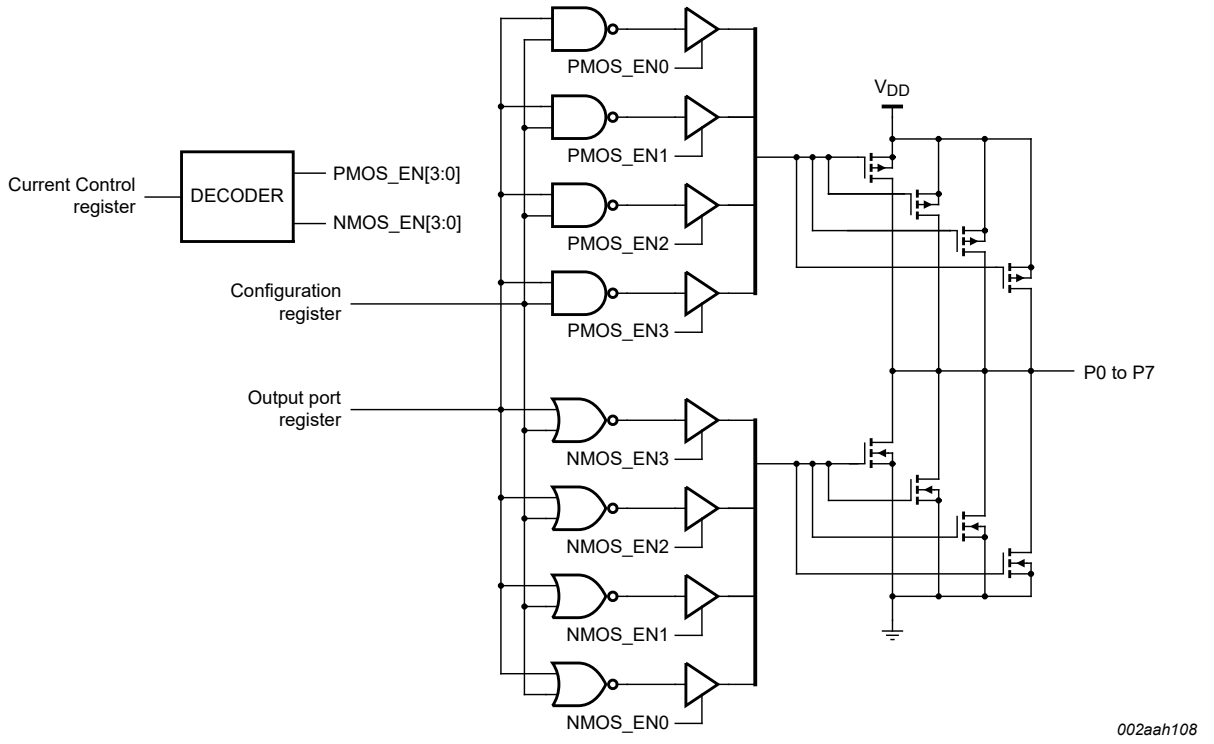

Figure 17. Simplified output stage

Reducing the current drive capability can be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{DD} and V_{SS} package inductance and creates noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time create ground

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and supplies noise. The output drive strength control through the Current Control registers allows the user to mitigate SSN issues without the need of additional external components.

8.3 12 V tolerant I/Os

The PCAL9538A device SCR group reference diode can go up to 10 V before latching back to 8 V. The ESD gate oxide protects the device, but not when used continually. Therefore, to achieve 12 V tolerant I/Os, the external protection circuitry (diode) must be used as shown in Figure 18.

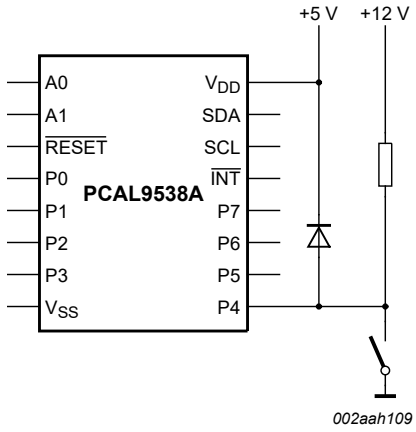

Figure 18. External protection circuitry

8.4 Power-On Reset (POR) requirements

In the event of a glitch or data corruption, PCAL9538A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device goes through a power cycle to be reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 19 and Figure 20.

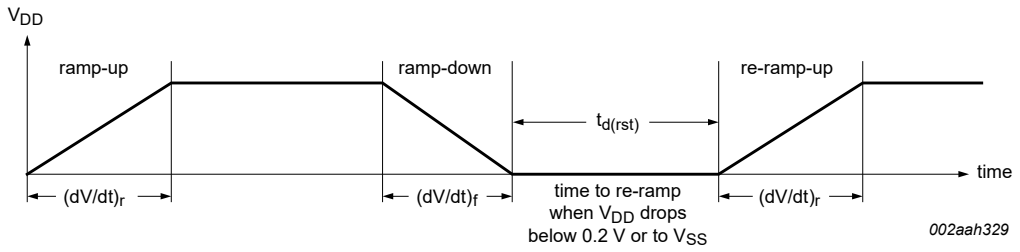

Figure 19. V_{DD} is lowered below 0.2 V or 0 V and then ramped up to V_{DD}

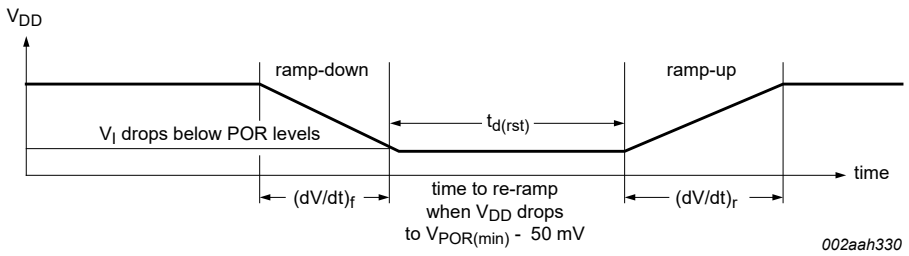

Figure 20. V_{DD} is lowered below the POR threshold, then ramped back up to V_{DD}

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Table 18 specifies the performance of the power-on reset feature for PCAL9538A for both types of power-on reset.

Table 18. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$(dV/dt)_f$	Fall rate of change of voltage	Figure 19	0.1	-	2000	ms
$(dV/dt)_r$	Rise rate of change of voltage	Figure 19	0.1	-	2000	ms
$t_{d(rst)}$	Reset delay time	Figure 19; re-ramp time when V_{DD} drops to V_{SS}	1	-	-	µs
		Figure 20; re-ramp time when V_{DD} drops to $V_{POR(min)}$ - 50 mV	1	-	-	µs
$\Delta V_{DD(gl)}$	Glitch supply voltage difference	Figure 21 [1]	-	-	1.0	V
$t_{w(gl)VDD}$	Supply voltage glitch pulse width	Figure 21 [2]	-	-	10	µs
$V_{POR(trip)}$	Power-on reset trip voltage	Falling V_{DD}	0.7	-	-	V
		Rising V_{DD}	-	-	1.4	V

[1] Level that V_{DD} can glitch down to, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.
[2] Glitch width that does not cause a functional disruption when $\Delta V_{DD(gl)}$ = 0.5 × V_{DD}.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) depend on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 21 and Table 18 provide more information on how to measure these specifications.

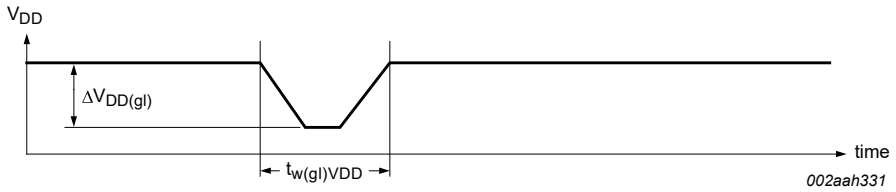

Figure 21. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released, and all registers and I^2C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. Figure 22 and Table 18 provide more details on this specification.

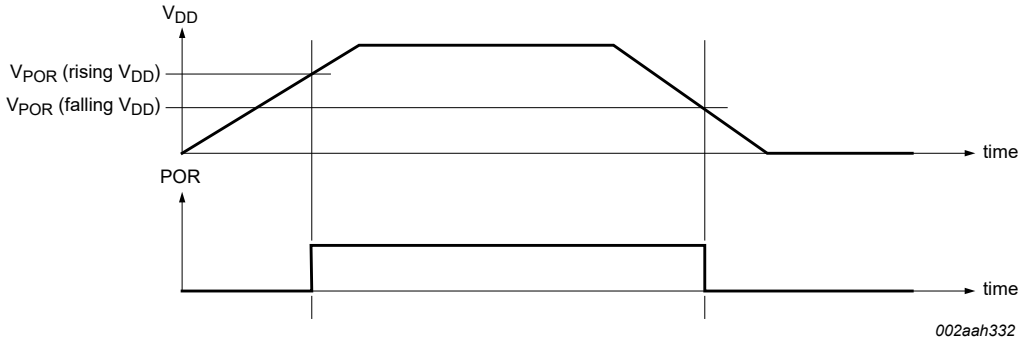

Figure 22. Power-on reset voltage (V_{POR})

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8.5 Device current consumption with internal pullup and pulldown resistors

The PCAL9538A integrates programmable pullup and pulldown resistors to eliminate external components when pins configured as inputs and pullup or pulldown resistors are required, for example, when nothing is driving the inputs to the power supply rails. Since these pullup and pulldown resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pullup or pulldown function is selected in register 44h, while the resistor is connected by the enable register 43h. The configuration of the resistors is shown in Figure 8.

If the resistor is configured as a pullup, that is, connected to V_{DD}, a current flows from the V_{DD} pin through the resistor to the ground when the pin is held LOW. This current appears as an additional I_{DD} upsetting any current consumption measurements.

In the same manner, if the resistor is configured as a pulldown and the pin is held HIGH, current flows from the power supply through the pin to the V_{SS} pin. While this current is not measured as part of I_{DD}, one must be mindful of the 200 mA limiting value through V_{SS}.

The pullup and pulldown resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 kΩ with a nominal 100 kΩ value. Any current flowing through these resistors is additive by the number of pins held HIGH or LOW. The current can be calculated using Ohm's law. See Figure 26 for a graph of supply current versus the number of pullup resistors.

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9 Limiting values

This section describes the limiting values of PCAL9538A.

Table 19. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Note	Min	Max	Unit
V_{DD}	Supply voltage			-0.5	+6.5	V
V_I	Input voltage		[1]	-0.5	+6.5	V
V_O	Output voltage		[1]	-0.5	+6.5	V
I_{IK}	Input clamping current	A0, A1, $\overline{RESET}$, SCL; V_I < 0 V		-	±20	mA
I_{OK}	Output clamping current	$\overline{INT}$; V_O < 0 V		-	±20	mA
I_{IOK}	Input/output clamping current	P port; V_O < 0 V or V_O > V_{DD}		-	±20	mA
		SDA; V_O < 0 V or V_O > V_{DD}		-	±20	mA
I_{OL}	LOW-level output current	Continuous; I/O port		-	50	mA
		Continuous; SDA, $\overline{INT}$		-	25	mA
I_{OH}	HIGH-level output current	Continuous; P port		-	25	mA
I_{DD}	Supply current			-	160	mA
I_{SS}	Ground supply current			-	200	mA
P_{tot}	Total power dissipation			-	200	mW
T_{stg}	Storage temperature			-65	+150	°C
$T_{j(max)}$	Maximum junction temperature			-	125	°C

[1] The input negative-voltage and output voltage ratings can be exceeded when the input and output current ratings are observed.

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10 Recommended operating conditions

This section describes the recommended operating conditions for PCAL9538A.

Table 20. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA, $\overline{RESET}$	0.7 × V_{DD}	5.5	V
		A0, A1, P port	0.7 × V_{DD}	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA, $\overline{RESET}$	-0.5	0.3 × V_{DD}	V
		A0, A1, P port	-0.5	0.3 × V_{DD}	V
I_{OH}	HIGH-level output current	P port	-	10	mA
I_{OL}	LOW-level output current	P port	-	25	mA
T_{amb}	Ambient temperature	Operating in free air	-40	+85	°C

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11 Thermal characteristics

This section describes the thermal characteristics of PCAL9538A.

Table 21. Thermal characteristics

Symbol	Parameter	Conditions	Note	Max	Unit
$Z_{th(j-a)}$	Transient thermal impedance from junction to ambient	HVQFN16 package	[1]	53	K/W
		TSSOP16 package	[1]	108	K/W
		XQFN16 package	[1]	184	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

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12 Static characteristics

This section describes the static characteristics of PCAL9538A.

Table 22. Static characteristics

T_{amb} = -40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	Input clamping voltage	I_I = -18 mA	-1.2	-	-	V
V_{POR}	Power-on reset voltage	$V_I = V_{DD}$ or V_{SS}; I_O = 0 mA	-	1.1	1.4	V
V_{OH}	HIGH-level output voltage[2]	P port; I_{OH} = -8 mA; CCX = 11b				
		V_{DD} = 1.65 V	1.2	-	-	V
		V_{DD} = 2.3 V	1.8	-	-	V
		V_{DD} = 3 V	2.6	-	-	V
		V_{DD} = 4.5 V	4.1	-	-	V
		P port; I_{OH} = -2.5 mA and CCX = 00b; I_{OH} = -5 mA and CCX = 01b; I_{OH} = -7.5 mA and CCX = 10b; I_{OH} = -10 mA and CCX = 11b				
		V_{DD} = 1.65 V	1.1	-	-	V
		V_{DD} = 2.3 V	1.7	-	-	V
		V_{DD} = 3 V	2.5	-	-	V
		V_{DD} = 4.5 V	4.0	-	-	V
V_{OL}	LOW-level output voltage [2]	P port; I_{OL} = 8 mA; CCX = 11b				
		V_{DD} = 1.65 V	-	-	0.45	V
		V_{DD} = 2.3 V	-	-	0.25	V
		V_{DD} = 3 V	-	-	0.25	V
		V_{DD} = 4.5 V	-	-	0.2	V
		P port; I_{OL} = 2.5 mA and CCX = 00b; I_{OL} = 5 mA and CCX = 01b; I_{OL} = 7.5 mA and CCX = 10b; I_{OL} = 10 mA and CCX = 11b				
		V_{DD} = 1.65 V	-	-	0.5	V
		V_{DD} = 2.3 V	-	-	0.3	V
		V_{DD} = 3 V	-	-	0.25	V
		V_{DD} = 4.5 V	-	-	0.2	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 1.65 V to 5.5 V				
		SDA	3	-	-	mA
		$\overline{INT}$	3	15[3]	-	mA
I_I	Input current	V_{DD} = 1.65 V to 5.5 V				
		SCL, SDA, $\overline{RESET}$; $V_I = V_{DD}$ or V_{SS}	-	-	0.1	µA
		A0, A1; $V_I = V_{DD}$ or V_{SS}	-	-	±1	µA

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Table 22. Static characteristics...*continued*

T_{amb} = -40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{IH}	HIGH-level input current	P port; $V_I = V_{DD}$; V_{DD} = 1.65 V to 5.5 V	-	-	1	µA
I_{IL}	LOW-level input current	P port; $V_I = V_{SS}$; V_{DD} = 1.65 V to 5.5 V	-	-	1	µA
I_{DD}	Supply current	SDA, P port, A0, A1, $\overline{RESET}$; V_I on SDA and $\overline{RESET}$ = V_{DD} or V_{SS}; V_I on P port and A0, A1 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz				
		V_{DD} = 3.6 V to 5.5 V	-	10	25	µA
		V_{DD} = 2.3 V to 3.6 V	-	6.5	15	µA
		V_{DD} = 1.65 V to 2.3 V	-	4	9	µA
		SCL, SDA, P port, A0, A1, $\overline{RESET}$; V_I on SCL, SDA, and $\overline{RESET}$ = V_{DD} or V_{SS}; V_I on P port and A0, A1 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz				
		V_{DD} = 3.6 V to 5.5 V	-	1.5	7	µA
		V_{DD} = 2.3 V to 3.6 V	-	1	3.2	µA
		V_{DD} = 1.65 V to 2.3 V	-	0.5	1.7	µA
ΔI_{DD}	Additional quiescent supply current	SCL, SDA, $\overline{RESET}$; one input at V_{DD} - 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	25	µA
		P port, A0, A1; one input at V_{DD} - 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	80	µA
C_i	Input capacitance	$V_I = V_{DD}$ or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	6	7	pF
C_{io}	Input/output capacitance	$V_{I/O} = V_{DD}$ or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	7	8	pF
		$V_{I/O} = V_{DD}$ or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	7.5	8.5	pF
$R_{pu(int)}$	Internal pullup resistance	Input/output	50	100	150	kΩ
$R_{pd(int)}$	Internal pulldown resistance	Input/output	50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V, or 5 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at V_{DD} = 3.3 V and T_{amb} = 25 °C.

[2] The total current sourced by all I/Os must be limited to 160 mA. The total current sunk by all I/Os must be limited to 200 mA.

[3] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and V_{DD} = 3.3 V. Typical value for V_{DD} < 2.5 V, V_{OL} = 0.6 V.

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12.1 Typical characteristics

This section describes the typical characteristics of PCAL9538A.

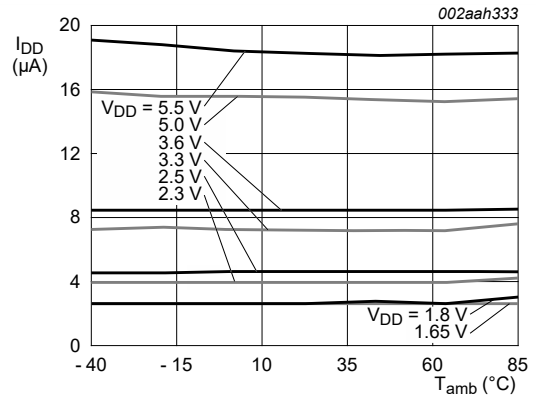


Figure 23. Supply current versus ambient temperature

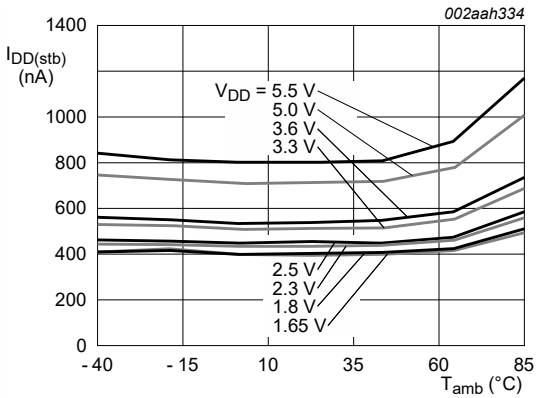
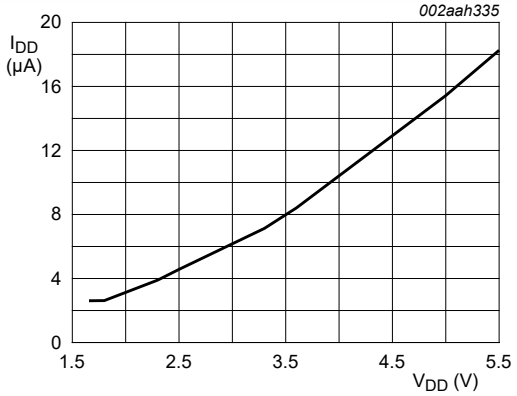
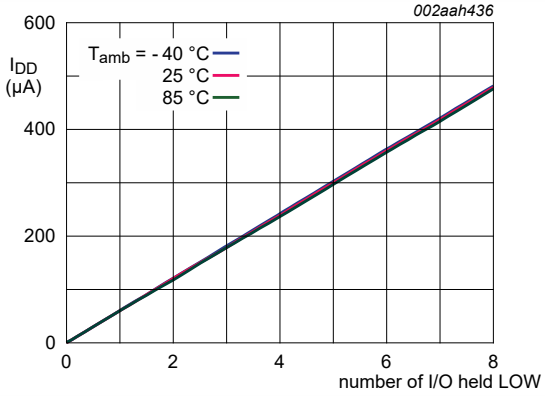


Figure 24. Standby supply current versus ambient temperature



T_{amb} = 25 °C

Figure 25. Supply current versus supply voltage



V_{DD} = 5 V

Figure 26. Supply current versus number of I/O held LOW

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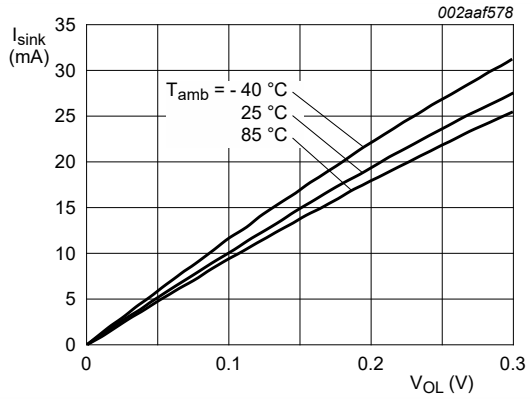
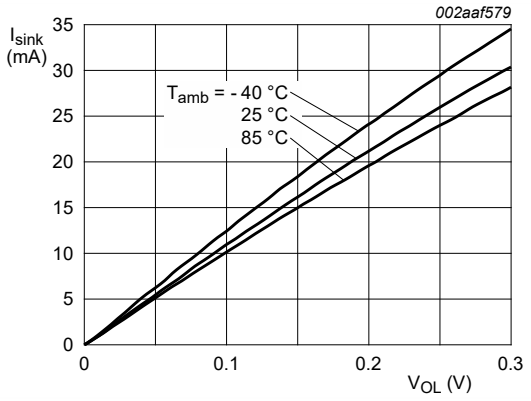
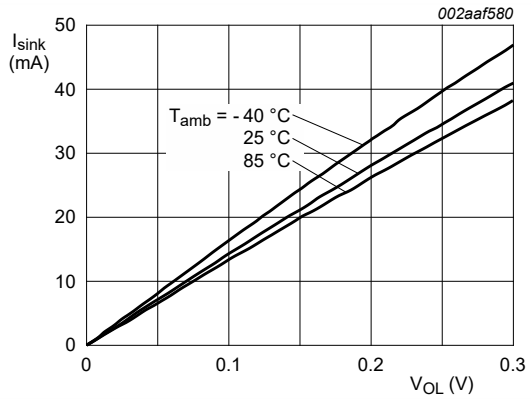


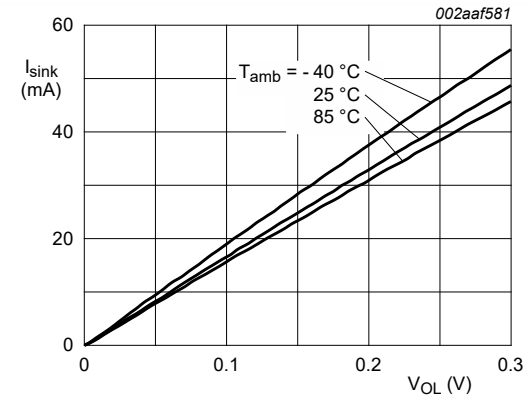
a. V_{DD} = 1.65 V



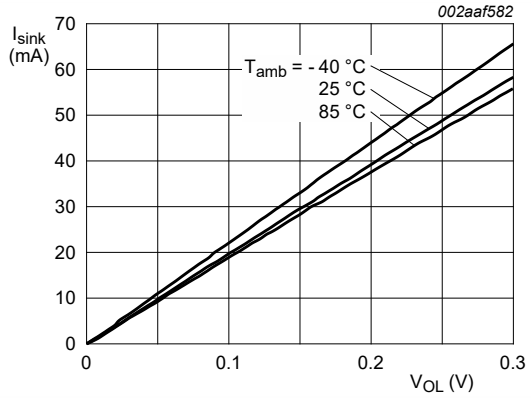
b. V_{DD} = 1.8 V



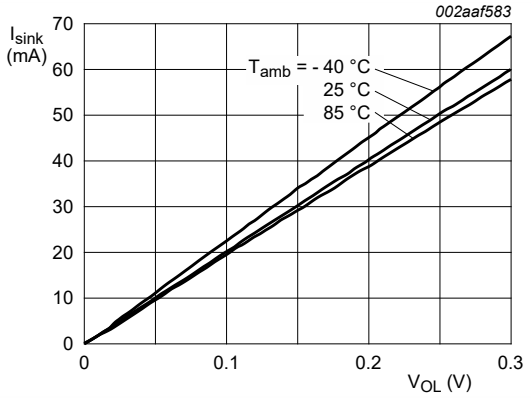
c. V_{DD} = 2.5 V



d. V_{DD} = 3.3 V



e. V_{DD} = 5.0 V



f. V_{DD} = 5.5 V

Figure 27. I/O sink current versus LOW-level output voltage with CCX.X = 11b

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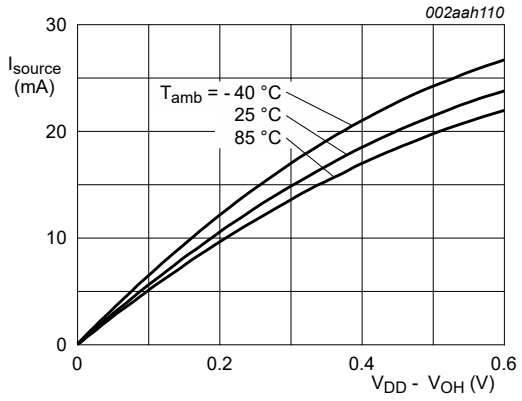
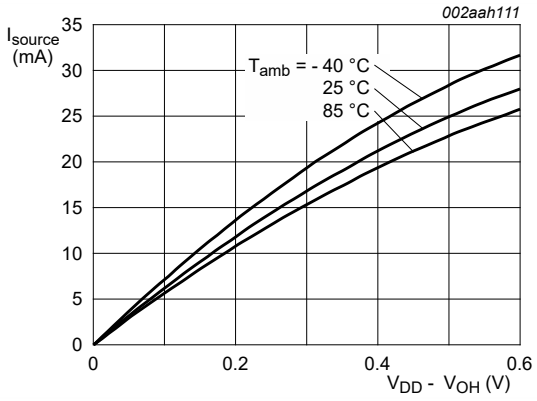
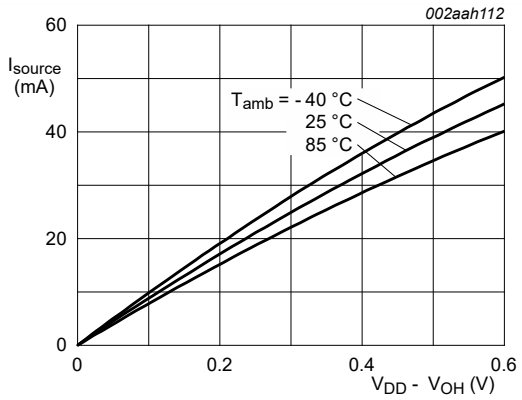


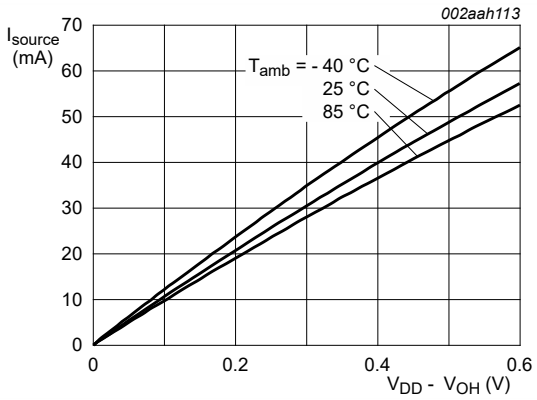
a. V_{DD} = 1.65 V



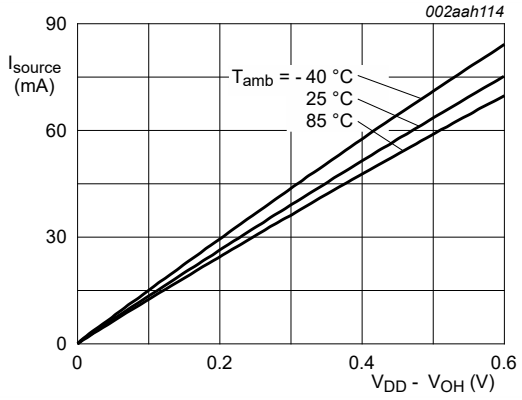
b. V_{DD} = 1.8 V



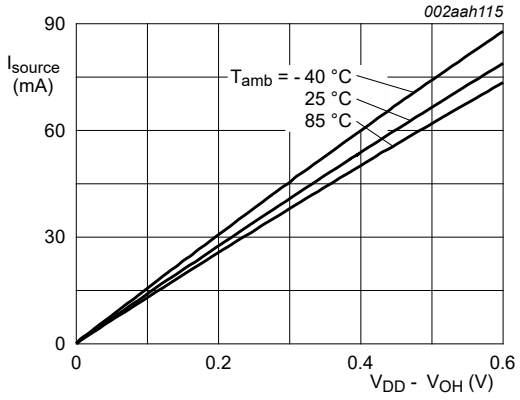
c. V_{DD} = 2.5 V



d. V_{DD} = 3.3 V



e. V_{DD} = 5.0 V



f. V_{DD} = 5.5 V

Figure 28. I/O source current versus HIGH-level output voltage with CCX.X = 11b

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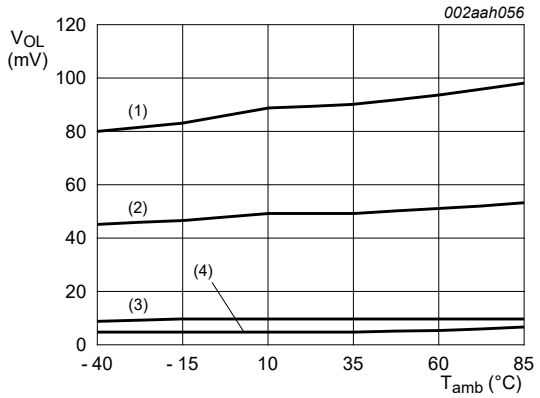
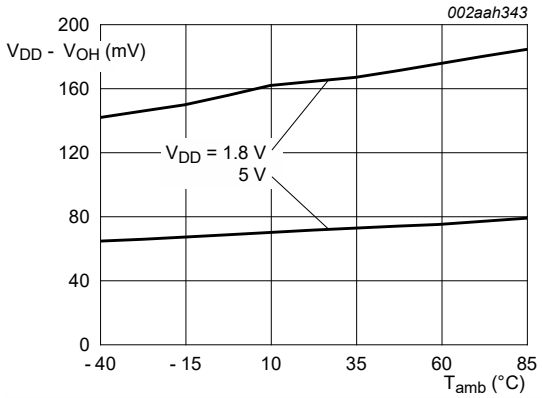


(1) V_{DD} = 1.8 V; I_{sink} = 10 mA
(2) V_{DD} = 5 V; I_{sink} = 10 mA
(3) V_{DD} = 1.8 V; I_{sink} = 1 mA
(4) V_{DD} = 5 V; I_{sink} = 1 mA

Figure 29. LOW-level output voltage versus temperature



I_{source} = -10 mA

Figure 30. I/O high voltage versus temperature

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13 Dynamic characteristics

This section describes the dynamic characteristics of PCAL9538A.

Table 23. I^2C-bus interface timing requirements

Over the recommended operating free air temperature range, unless otherwise specified. See Figure 31.

Symbol	Parameter	Conditions	Standard-mode I^2C-bus		Fast-mode I^2C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU;DAT}$	Data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	Data hold time		0	-	0	-	ns
t_r	Rise time of both SDA and SCL signals		-	1000	20	300	ns
t_f	Fall time of both SDA and SCL signals		-	300	20 × (V_{DD}/5.5 V)	300	ns
t_{BUF}	Bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{HD;STA}$	Hold time (repeated) START condition		4	-	0.6	-	µs
$t_{SU;STO}$	Set-up time for STOP condition		4	-	0.6	-	µs
$t_{VD;DAT}$	Data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	µs

Table 24. Reset timing requirements

Over the recommended operating free air temperature range, unless otherwise specified. See Figure 34.

Symbol	Parameter	Conditions	Standard-mode I^2C-bus		Fast-mode I^2C-bus		Unit
			Min	Max	Min	Max	
$t_{w(rst)}$	Reset pulse width		30	-	30	-	ns
$t_{rec(rst)}$	Reset recovery time		200	-	200	-	ns
t_{rst}	Reset time	[1]	600	-	600	-	ns

[1] Minimum time for SDA to become HIGH or minimum time to wait before doing a START.

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Table 25. Switching characteristics

Over the recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Figure 31.

Symbol	Parameter	Conditions	Standard-mode I^2C-bus		Fast-mode I^2C-bus		Unit
			Min	Max	Min	Max	
$t_{v(INT)}$	Valid time on pin $\overline{INT}$	From P port to $\overline{INT}$	-	1	-	1	µs
$t_{rst(INT)}$	Reset time on pin $\overline{INT}$	From SCL to $\overline{INT}$	-	1	-	1	µs
$t_{v(Q)}$	Data output valid time	From SCL to P port	-	400	-	400	ns
$t_{su(D)}$	Data input set-up time	From P Port to SCL	0	-	0	-	ns
$t_{h(D)}$	Data input hold time	From P Port to SCL	300	-	300	-	ns

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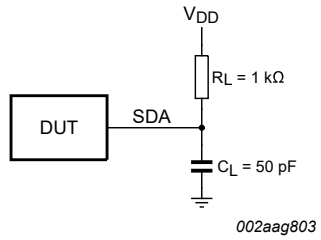
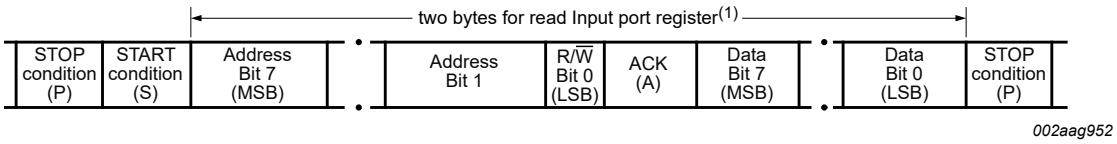
14 Parameter measurement information

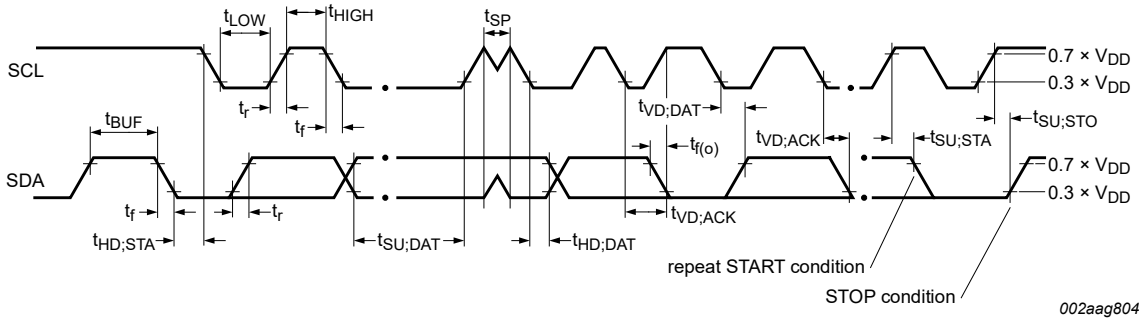
This section describes the parameter measurement information for PCAL9538A.



a. SDA load configuration



b. Transaction format



c. Voltage waveforms

C_L includes probe and jig capacitance.
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.
All parameters and waveforms are not applicable to all devices.
Byte 1 = I^2C-bus address; Byte 2, byte 3 = P port data.

(1) See Figure 11.

Figure 31. I^2C-bus interface load circuit and voltage waveforms

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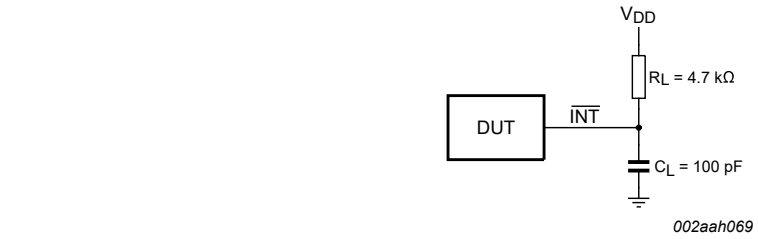
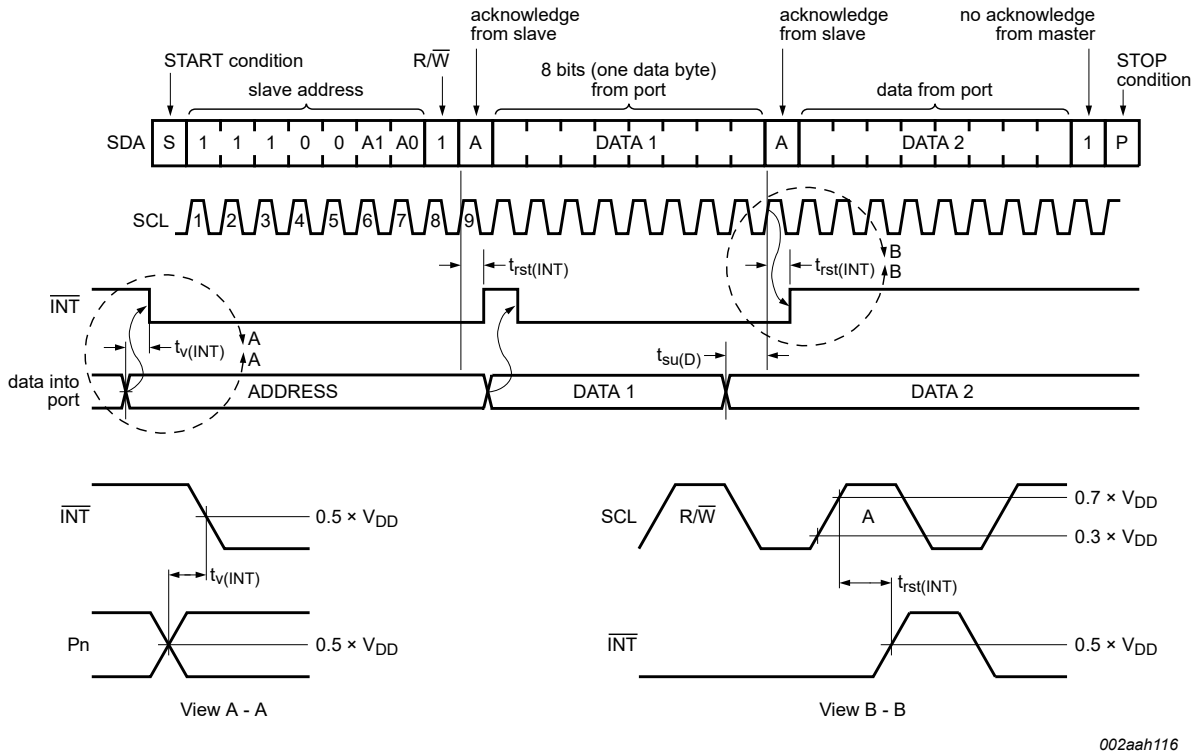


a. Interrupt load configuration



b. Voltage waveforms

C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

Figure 32. Interrupt load circuit and voltage waveforms

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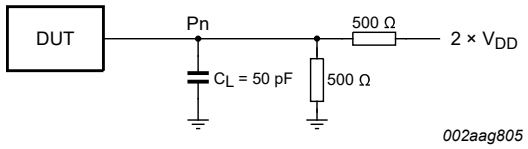
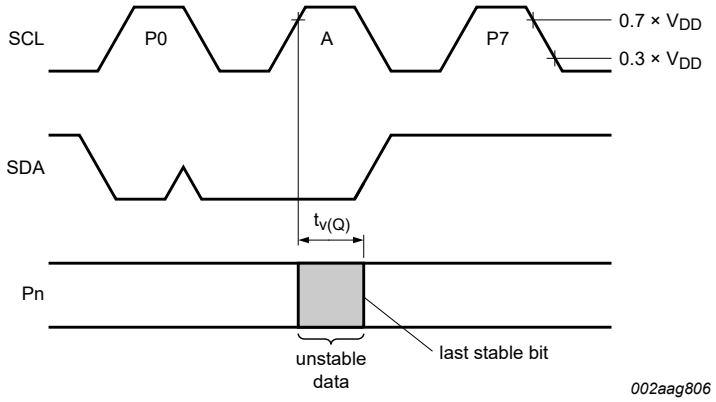
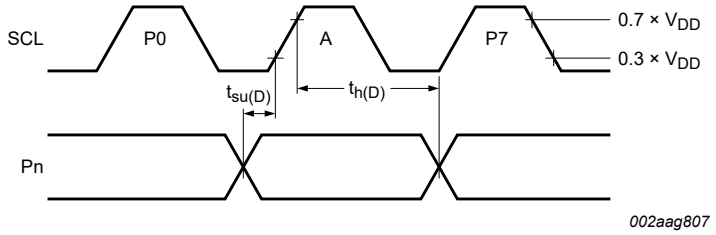


a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.
$t_{v(Q)}$ is measured from 0.7 × V_{DD} on SCL to 50 % I/O (Pn) output.
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.
The outputs are measured one at a time, with one transition per measurement.
All parameters and waveforms are not applicable to all devices.

Figure 33. P port load circuit and voltage waveforms

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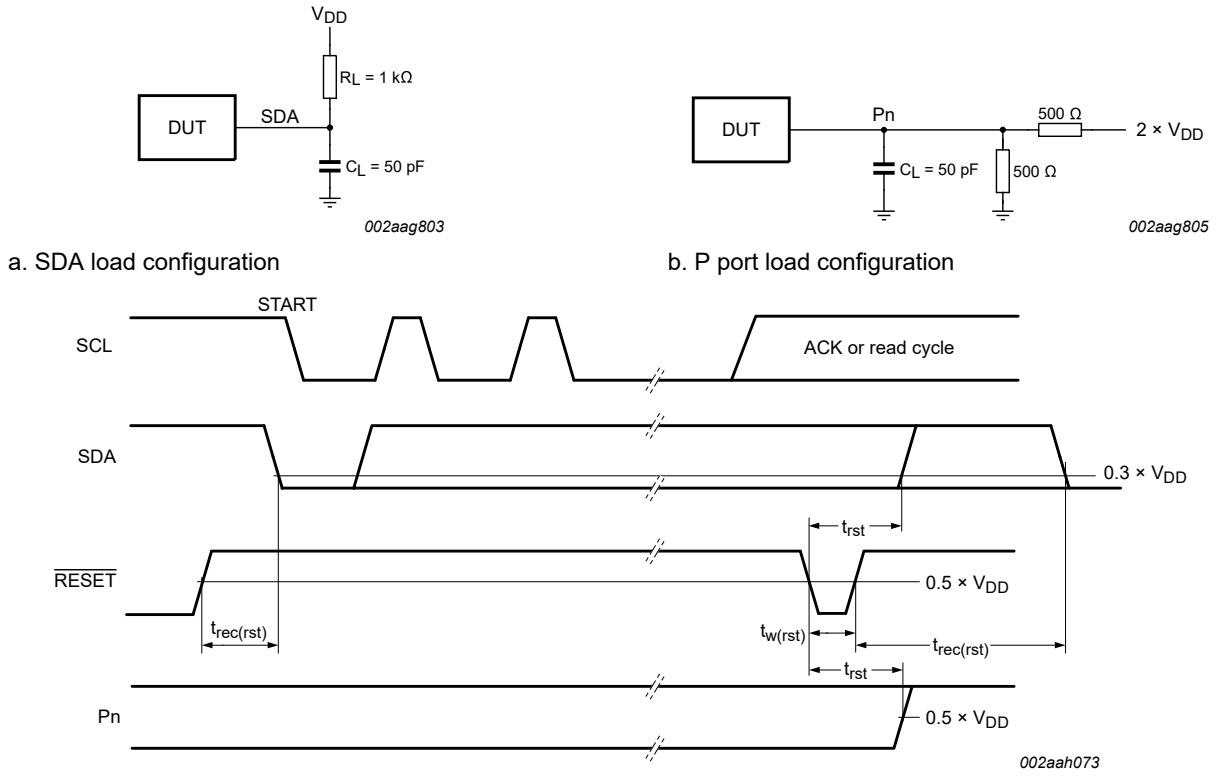

C_L includes probe and jig capacitance.
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.
The outputs are measured one at a time, with one transition per measurement.
I/Os are configured as inputs.
All parameters and waveforms are not applicable to all devices.

Figure 34. Reset load circuits and voltage waveforms

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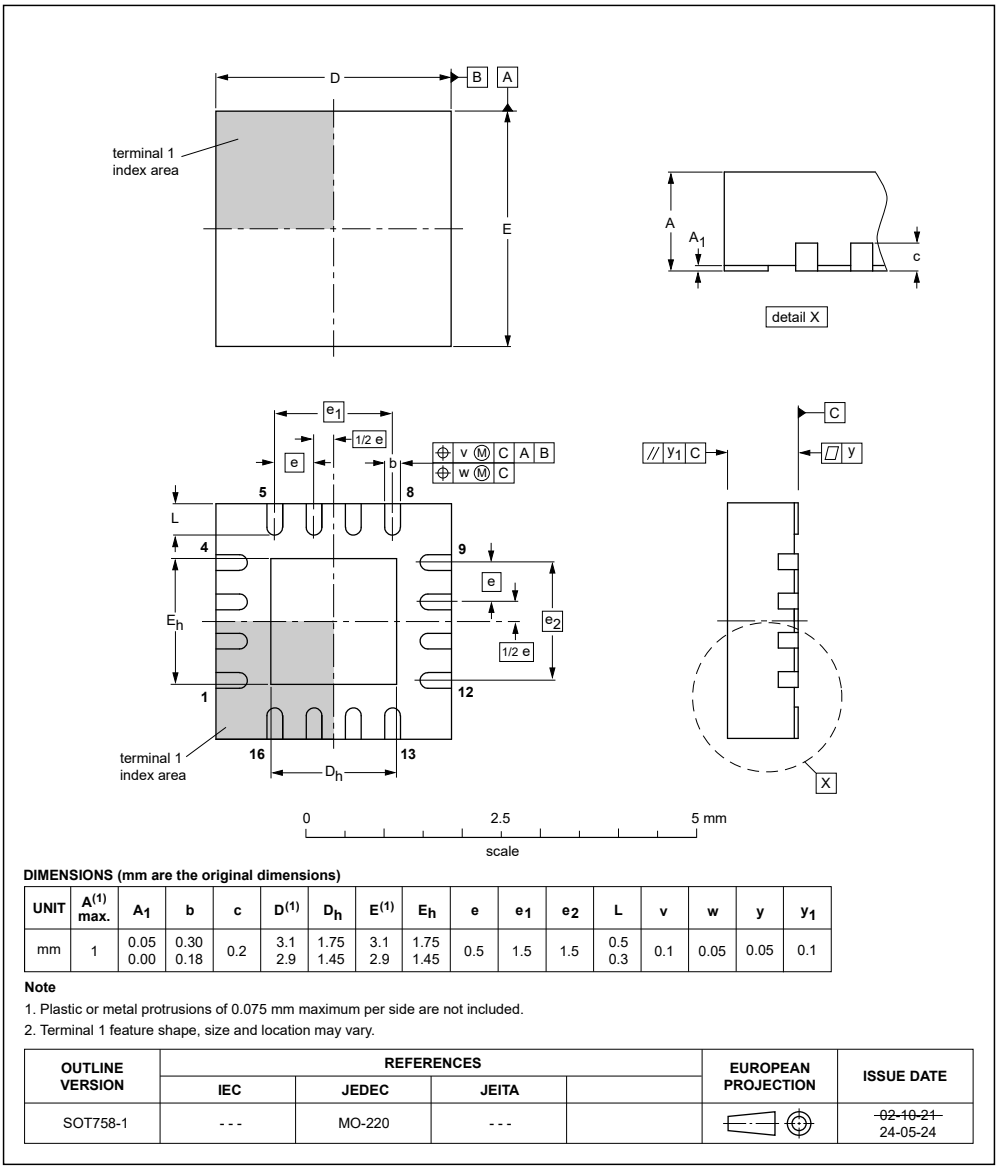
15 Package outline

This section shows the package outline for the PCAL9538A.

HVQFN16: plastic, thermal enhanced very thin quad flatpack; no leads; 16 terminals; 3 mm x 3 mm x 0.85 mm body **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.
2. Terminal 1 feature shape, size and location may vary.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-10-21~~ 24-05-24

Figure 35. Package outline SOT758-1 (HVQFN16)

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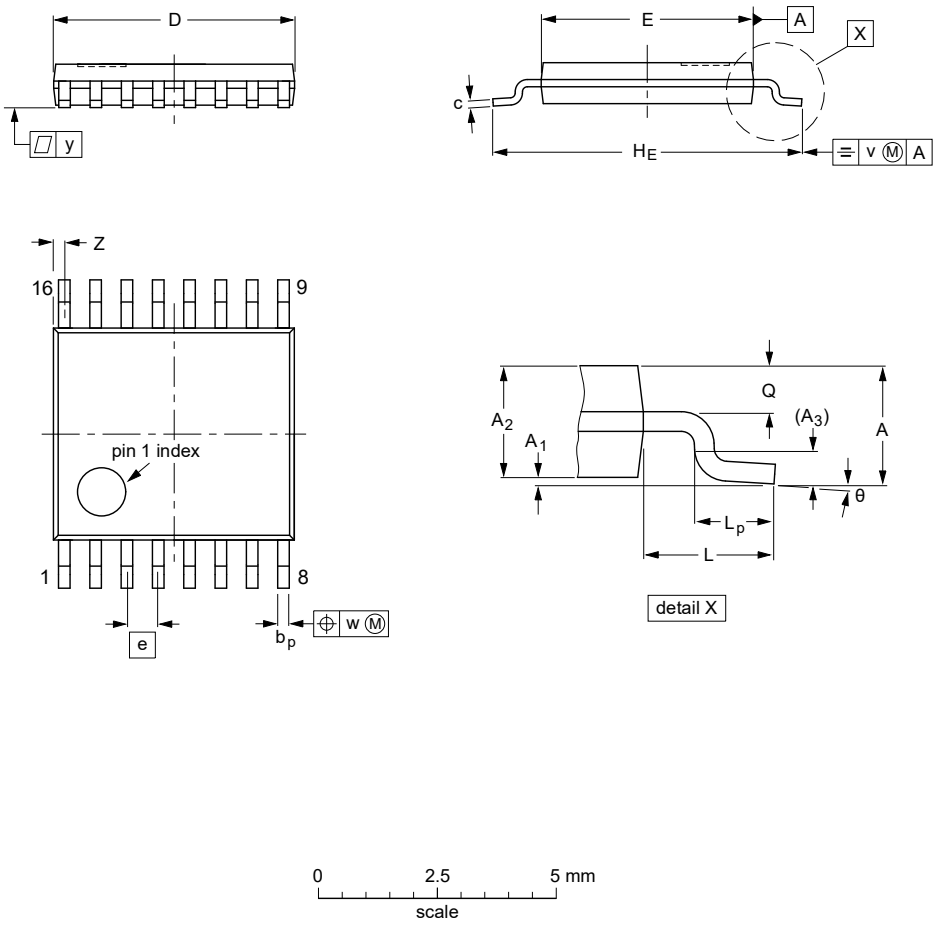
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Figure 36. Package outline SOT403-1 (TSSOP16)

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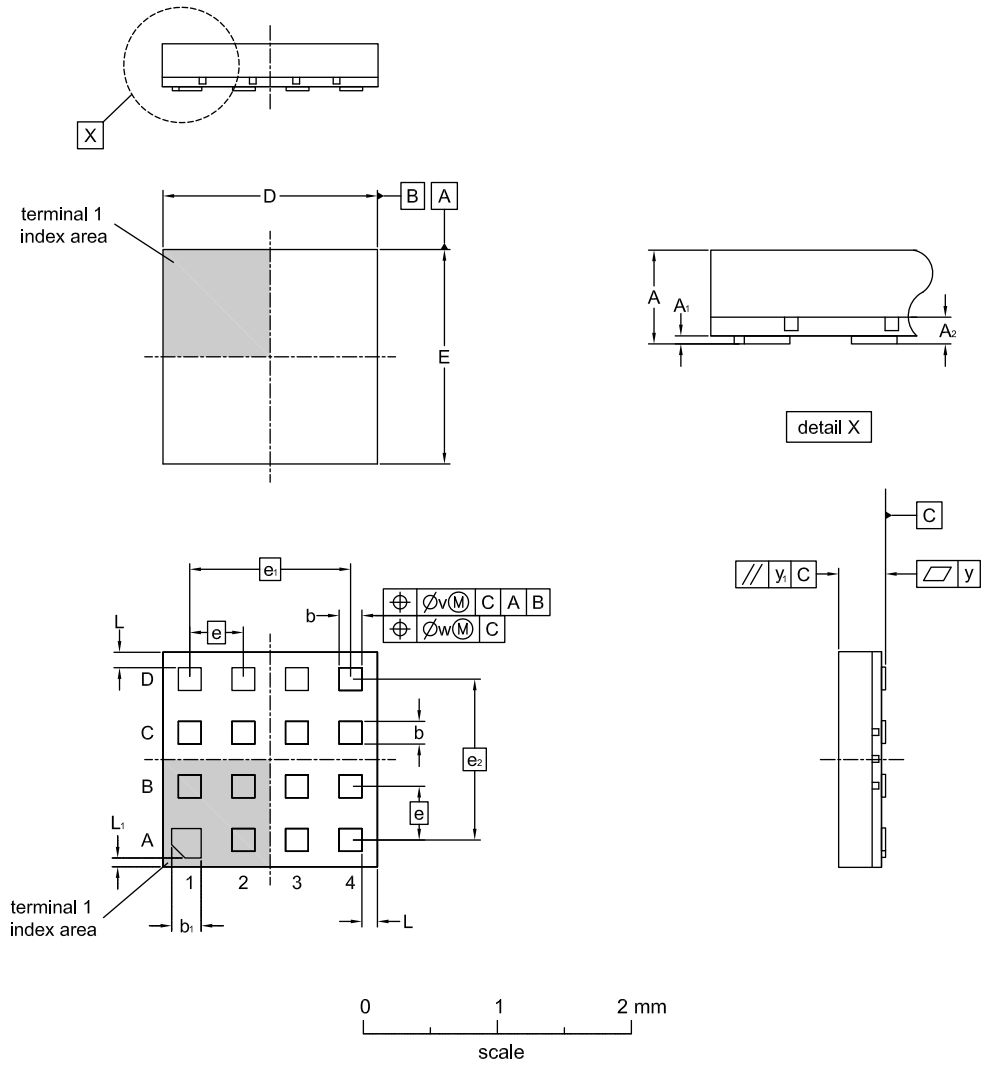
X2QFN16: plastic, thermal enhanced super thin quad flat package; no leads; 16 terminals; 1.6 mm x 1.6 mm x 0.35 mm body **SOT1896-1**



Dimensions (mm are the original dimensions)

UNIT		A	A_1	A_2	b	b_1	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	MAX	0.40	0.05		0.22	0.27	1.70	1.70									
	NOM	0.35		0.10	0.17	0.22	1.60	1.60	0.4	1.2	1.2	0.12	0.065	0.15	0.05	0.10	0.10
	MIN	0.30	0.00		0.12	0.17	1.50	1.50									

sot1896-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1896-1	- - -	- - -	- - -			~~16-08-17~~ 17-06-26

Figure 37. Package outline SOT1896-1 (X2QFN16)

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16 Handling information

Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

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17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 38) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

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- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 26 and Table 27

Table 26. SnPb eutectic process (from J-STD-020D)

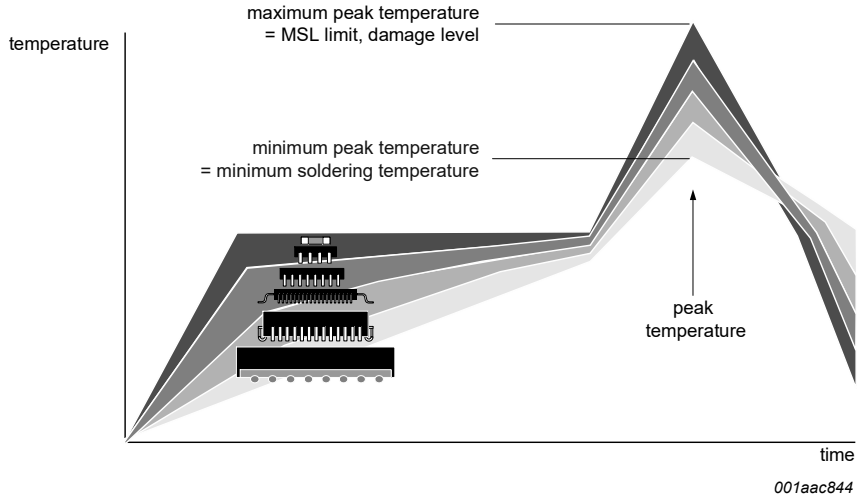
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 27. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 38.



MSL: Moisture Sensitivity Level

Figure 38. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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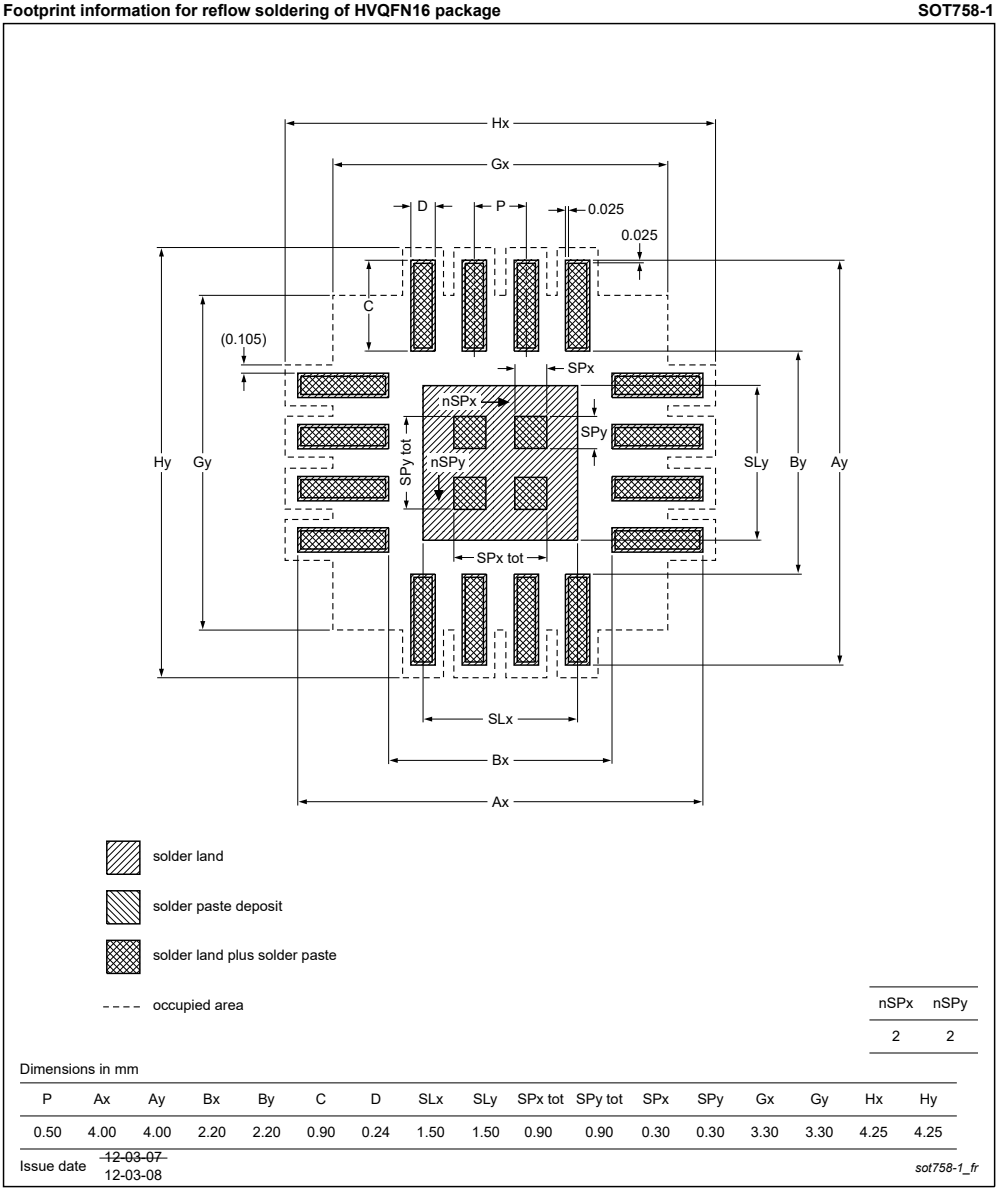
18 Soldering: PCB footprints

This section shows the PCB footprint information for the PCAL9538A.

Footprint information for reflow soldering of HVQFN16 package **SOT758-1**



nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.50	4.00	4.00	2.20	2.20	0.90	0.24	1.50	1.50	0.90	0.90	0.30	0.30	3.30	3.30	4.25	4.25

Issue date ~~12-03-07~~ 12-03-08 *sot758-1_fr*

Figure 39. PCB footprint for SOT758-1 (HVQFN16); reflow soldering

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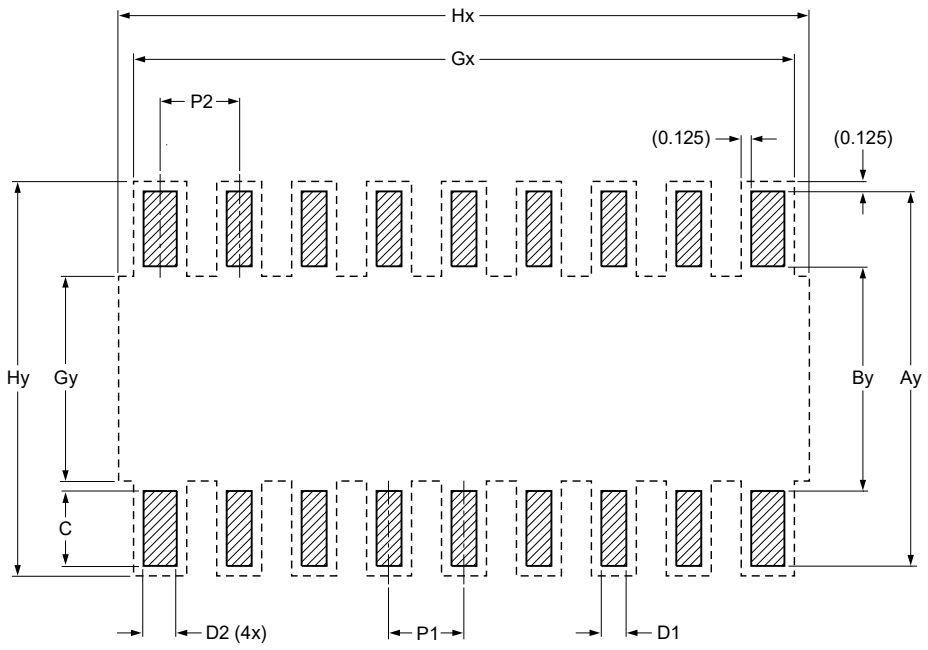
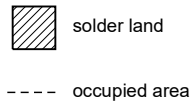
Footprint information for reflow soldering of TSSOP16 package **SOT403-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout



DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Figure 40. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

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Footprint information for reflow soldering of X2QFN16 package **SOT1896-1**

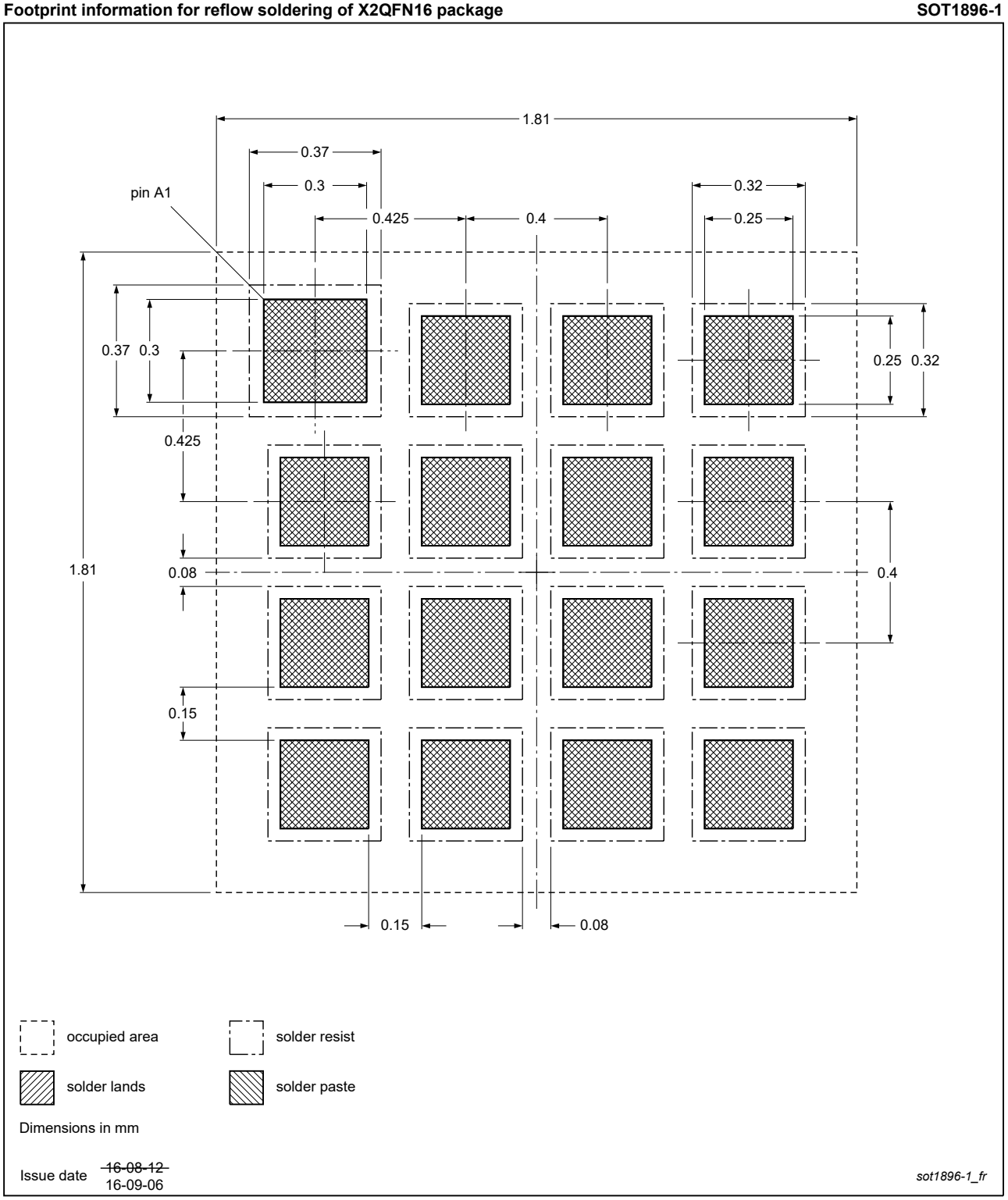

Figure 41. PCB footprint for SOT1896-1 (X2QFN16); reflow soldering

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19 Acronyms

Table 28 describes the acronyms used in this datasheet.

Table 28. Acronyms

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General-Purpose Input/Output
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
LP	Low-Pass
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed Circuit Board
POR	Power-On Reset
PRR	Pulse Repetition Rate
SCL	Serial Clock Line
SCR	Silicon Controlled Rectifier
SDA	Serial Data Line
SMBus	System Management Bus
SMD	Surface-Mount Device

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20 Revision history

Table 29 summarizes revisions to this document.

Table 29. Revision history

Document ID	Release date	Description
PCAL9538A v.4.0	28 August 2026	Added information for the X2QFN16 package in as per CIN# 202608025I: • Section 3 "Ordering information" • Section 3.1 "Ordering options" • Section 5.1 "Pinning" • Section 5.2 "Pin description" • Section 15 "Package outline" • Section 18 "Soldering: PCB footprints" Editorial fixes
PCAL9538A v.3.1	27 May 2015	Updated: • Section 2.1 "Agile I/O features": Part type corrected from "PCA9539 and PCA9539A" to "PCA9538 and PCA9538A"
PCAL9538A v.3.0	9 August 2013	• Product data sheet
PCAL9538A v.2.0	10 December 2012	• Product data sheet
PCAL9538A v.1.0	28 September 2012	• Initial public release

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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