# 4M-BIT [512K x 8 / 256K x 16] SINGLE VOLTAGE 5V ONLY FLASH MEMORY

## FEATURES

### GENERAL FEATURES

- Single Power Supply Operation
  - 4.5 to 5.5 volt for read, erase, and program operations
- 524,288 x 8 / 262,144 x 16 switchable
- Boot Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Sector Structure
  - 16K-Byte x 1, 8K-Byte x 2, 32K-Byte x 1, and 64K-Byte x 7
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Temporary sector unprotected allows code changes in previously locked sectors
- Latch-up protected to 100mA from -1V to Vcc + 1V
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash

### PERFORMANCE

- High Performance
  - Access time: 70/90ns
  - Byte/Word program time: 9us/11us (typical)
  - Erase time: 0.7s/sector, 4s/chip (typical)
- Low Power Consumption
  - Low active read current: 40mA (maximum) at 5MHz
  - Low standby current: 1uA (typical)
- Minimum 100,000 erase/program cycle
- 20 years data retention

### SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion

### HARDWARE FEATURES

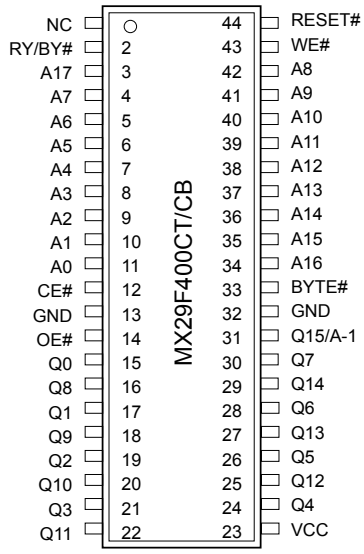
- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode

### PACKAGE

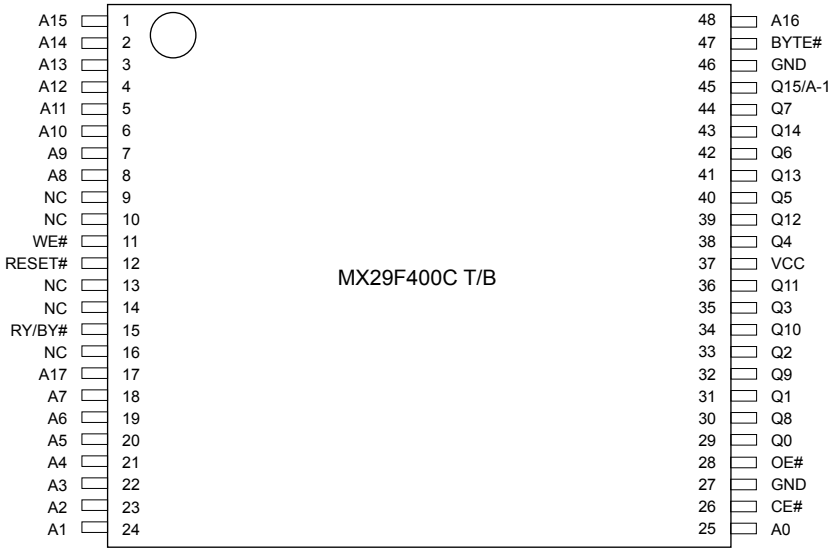
- 44-Pin SOP
- 48-Pin TSOP
- **All devices are RoHS Compliant**
- **All non RoHS Compliant devices are not recommeded for new design in**

## PIN CONFIGURATIONS

### 44 SOP(500mil)



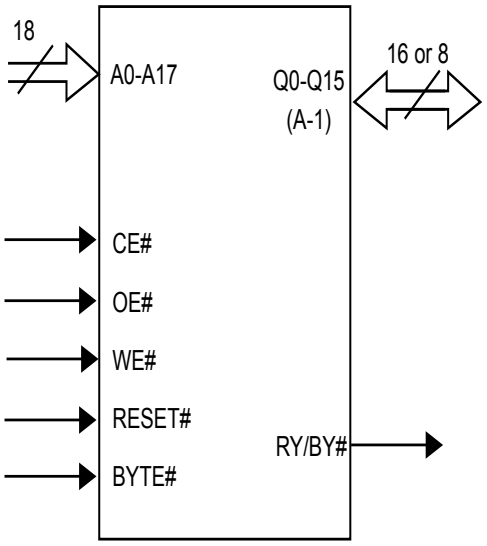

### 48 TSOP(TYPE I) (12mm x 20mm)



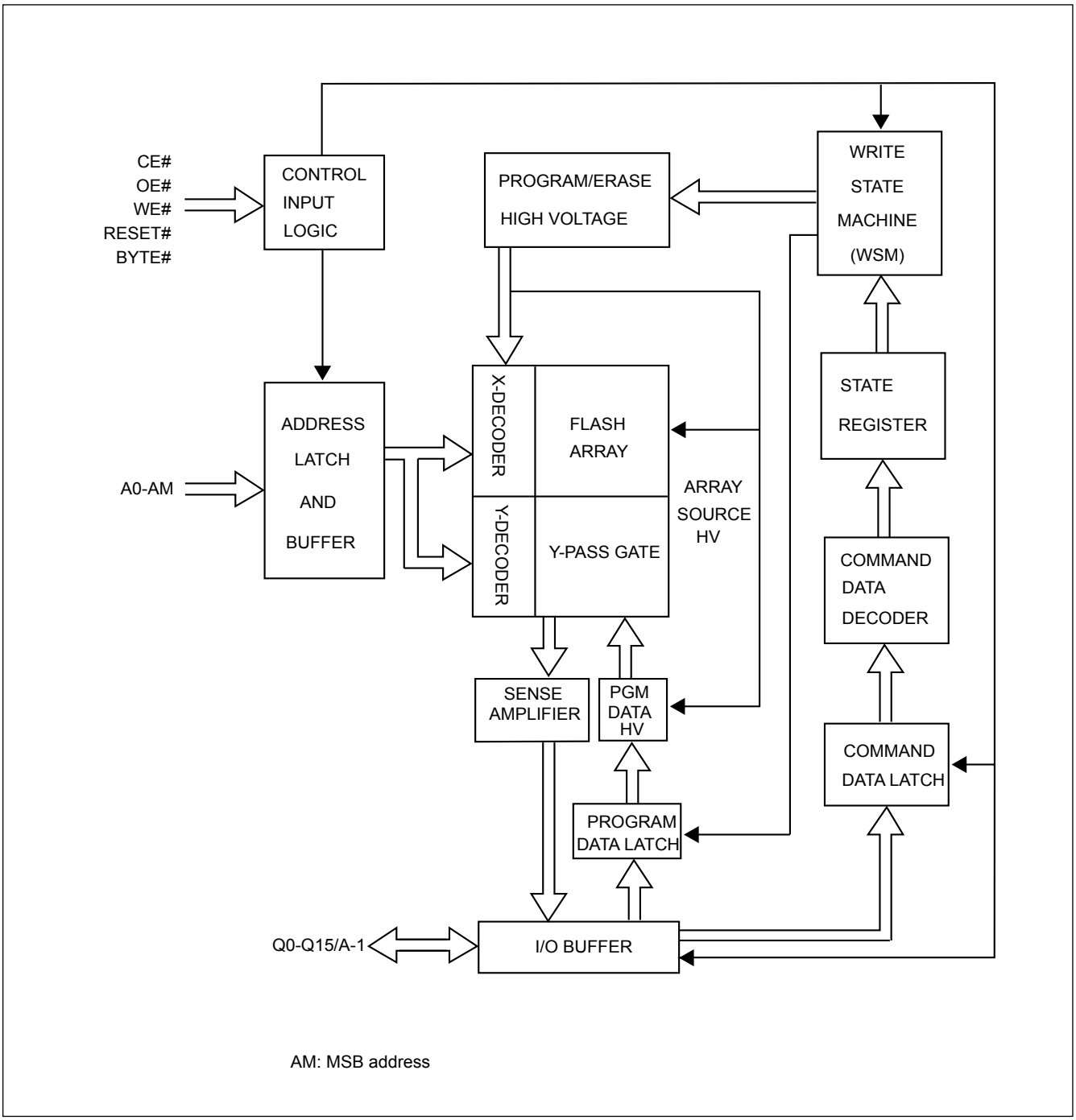
## PIN DESCRIPTION

| SYMBOL | PIN NAME |
|---|---|
| A0~A17 | Address Input |
| Q0~Q14 | Data Input/Output |
| Q15/A-1 | Q15(Word mode)/LSB addr(Byte mode) |
| CE# | Chip Enable Input |
| WE# | Write Enable Input |
| BYTE# | Word/Byte Selection input |
| RESET# | Hardware Reset Pin/Sector Protect Unlock |
| OE# | Output Enable Input |
| RY/BY# | Ready/Busy Output |
| VCC | Power Supply Pin (+5V) |
| GND | Ground Pin |

## LOGIC SYMBOL



## BLOCK DIAGRAM



## Table 1. SECTOR STRUCTURE

### MX29F400CT TOP BOOT SECTOR ADDRESS TABLE

| Sector | A17 | A16 | A15 | A14 | A13 | A12 | Sector Size (Kbytes/ Kwords) | Address Range (in hexadecimal) | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | (x8) Address Range | (x16) Address Range |
| SA0 | 0 | 0 | 0 | X | X | X | 64/32 | 00000h-0FFFFh | 00000h-07FFFh |
| SA1 | 0 | 0 | 1 | X | X | X | 64/32 | 10000h-1FFFFh | 08000h-0FFFFh |
| SA2 | 0 | 1 | 0 | X | X | X | 64/32 | 20000h-2FFFFh | 10000h-17FFFh |
| SA3 | 0 | 1 | 1 | X | X | X | 64/32 | 30000h-3FFFFh | 18000h-1FFFFh |
| SA4 | 1 | 0 | 0 | X | X | X | 64/32 | 40000h-4FFFFh | 20000h-27FFFh |
| SA5 | 1 | 0 | 1 | X | X | X | 64/32 | 50000h-5FFFFh | 28000h-2FFFFh |
| SA6 | 1 | 1 | 0 | X | X | X | 64/32 | 60000h-6FFFFh | 30000h-37FFFh |
| SA7 | 1 | 1 | 1 | 0 | X | X | 32/16 | 70000h-77FFFh | 38000h-3BFFFh |
| SA8 | 1 | 1 | 1 | 1 | 0 | 0 | 8/4 | 78000h-79FFFh | 3C000h-3CFFFh |
| SA9 | 1 | 1 | 1 | 1 | 0 | 1 | 8/4 | 7A000h-7BFFFh | 3D000h-3DFFFh |
| SA10 | 1 | 1 | 1 | 1 | 1 | X | 16/8 | 7C000h-7FFFFh | 3E000h-3FFFFh |

### MX29F400CB BOTTOM BOOT SECTOR ADDRESS TABLE

| Sector | A17 | A16 | A15 | A14 | A13 | A12 | Sector Size (Kbytes/ Kwords) | Address Range (in hexadecimal) | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | (x8) Address Range | (x16) Address Range |
| SA0 | 0 | 0 | 0 | 0 | 0 | X | 16/8 | 00000h-03FFFh | 00000h-01FFFh |
| SA1 | 0 | 0 | 0 | 0 | 1 | 0 | 8/4 | 04000h-05FFFh | 02000h-02FFFh |
| SA2 | 0 | 0 | 0 | 0 | 1 | 1 | 8/4 | 06000h-07FFFh | 03000h-03FFFh |
| SA3 | 0 | 0 | 0 | 1 | X | X | 32/16 | 08000h-0FFFFh | 04000h-07FFFh |
| SA4 | 0 | 0 | 1 | X | X | X | 64/32 | 10000h-1FFFFh | 08000h-0FFFFh |
| SA5 | 0 | 1 | 0 | X | X | X | 64/32 | 20000h-2FFFFh | 10000h-17FFFh |
| SA6 | 0 | 1 | 1 | X | X | X | 64/32 | 30000h-3FFFFh | 18000h-1FFFFh |
| SA7 | 1 | 0 | 0 | X | X | X | 64/32 | 40000h-4FFFFh | 20000h-27FFFh |
| SA8 | 1 | 0 | 1 | X | X | X | 64/32 | 50000h-5FFFFh | 28000h-2FFFFh |
| SA9 | 1 | 1 | 0 | X | X | X | 64/32 | 60000h-6FFFFh | 30000h-37FFFh |
| SA10 | 1 | 1 | 1 | X | X | X | 64/32 | 70000h-7FFFFh | 38000h-3FFFFh |

**Note:** Address range is A17~A-1 in byte mode and A17~A0 in word mode.

**Table 2. BUS OPERATION**

| Mode / Pins | CE# | OE# | WE# | RESET# | A0 | A1 | A6 | A9 | Q0 ~ Q15 |
|---|---|---|---|---|---|---|---|---|---|
| Read Silicon ID Manufacture Code | L | L | H | H | L | L | X | Vhv | C2H (Byte mode) 00C2H (Word mode) |
| Read Silicon ID Device Code | L | L | H | H | H | L | X | Vhv | 23H/ABH (Byte mode) 2223H/22ABH (Word mode) |
| Read | L | L | H | H | A0 | A1 | A6 | A9 | $D_{OUT}$ |
| Standby | H | X | X | H | X | X | X | X | HIGH Z |
| Output Disable | L | H | H | H | X | X | X | X | HIGH Z |
| Write | L | H | L | H | A0 | A1 | A6 | A9 | $D_{IN}$ |
| Sector Protect | L | H | L | Vhv | L | H | L | X | $D_{IN}$ |
| Chip Unprotect | L | H | L | Vhv | L | H | H | X | $D_{IN}$ |
| Verify Sector Protect/ Unprotect | L | L | H | H | L | H | L | Vhv | Code(4) |
| Reset | X | X | X | L | X | X | X | X | HIGH Z |

**Notes:**
1. Vhv is the very high voltage, 11.5V to 12.5V.
2. X means input high (Vih) or input low (Vil).
3. SA means sector address: A12~A17.
4. Code=00H/XX00H means unprotected.
   Code=01H/XX01H means protected.

## REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array out. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped after a period of time no more than Treadyand the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

## WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

## RESET# OPERATION

Driving RESET# pin low for a period more than Trp will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of Tready for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at GND±0.3V, the device consumes standby current(Isb).However, device draws larger current if RESET# pin is held at Vil but not within GND±0.3V.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

## SECTOR PROTECT OPERATION

When a sector is protected, program or erase operation will be disabled on these sectors. MX29F400C T/B provides one method for sector protection.

Once the sector is protected, the sector remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at Vhv. Refer to temporary sector unprotect operation for further details.

This method is by applying Vhv on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for the algorithm for this method.

## CHIP UNPROTECT OPERATION

MX29F400C T/B provides one method for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sector are unprotected when shipped from the factory.

This method is by applying Vhv on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for algorithm of the operation.

## TEMPORARY SECTOR UNPROTECT OPERATION

System can apply RESET# pin at Vhv to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The devices returns to normal operation once Vhv is removed from RESET# pin and previously protected sectors are again protected.

## AUTOMATIC SELECT OPERATION

When the device is in Read array mode or erase-suspended read array mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE# and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

## VERIFY SECTOR PROTECT STATUS OPERATION

MX29F400C T/B provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires $V_{hv}$ on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A12 to A17 pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is still not being protected.

## DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

## WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

## LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

## POWER-UP SEQUENCE

Upon power up, MX29F400C T/B is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

## POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

## POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

**TABLE 3. MX29F400C T/B COMMAND DEFINITIONS**

| Command | | Read Mode | Reset Mode | Automatic Select | | | | | | Program | | Chip Erase | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Manufacturer ID | | Device ID | | Sector Protect Verify | | | | | |
| | Hex | | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | Addr | XXX | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA |
| | Data | Data | F0 | AA | AA | AA | AA | AA | AA | AA | AA | AA | AA |
| 2nd Bus Cycle | Addr | | | 2AA | 555 | 2AA | 555 | 2AA | 555 | 2AA | 555 | 2AA | 555 |
| | Data | | | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 |
| 3rd Bus Cycle | Addr | | | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA |
| | Data | | | 90 | 90 | 90 | 90 | 90 | 90 | A0 | A0 | 80 | 80 |
| 4th Bus Cycle | Addr | | | X00 | X00 | X01 | X02 | (Sector) X02 | (Sector) X04 | Addr | Addr | 555 | AAA |
| | Data | | | 00C2 | C2 | ID | ID | XX00/ XX01 | 00/01 | Data | Data | AA | AA |
| 5th Bus Cycle | Addr | | | | | | | | | | | 2AA | 555 |
| | Data | | | | | | | | | | | 55 | 55 |
| 6th Bus Cycle | Addr | | | | | | | | | | | 555 | AAA |
| | Data | | | | | | | | | | | 10 | 10 |

| Command | | Sector Erase | | Erase Suspend | Erase Resume | Sector Protect | |
|---|---|---|---|---|---|---|---|
| | Hex | Word | Byte | | | Word | Byte |
| 1st Bus Cycle | Addr | 555 | AAA | Sector | Sector | XXX | XXX |
| | Data | AA | AA | B0 | 30 | 60 | 60 |
| 2nd Bus Cycle | Addr | 2AA | 555 | | | Sector | Sector |
| | Data | 55 | 55 | | | 60 | 60 |
| 3rd Bus Cycle | Addr | 555 | AAA | | | Sector | Sector |
| | Data | 80 | 80 | | | 40 | 40 |
| 4th Bus Cycle | Addr | 555 | AAA | | | Sector | Sector |
| | Data | AA | AA | | | 00/01 | 00/01 |
| 5th Bus Cycle | Addr | 2AA | 555 | | | | |
| | Data | 55 | 55 | | | | |
| 6th Bus Cycle | Addr | Sector | Sector | | | | |
| | Data | 30 | 30 | | | | |

Notes:
1. Device ID: 2223H/23H for Top Boot Sector device.
   22ABH/ABH for Bottom Boot Sector device.
2. For sector protect verify result, XX00H/00H means sector is not protected, XX01H/01H means sector has been protected.
3. Sector Protect command is valid during Vhv at RESET# pin, Vih at A1 pin and Vil at A0, A6 pins. The last Bus cyc is for protect verify.
4. It is not allowed to adopt any other code which is not in the above command definition table.

## RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode or sector protect verify mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

## AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

| | | Address | Data (Hex) | Representation |
|---|---|---|---|---|
| Manufacturer ID | Word | X00 | 00C2 | |
| | Byte | X00 | C2 | |
| Device ID | Word | X01 | 2223/22AB | Top/Bottom Boot Sector |
| | Byte | X02 | 23/AB | Top/Bottom Boot Sector |
| Sector Protect Verify | Word | (Sector address) X 02 | 00/01 | Unprotected/protected |
| | Byte | (Sector address) X 04 | 00/01 | Unprotected/protected |

There is an alternative method to that shown in Table 2, which is intended for EPROM programmers and requires Vhv on address bit A9.

## AUTOMATIC PROGRAMMING

The MX29F400C T/B can provide the user program function by the form of Byte-Mode or Word-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

With the internal write state controller, the device requires the user to write the program command and data only. The typical chip program time at room temperature of the MX29F400C T/B is 3 seconds. (Word-Mode)

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

| Status | Q7 | Q6 | Q5 | RY/BY#*2 |
|---|---|---|---|---|
| In progress*1 | Q7# | Toggling | 0 | 0 |
| Finished | Q7 | Stop toggling | 0 | 1 |
| Exceed time limit | Q7# | Toggling | 1 | 0 |

*1: The status "in progress" means both program mode and erase-suspended program mode.
*2: RY/BY# is an open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us and the device returns to read array state without programing the data in the protected sector.

## CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware rests or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

| Status | Q7 | Q6 | Q5 | Q2 | RY/BY# |
|---|---|---|---|---|---|
| In progress | 0 | Toggling | 0 | Toggling | 0 |
| Finished | 1 | Stop toggling | 0 | 1 | 1 |
| Exceed time limit | 0 | Toggling | 1 | Toggling | 0 |

## SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector erase or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

| Status | Q7 | Q6 | Q5 | Q3 | Q2 | RY/BY#*2 |
|---|---|---|---|---|---|---|
| Time-out period | 0 | Toggling | 0 | 0 | Toggling | 0 |
| In progress | 0 | Toggling | 0 | 1 | Toggling | 0 |
| Finished | 1 | Stop toggling | 0 | 1 | 1 | 1 |
| Exceed time limit | 0 | Toggling | 1 | 1 | Toggling | 0 |

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptible to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.
*2: RY/BY# is open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us and the device returned to read array status without erasing the data in the protected sector.

## SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1(<=20us) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

| Status | Q7 | Q6 | Q5 | Q3 | Q2 | RY/BY# |
|---|---|---|---|---|---|---|
| Erase suspend read in erase suspended sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| Erase suspend read in non-erase suspended sector | Data | Data | Data | Data | Data | 1 |
| Erase suspend program in non-erase suspended sector | Q7# | Toggle | 0 | N/A | N/A | 0 |

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, and erase resume.

## SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 400us interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

## ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage Range
Vcc . . . . . -0.5V to +7.0 V
RESET#, A9. . . . . -0.5V to +13.5 V
The other pins. . . . . -0.5V to Vcc +0.7 V
Output Short Circuit Current (less than one second) . . . . . 200 mA

Note:
1. Mininum voltage may undershoot to -2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to VCC+2V during transition and for less than 20ns during transitions.

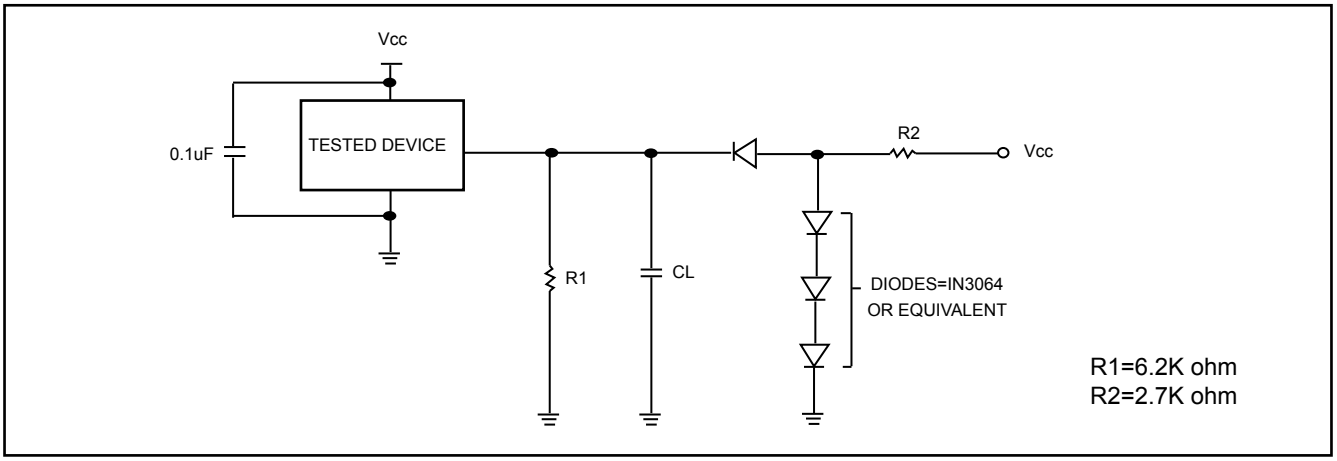
## OPERATING TEMPERATURE AND VOLTAGE

**Commercial (C) Grade**
Surrounding Temperature ($T_A$). . . . . 0°C to +70°C
**Industrial (I) Grade**
Surrounding Temperature ($T_A$). . . . . -40°C to +85°C
**$V_{CC}$ Supply Voltages**
$V_{CC}$ range. . . . . +4.5V to 5.5V

## DC CHARACTERISTICS

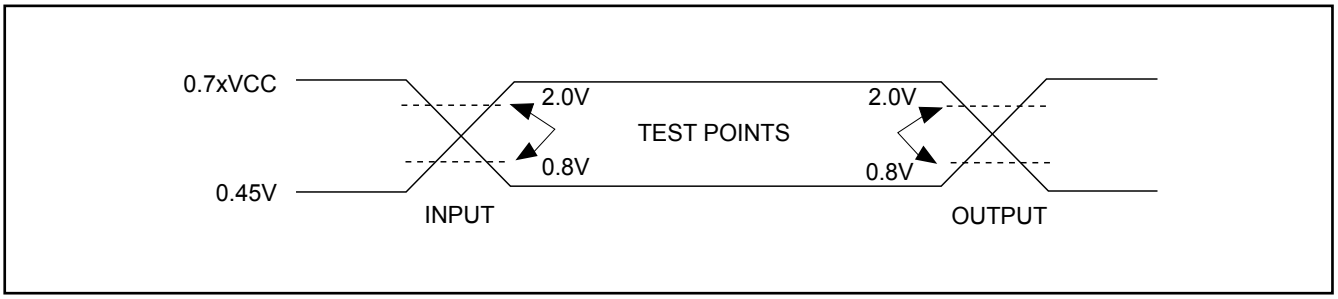
| Symbol | Description | Min | Typ | Max | Remark |
|---|---|---|---|---|---|
| Iilk | Input Leak | | | ± 1.0uA | |
| Iolk | Output Leak | | | 10uA | |
| Icr1 | Read Current (10MHz) | | | 50mA | CE#=Vil,<br>OE#=Vih |
| Icr2 | Read Current (5MHz) | | | 40mA | CE#=Vil,<br>OE#=Vih |
| Isb1 | Standby Current (TTL) | | | 1mA | Vcc=Vcc max,<br>CE#=Vih<br>other pin disabled |
| Isb2 | Standby current (CMOS) | | 1uA | 5uA | Vcc=Vcc max,<br>CE#=vcc +0.3V,<br>other pin disabled |
| Icw | Write Current | | 15mA | 30mA | CE#=Vil, OE#=Vih<br>WE#=Vil |
| Vil | Input Low Voltage | -0.3V | | 0.8V | |
| Vih | Input High Voltage | 0.7xVcc | | Vcc+0.3V | |
| Vhv | Very High Voltage for hardware Protect/ Unprotect/Auto Select/Temporary Unprotect | 11.5V | 12V | 12.5V | |
| Vol | Output Low Voltage | | | 0.45V | Iol=2.1mA,<br>Vcc=Vcc min |
| Voh1 | Ouput High Voltage (TTL) | 2.4V | | | Ioh1=-2mA |
| Voh2 | Ouput High Voltage (CMOS) | Vcc-0.4V | | | Ioh2=-100uA |

## SWITCHING TEST CIRCUITS




Test Condition
Output Load : 1 TTL gate
Output Load Capacitance,CL : 100PF for 90ns ; 30PF for 70ns
Rise/Fall Times : 10ns
Input pulse levels: 0.45V/0.7xVcc
Reference levels for measuring timing :0.8V, 2.0V

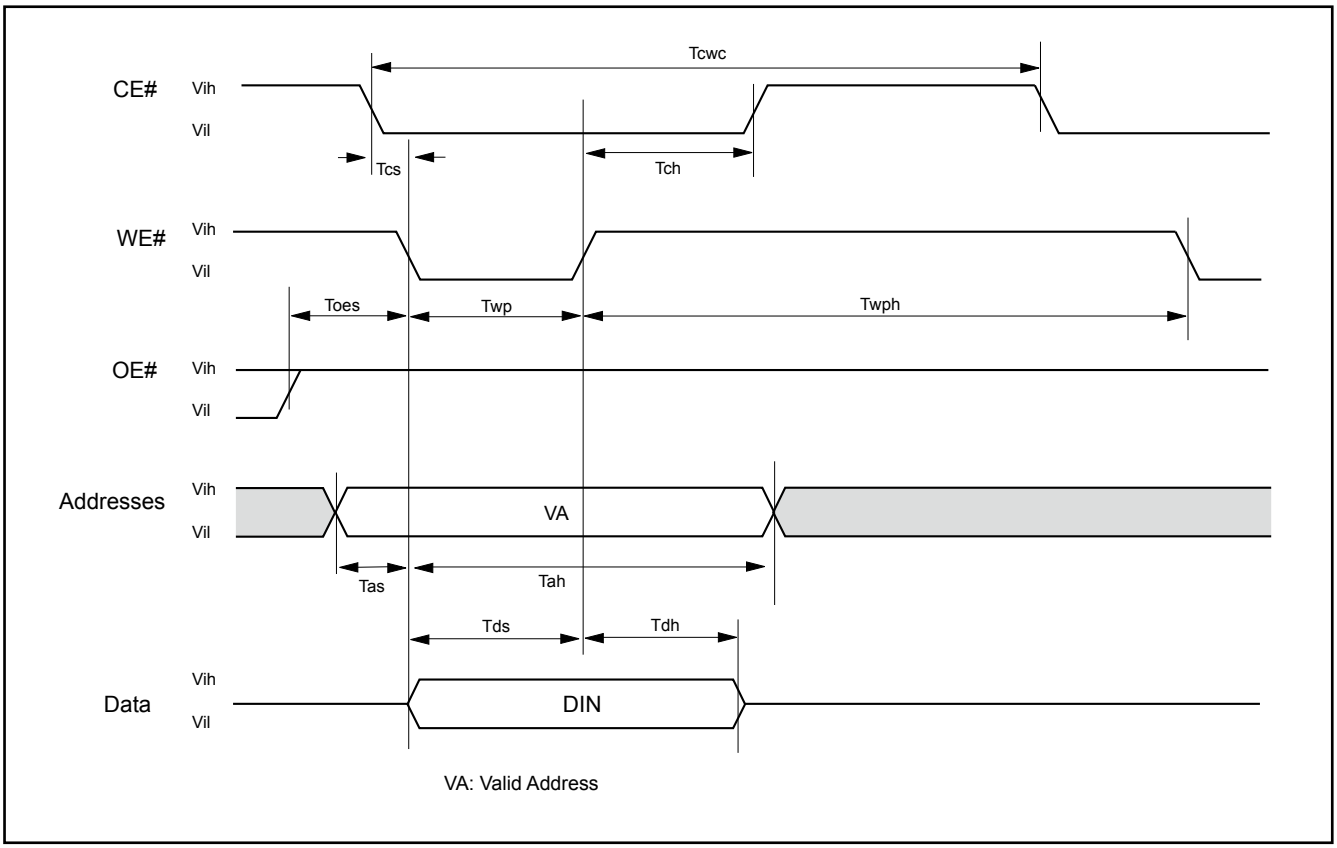
## SWITCHING TEST WAVEFORMS



## AC CHARACTERISTICS

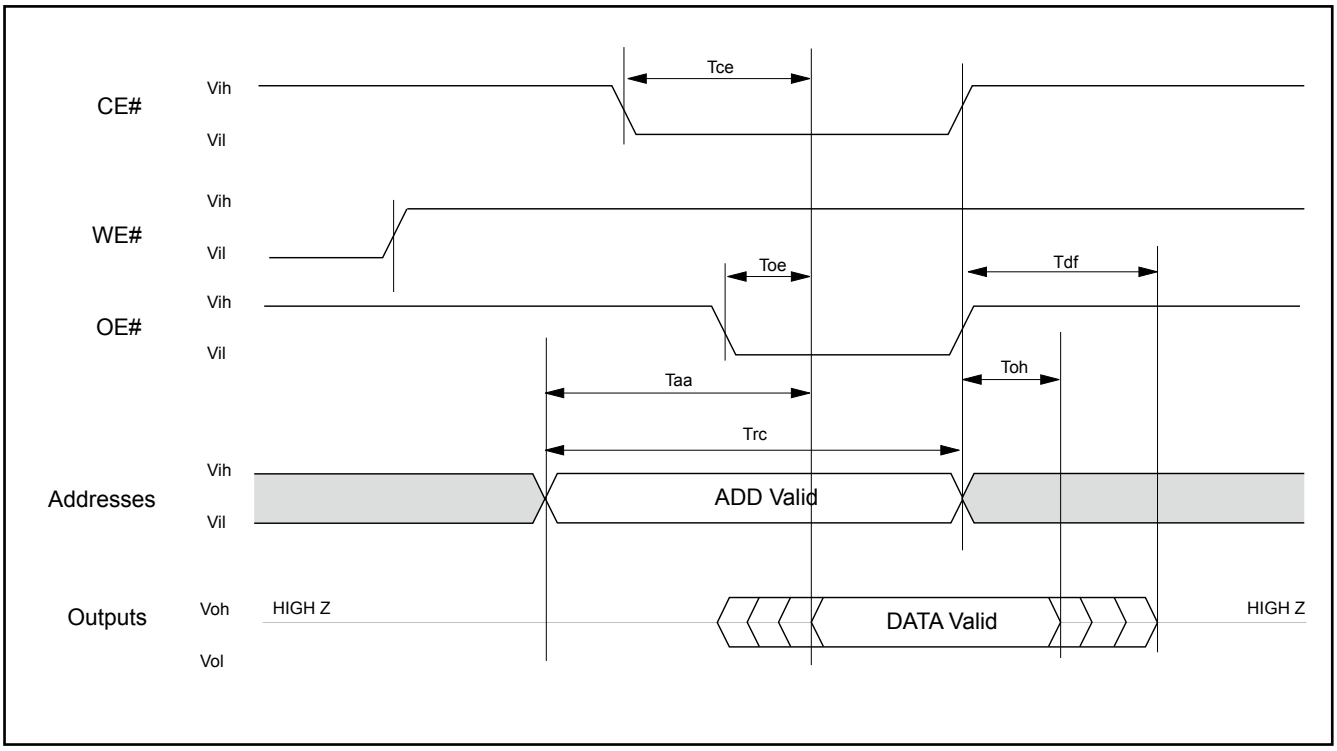
| Symbol | Description | | Speed Option -70/90 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Taa | Valid data output after address | | | | 70/90 | ns |
| Tce | Valid data output after CE# low | | | | 70/90 | ns |
| Toe | Valid data output after OE# low | | | | 30/35 | ns |
| Tdf | Data output floating after OE# high | | | | 20 | ns |
| Toh | Output hold time from the earliest rising edge of Addrss, CE#, OE# | | 0 | | | ns |
| Trc | Read period time | | 70/90 | | | ns |
| Twc | Write period time | | 70/90 | | | ns |
| Tcwc | Command write period time | | 70/90 | | | ns |
| Tas | Address setup time | | 0 | | | ns |
| Tah | Address hold time | | 45 | | | ns |
| Tds | Data setup time | | 30/45 | | | ns |
| Tdh | Data hold time | | 0 | | | ns |
| Tvcs | Vcc setup time | | 50 | | | us |
| Tcs | CE# Setup time | | 0 | | | ns |
| Tch | CE# hold time | | 0 | | | ns |
| Toes | OE# setup time | | 0 | | | ns |
| Toeh | Output enable hold time | Read | 0 | | | ns |
| | | Toggle & Data# Polling | 10 | | | ns |
| Tws | WE# setup time | | 0 | | | ns |
| Twh | WE# hold time | | 0 | | | ns |
| Tcep | CE# pulse width | | 35/45 | | | ns |
| Tceph | CE# pulse width high | | 20 | | | ns |
| Twp | WE# pulse width | | 35 | | | ns |
| Twph | WE# pulse width high | | 30 | | | ns |
| Tghwl | Read recover time before write | | 0 | | | ns |
| Tbusy | Program/Erase active time by RY/BY# | | | | 90 | ns |
| Tavt | Program operation | Byte | | 9 | 300 | us |
| Tavt | Program operation | Word | | 11 | 360 | us |
| Taetc | Chip Erase Operation | | | 4 | 32 | sec |
| Taetb | Sector Erase Operation | | | 0.7 | 8 | sec |
| Tbal | Sector Address hold time | | | | 50 | us |

**Figure 1. COMMAND WRITE OPERATION**



## READ/RESET OPERATION

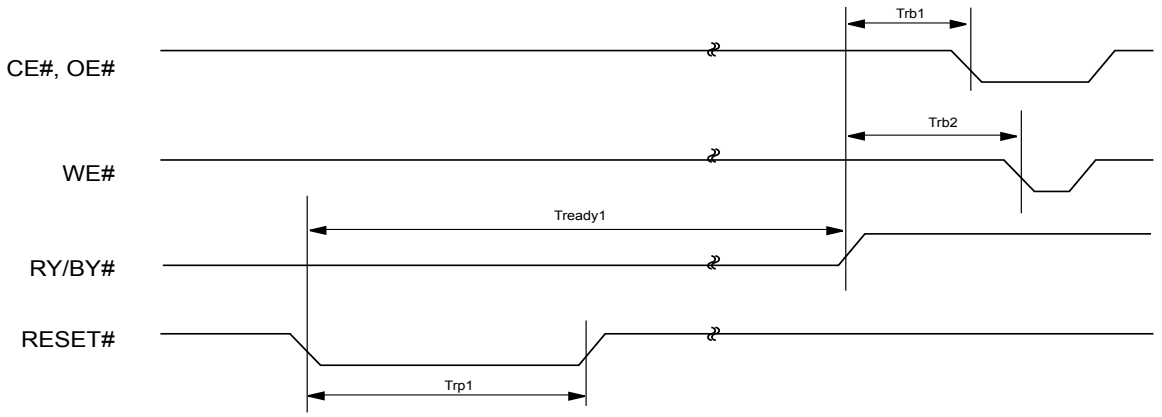
### Figure 2. READ TIMING WAVEFORMS



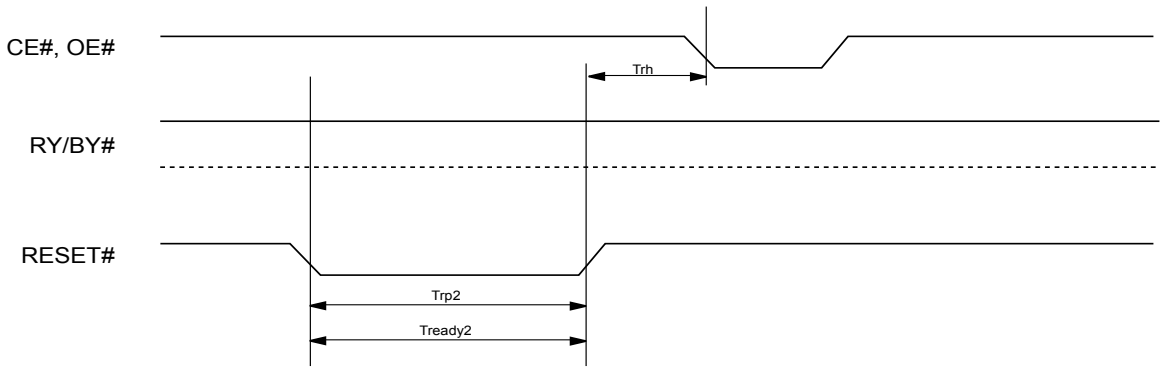
## AC CHARACTERISTICS

| Item | Description | Setup | Speed | Unit |
|---|---|---|---|---|
| Trp1 | RESET# Pulse Width (During Automatic Algorithms) | MIN | 10 | us |
| Trp2 | RESET# Pulse Width (NOT During Automatic Algorithms) | MIN | 500 | ns |
| Trh | RESET# High Time Before Read | MIN | 0 | ns |
| Trb1 | RY/BY# Recovery Time (to CE#, OE# go low) | MIN | 0 | ns |
| Trb2 | RY/BY# Recovery Time (to WE# go low) | MIN | 50 | ns |
| Tready1 | RESET# PIN Low (During Automatic Algorithms) to Read or Write | MAX | 20 | us |
| Tready2 | RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write | MAX | 500 | ns |

**Figure 3. RESET# TIMING WAVEFORM**




Reset Timing during Automatic Algorithms




Reset Timing NOT during Automatic Algorithms

## ERASE/PROGRAM OPERATION

### Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

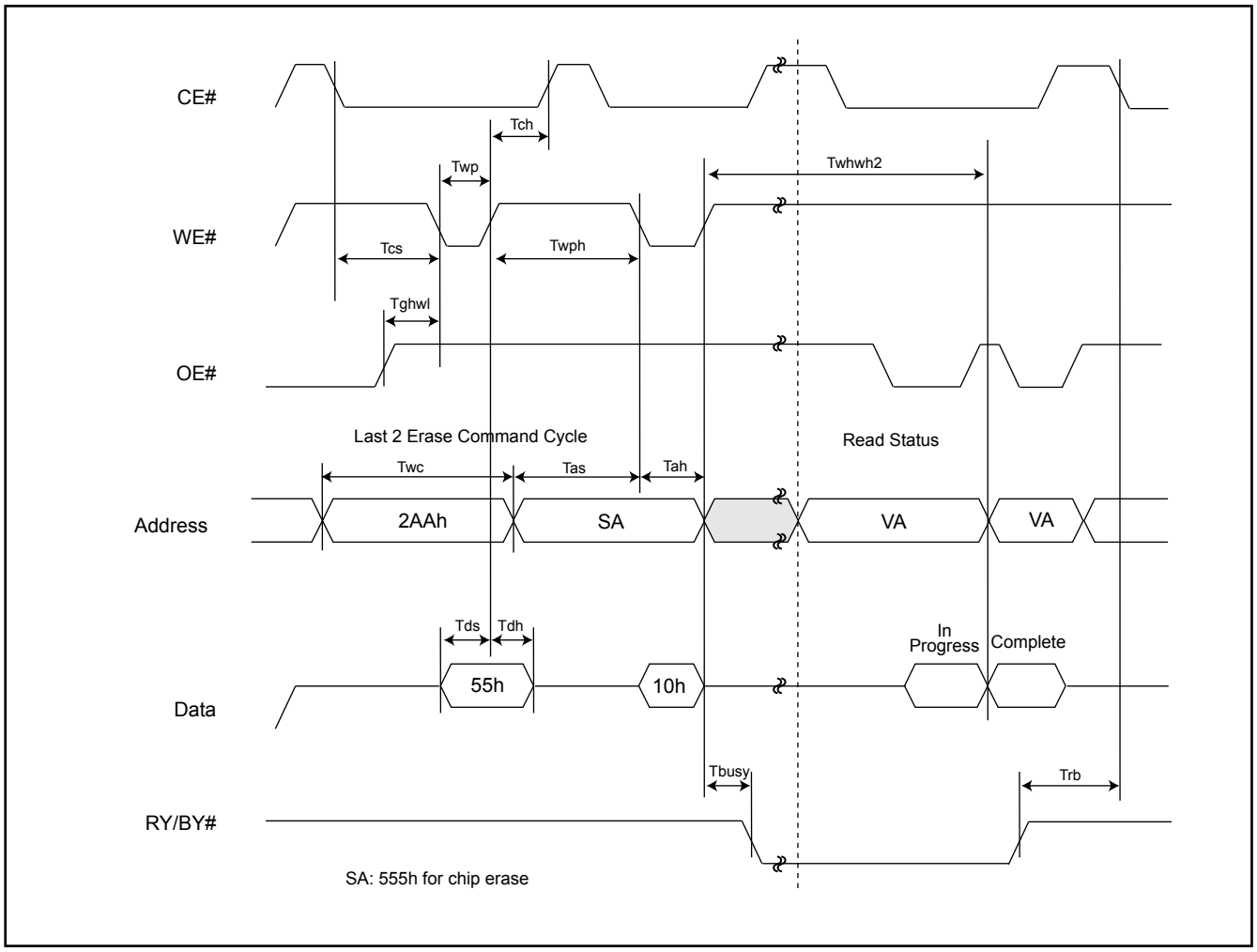


**Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART**

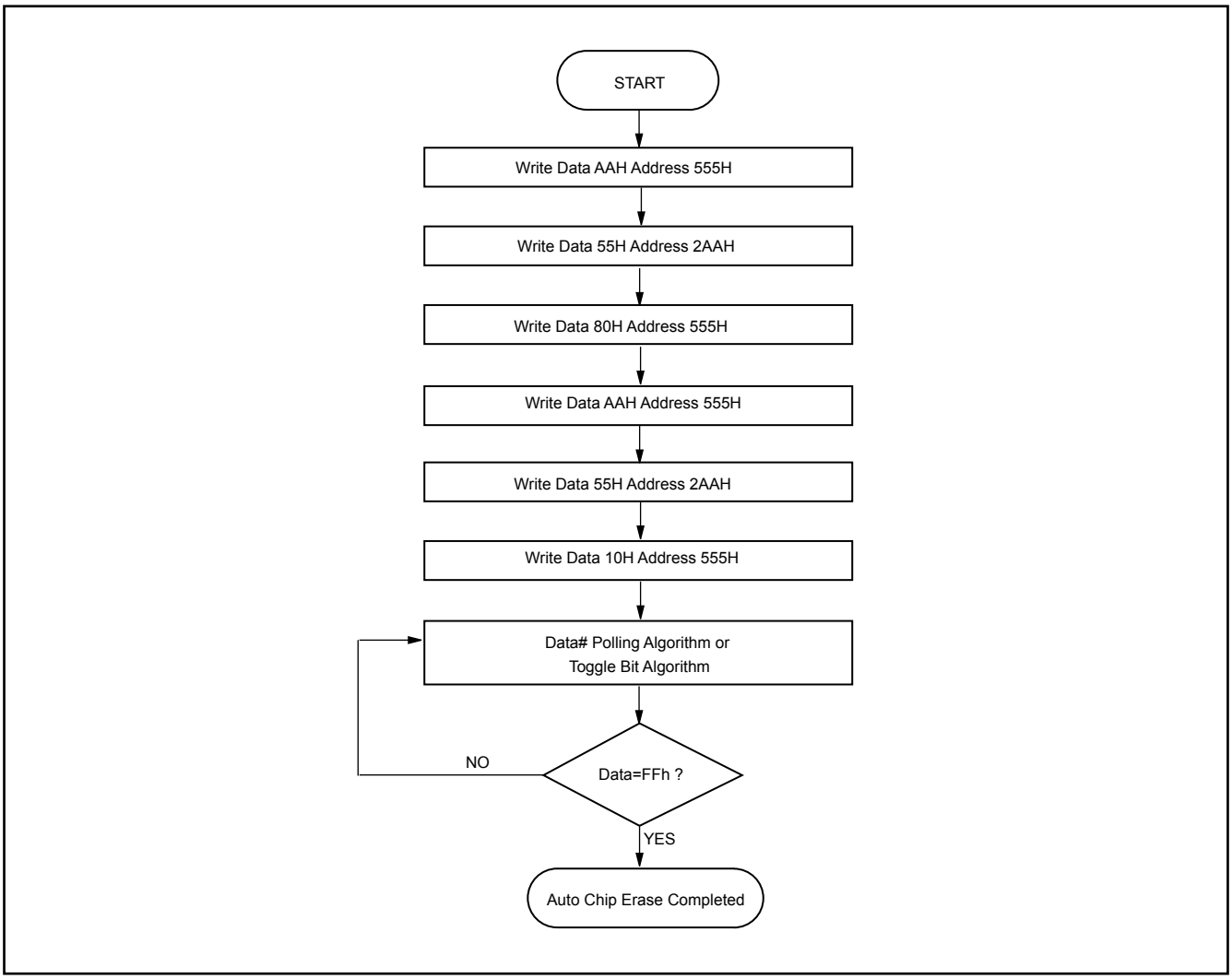


**Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM**

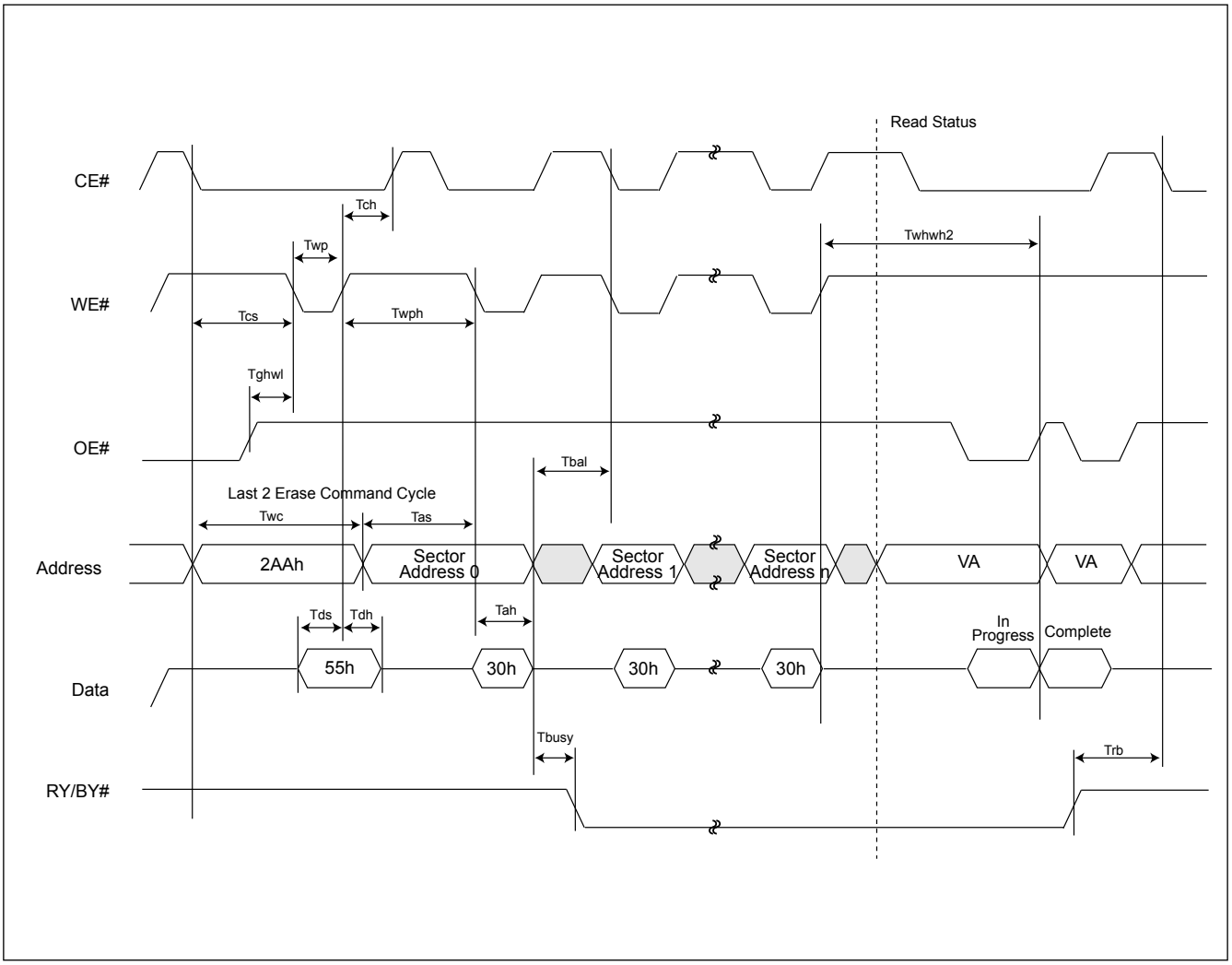


**Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART**

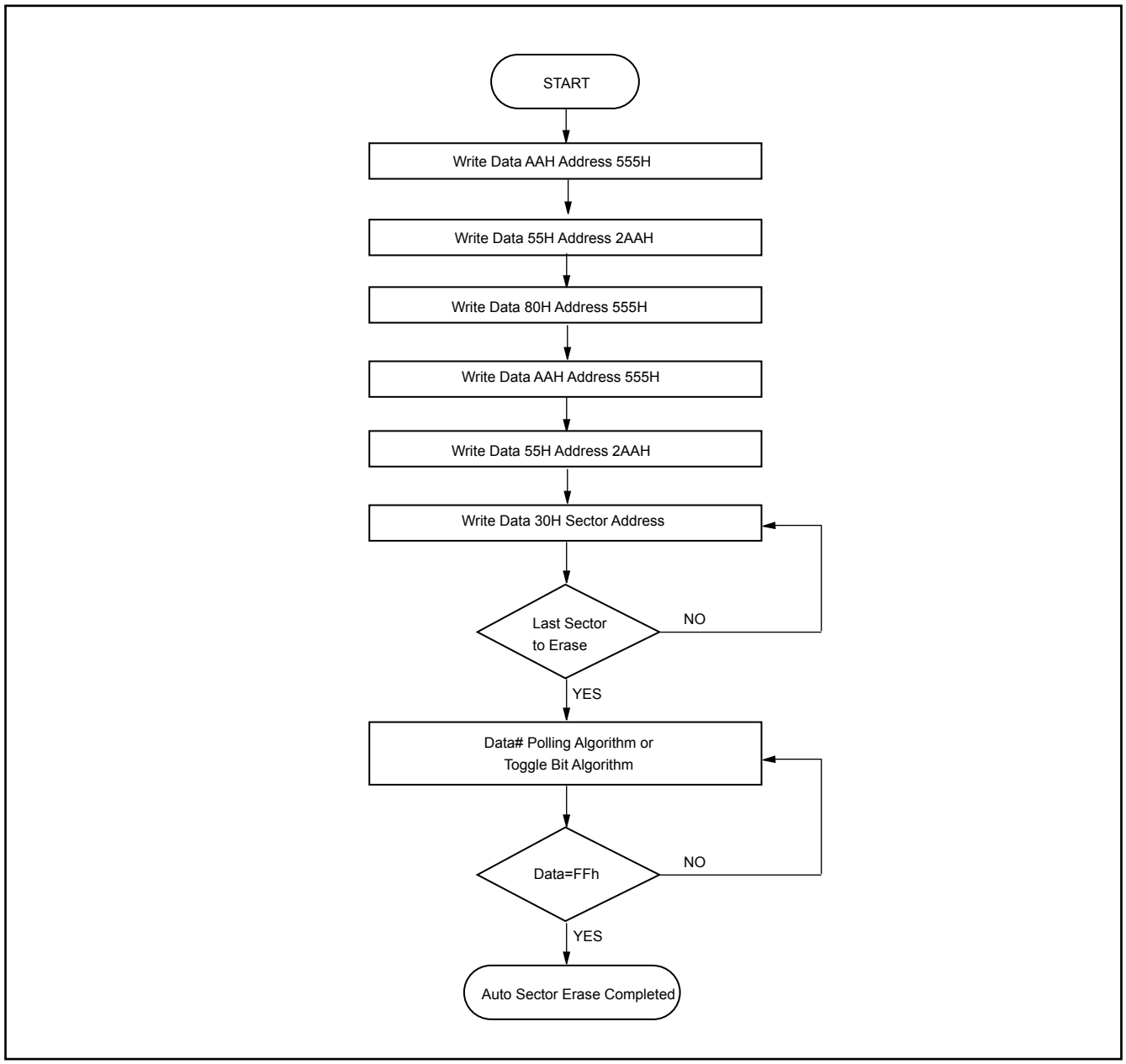


**Figure 8. ERASE SUSPEND/RESUME FLOWCHART**

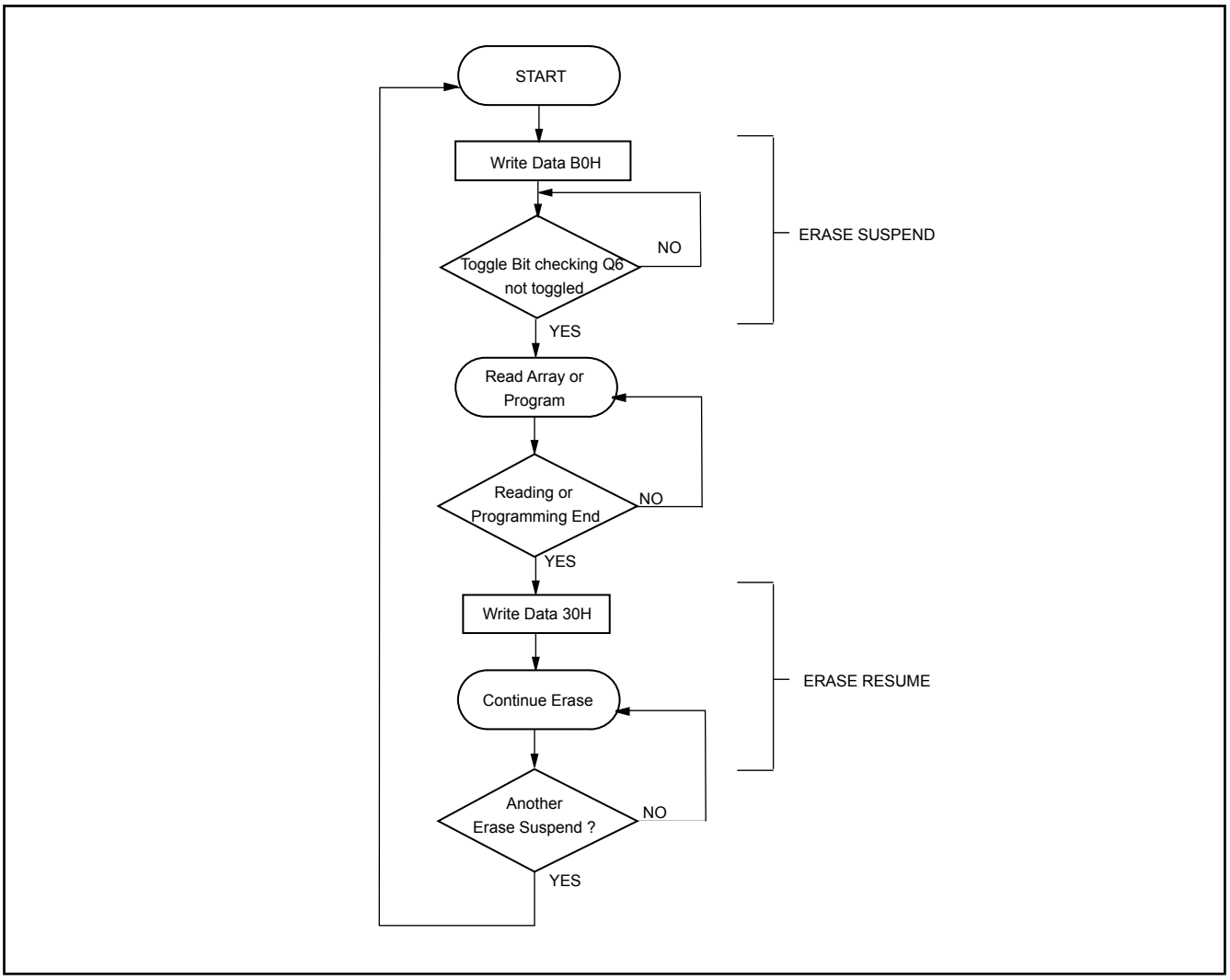


**Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS**

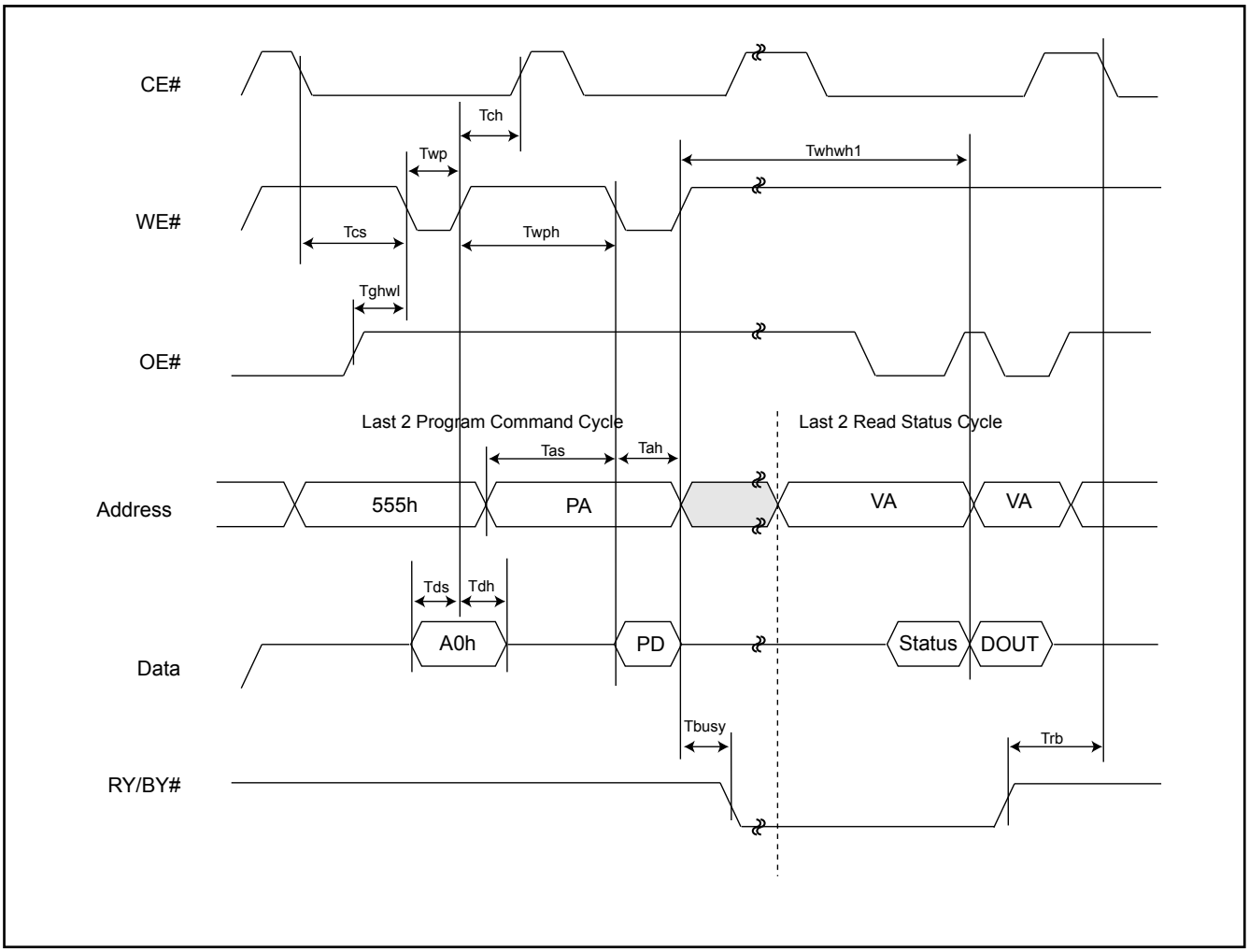


**Figure 10. CE# CONTROLLED WRITE TIMING WAVEFORM**

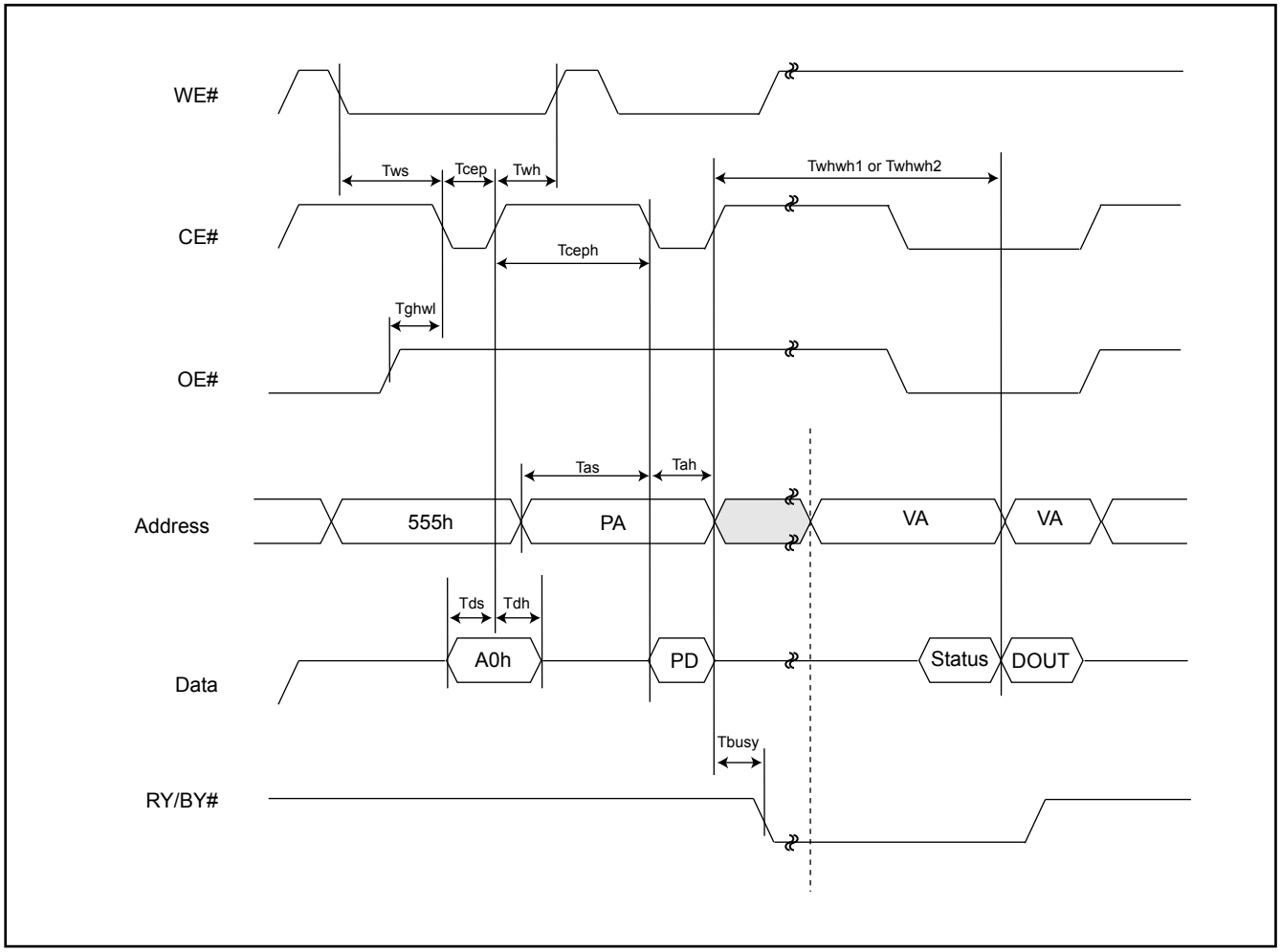
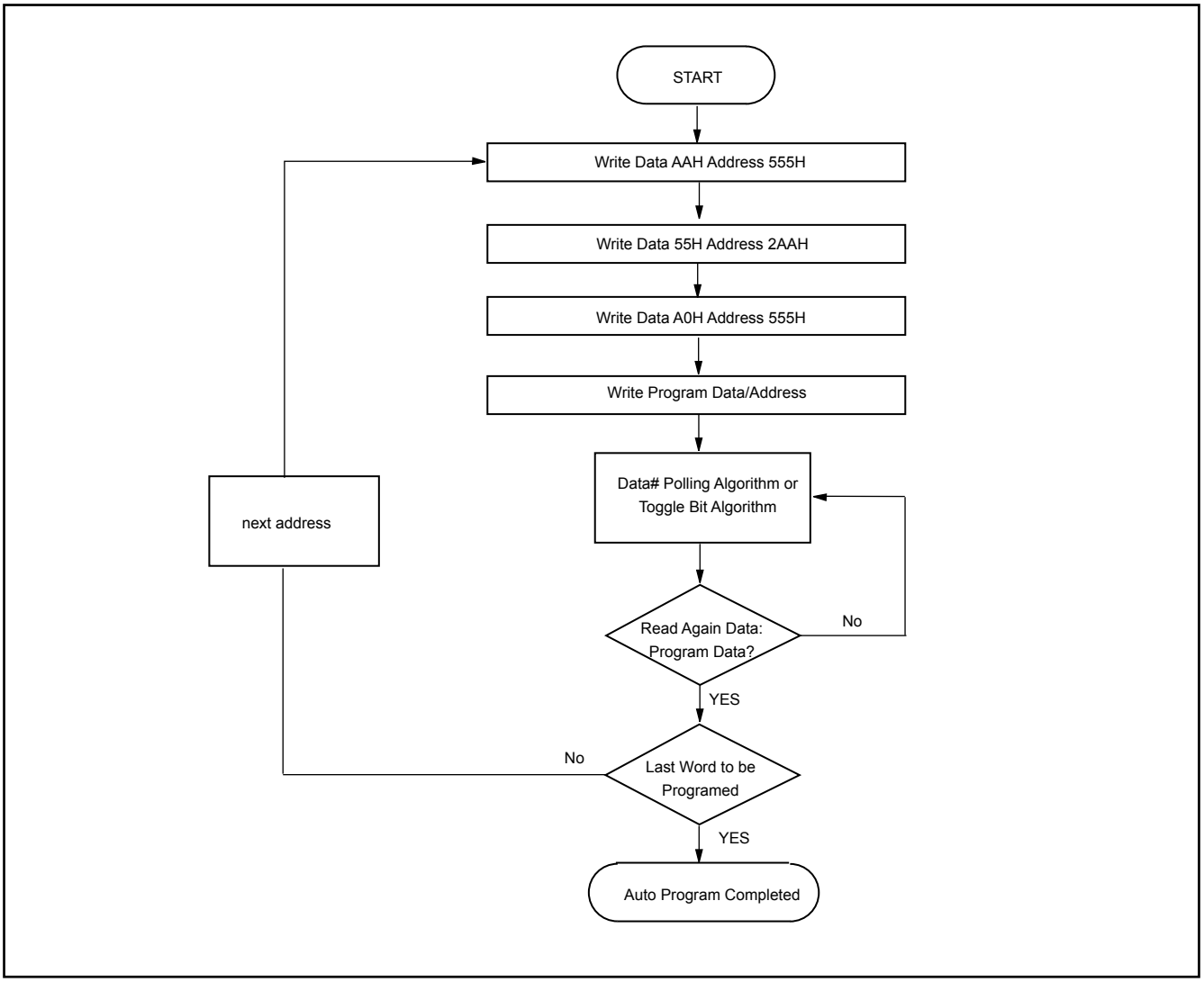


**Figure 11. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART**



## SECTOR PROTECT/CHIP UNPROTECT

**Figure 12. SECTOR PROTECT/CHIP UNPROTECT WAVEFORM (RESET# Control)**

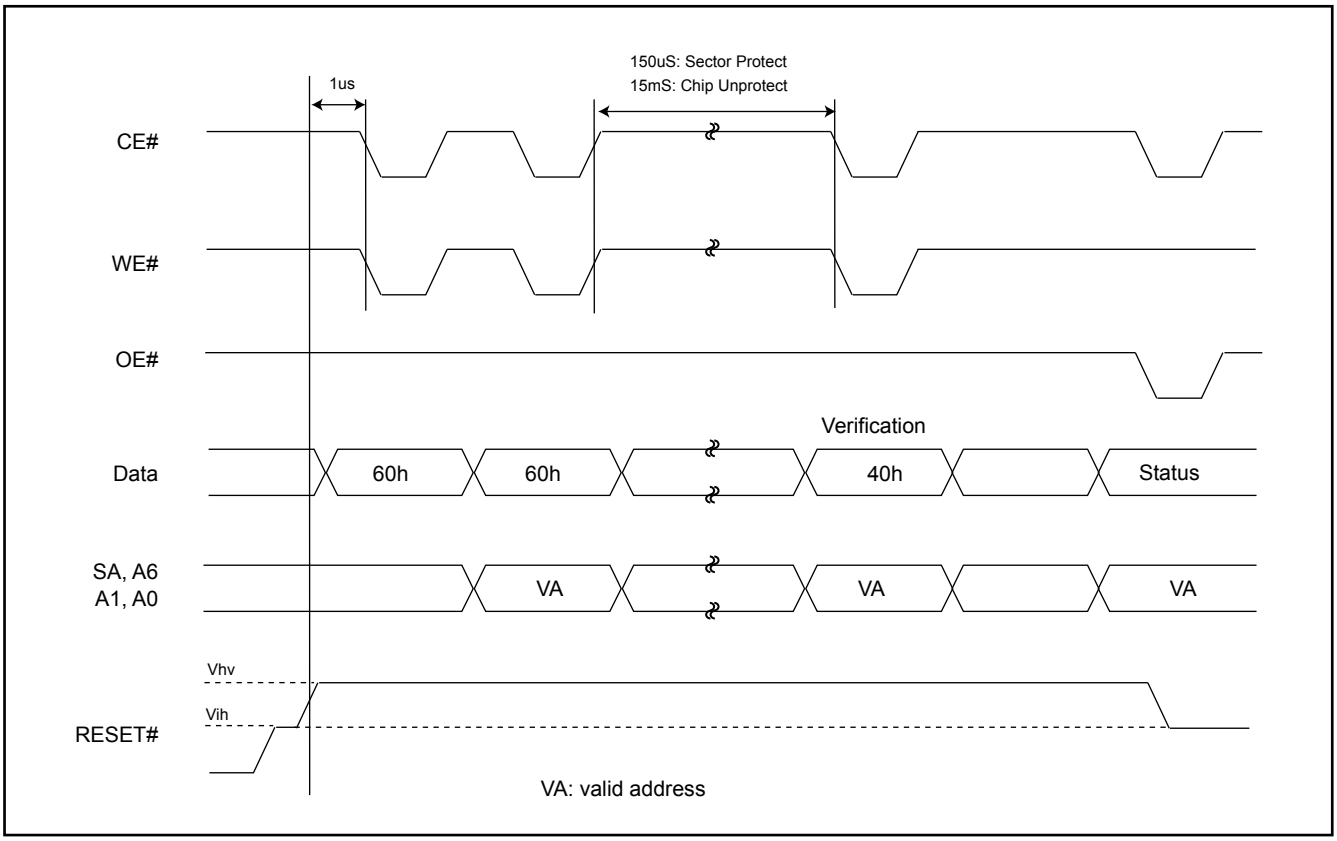


**Figure 13-1. IN-SYSTEM SECTOR PROTECT WITH RESET#=Vhv**

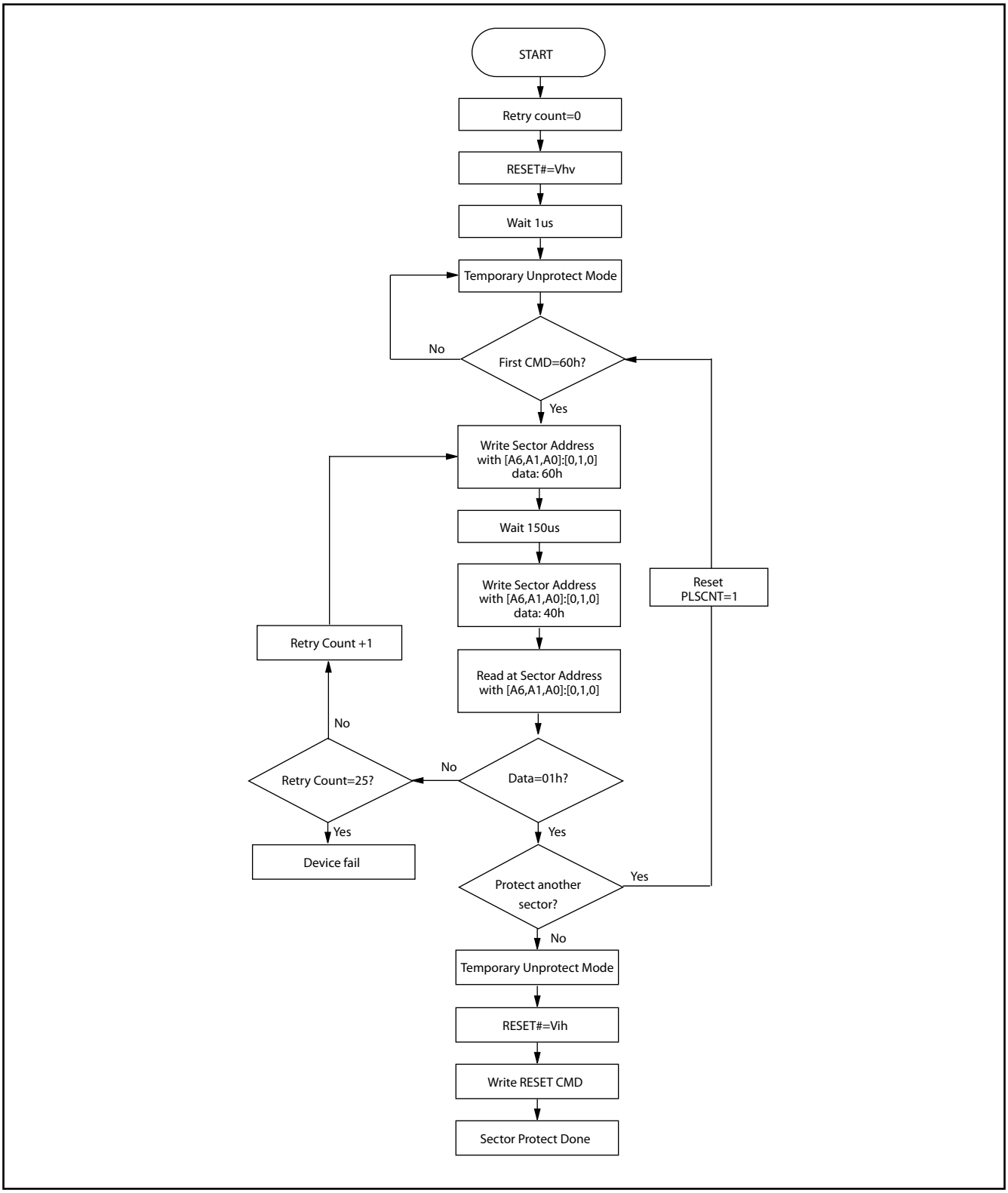


**Figure 13-2. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv**

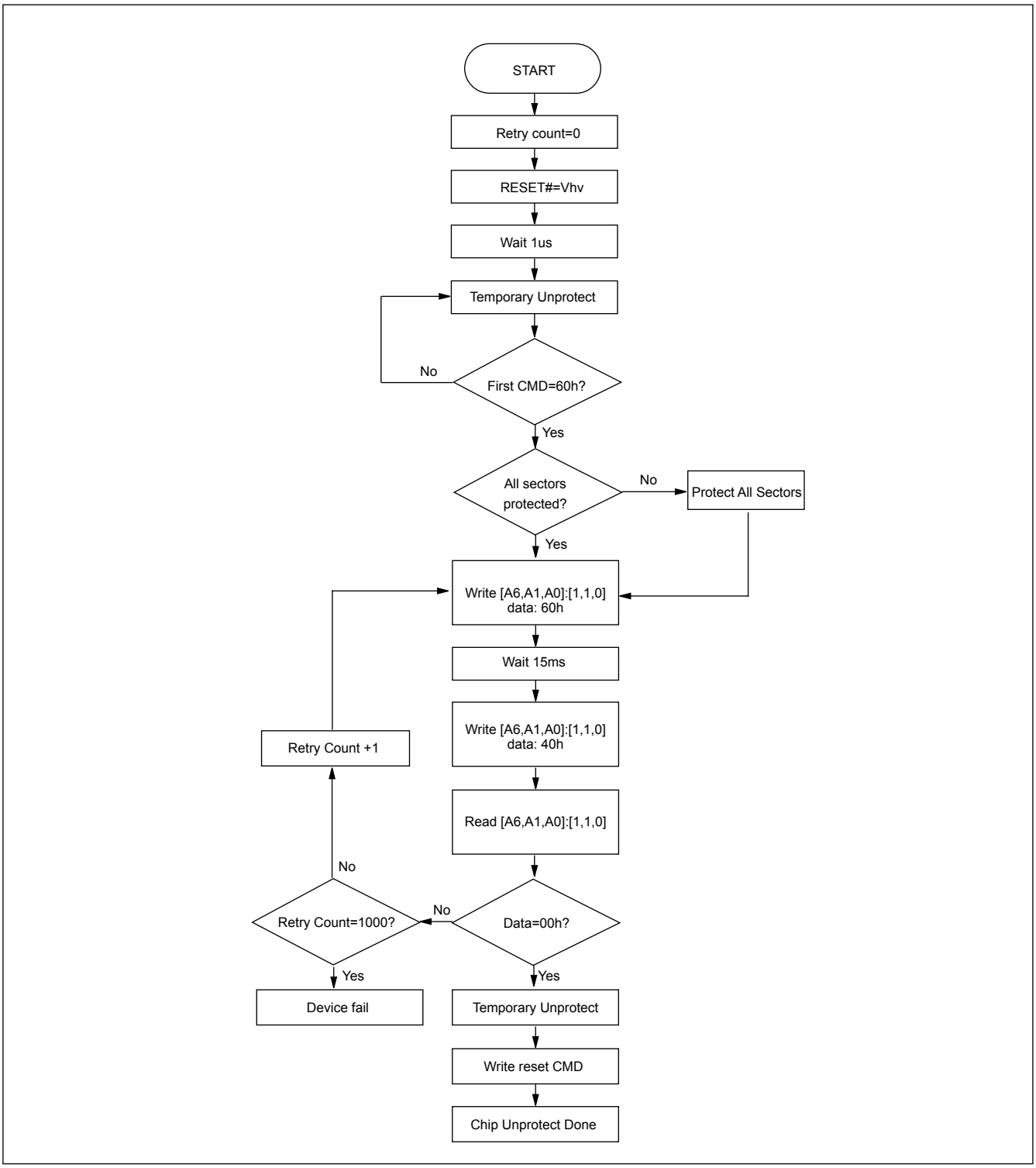


**Table 5. TEMPORARY SECTOR UNPROTECT**

| Parameter | Alt | Description | Condition | Speed | Unit |
|---|---|---|---|---|---|
| Trpvhh | Tvidr | RESET# Rise Time to Vhv and Vhv Fall Time to RESET# | MIN | 500 | ns |
| Tvhhwl | Trsp | RESET# Vhv to WE# Low | MIN | 4 | us |

**Figure 14. TEMPORARY SECTOR UNPROTECT WAVEFORMS**

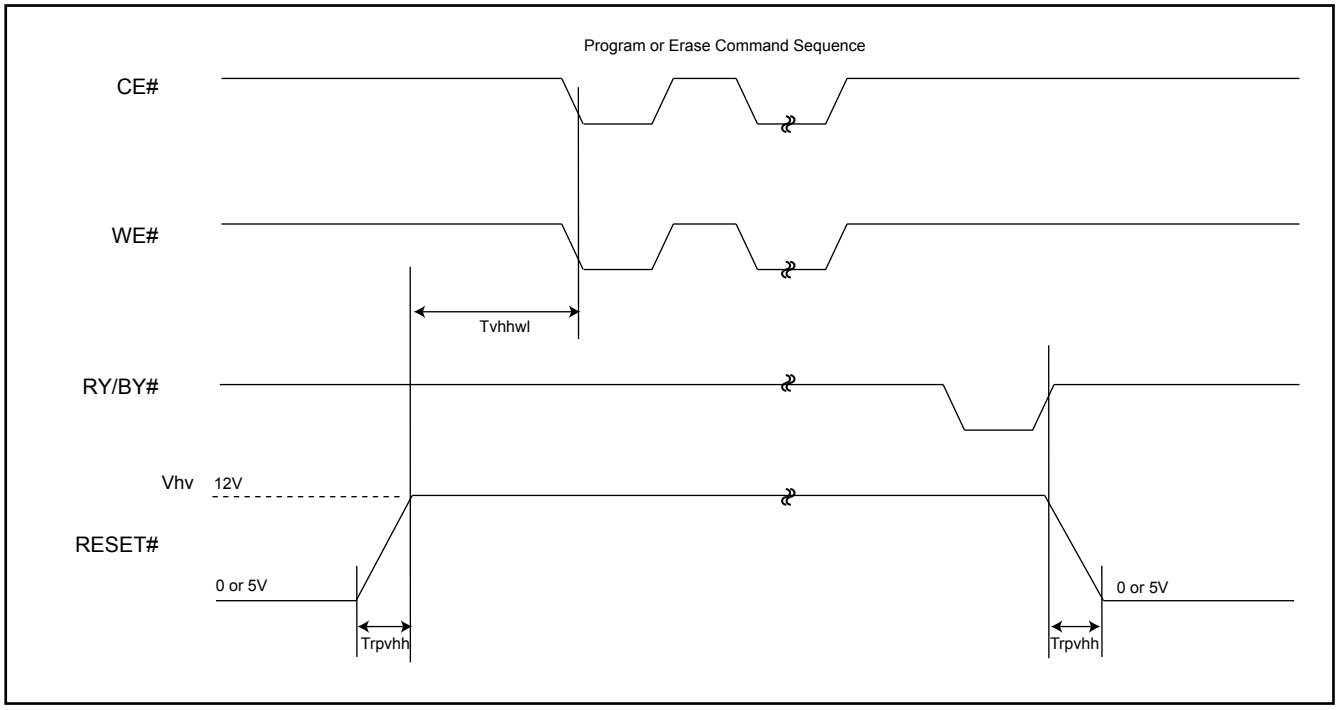
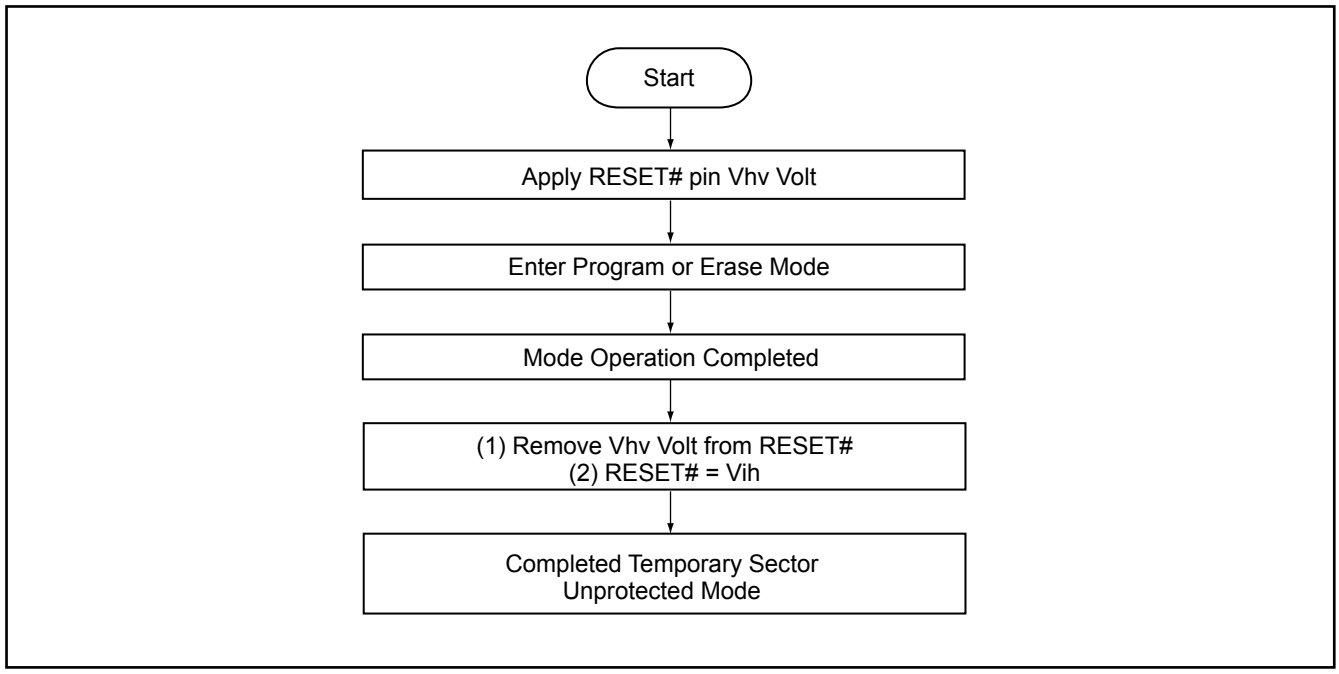
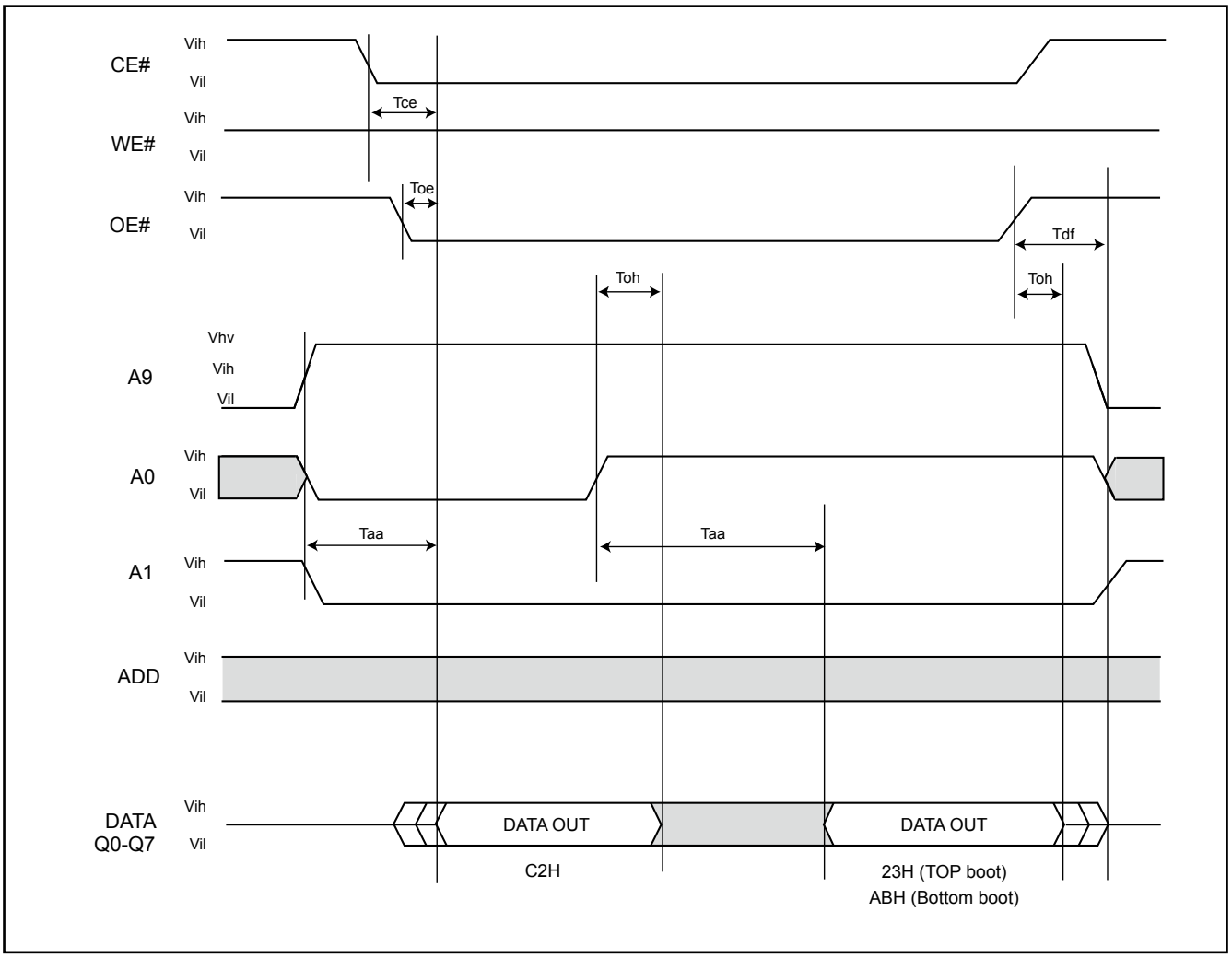


**Figure 15. TEMPORARY SECTOR UNPROTECT FLOWCHART**




Notes:
1. Temporary unprotect all protected sectors Vhv=11.5 ~ 12.5V.
2. The protected conditions of the protected sectors are the same to temporary sector unprotect mode.

**Figure 16. SILICON ID READ TIMING WAVEFORM**



## WRITE OPERATION STATUS

**Figure 17. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)**

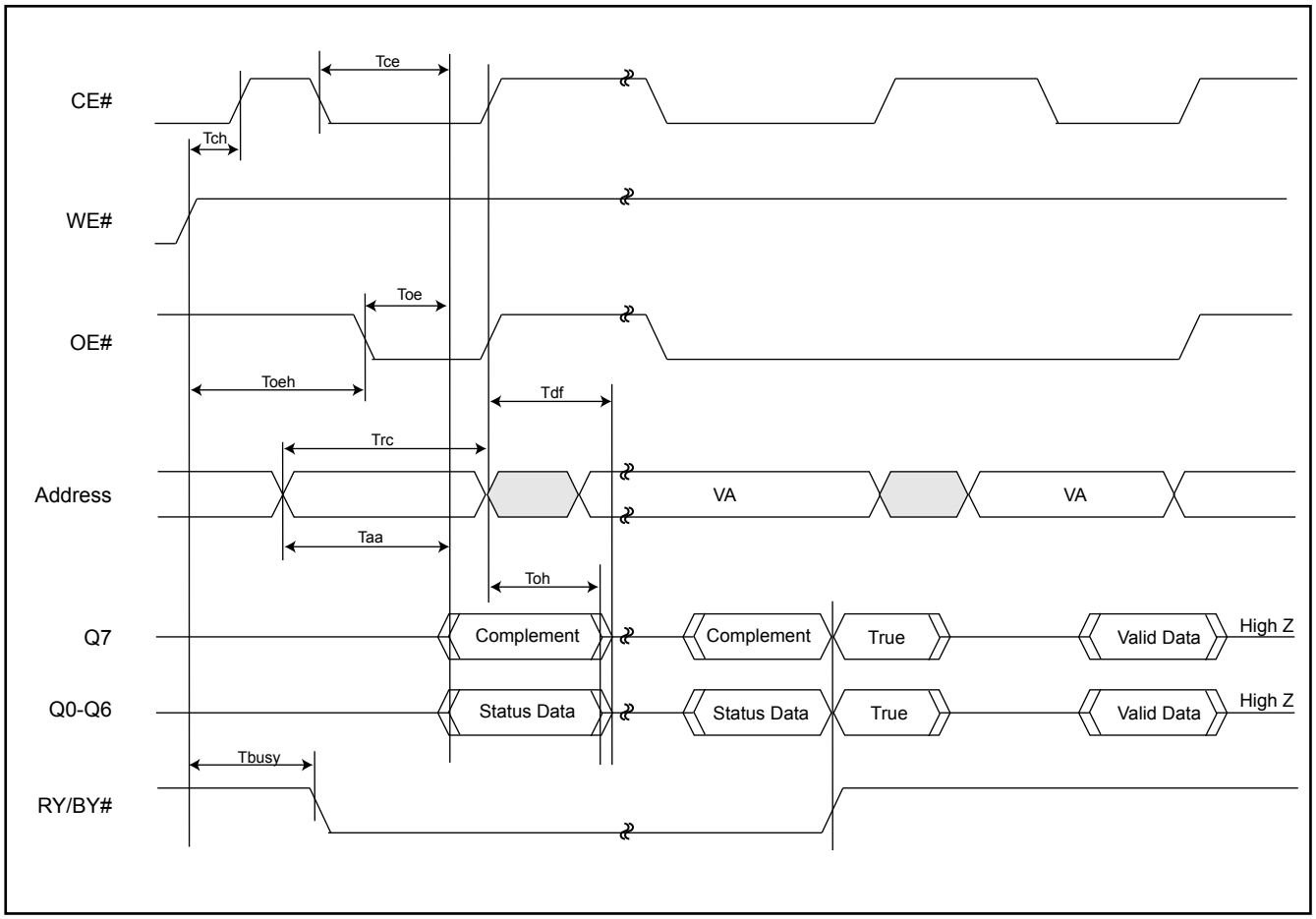
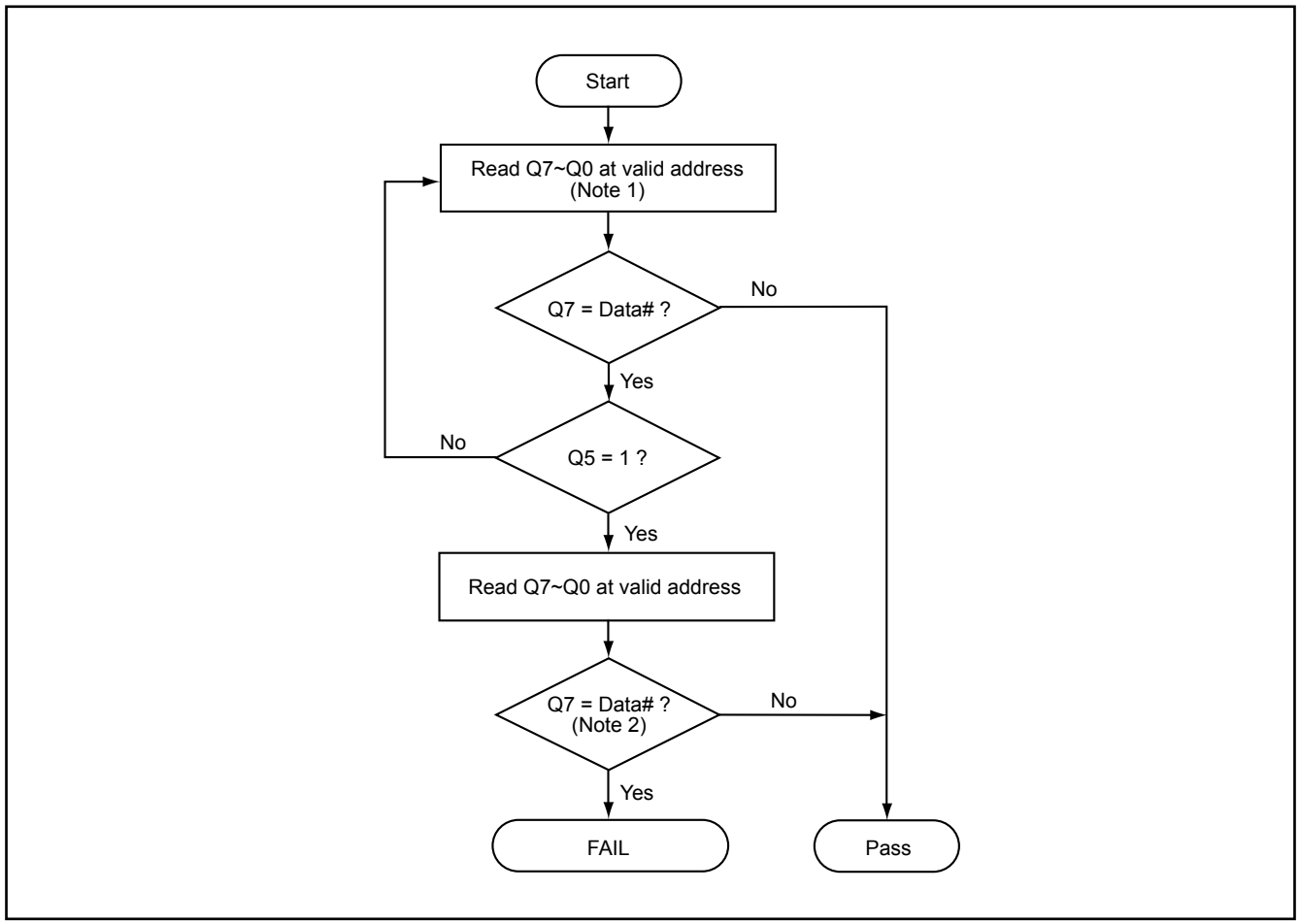


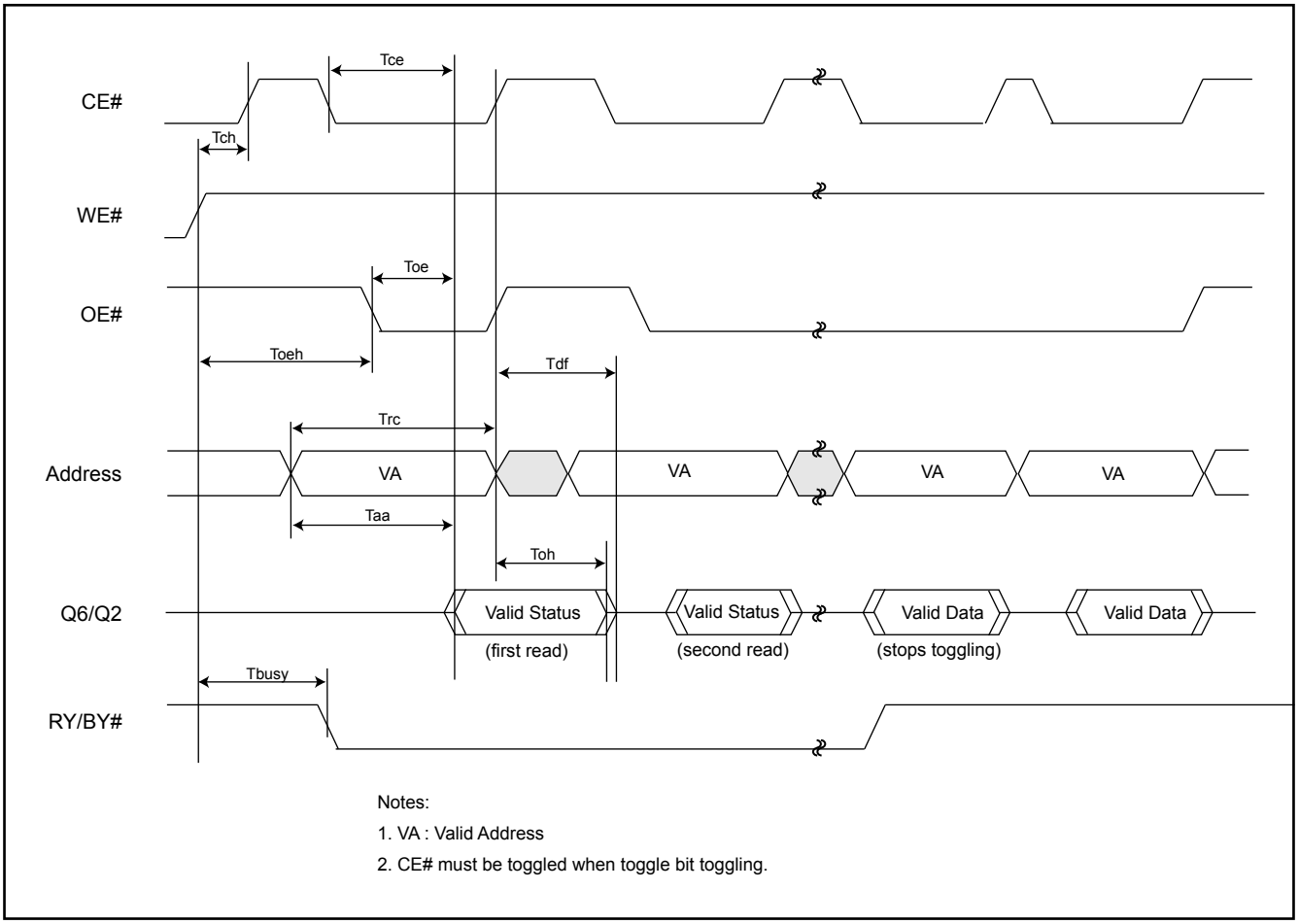
**Figure 18. DATA# POLLING ALGORITHM**




**Notes:**

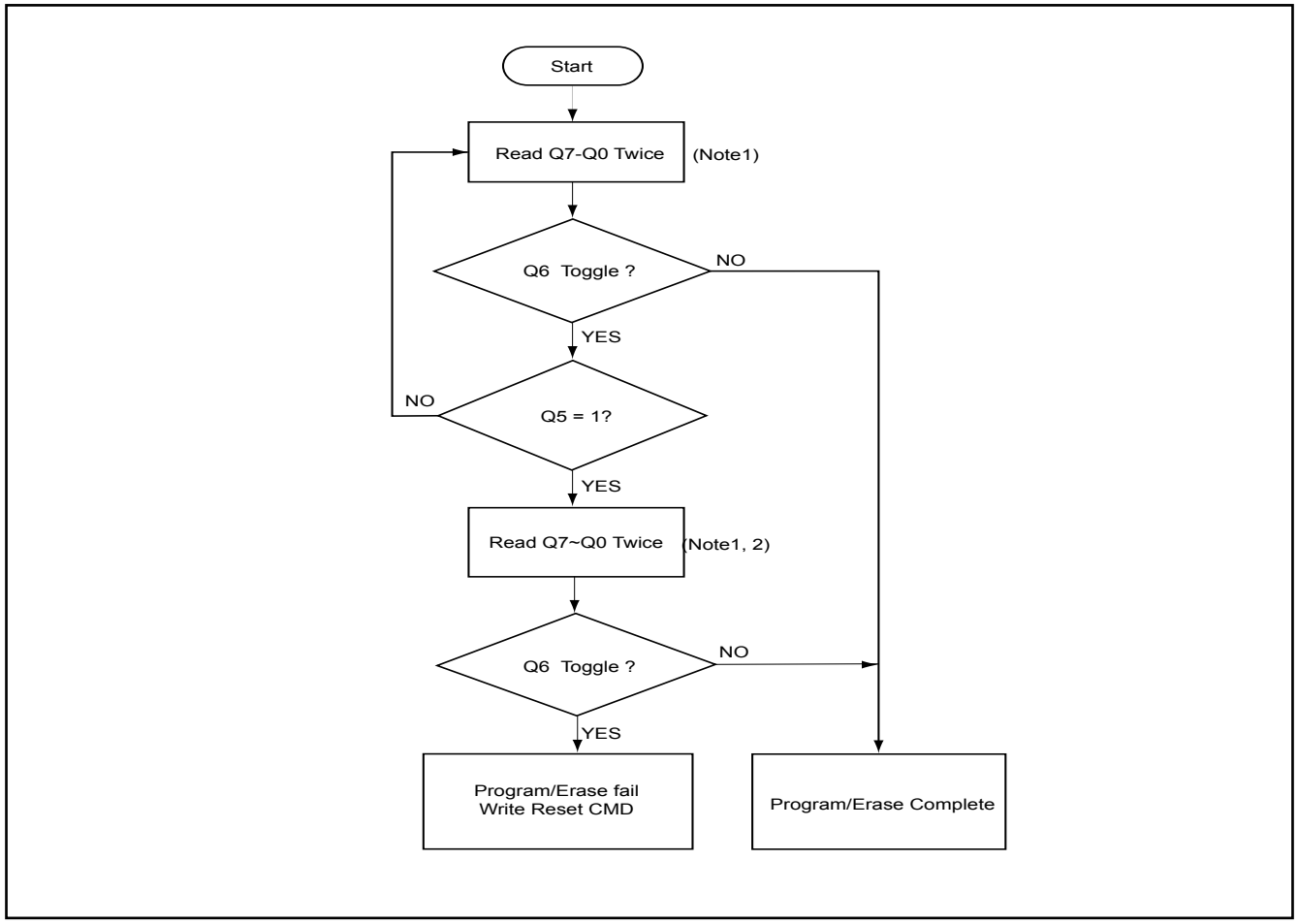
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

**Figure 19. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)**




Notes:
1. VA : Valid Address
2. CE# must be toggled when toggle bit toggling.

**Figure 20. TOGGLE BIT ALGORITHM**




Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

## RECOMMENDED OPERATING CONDITIONS

### At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

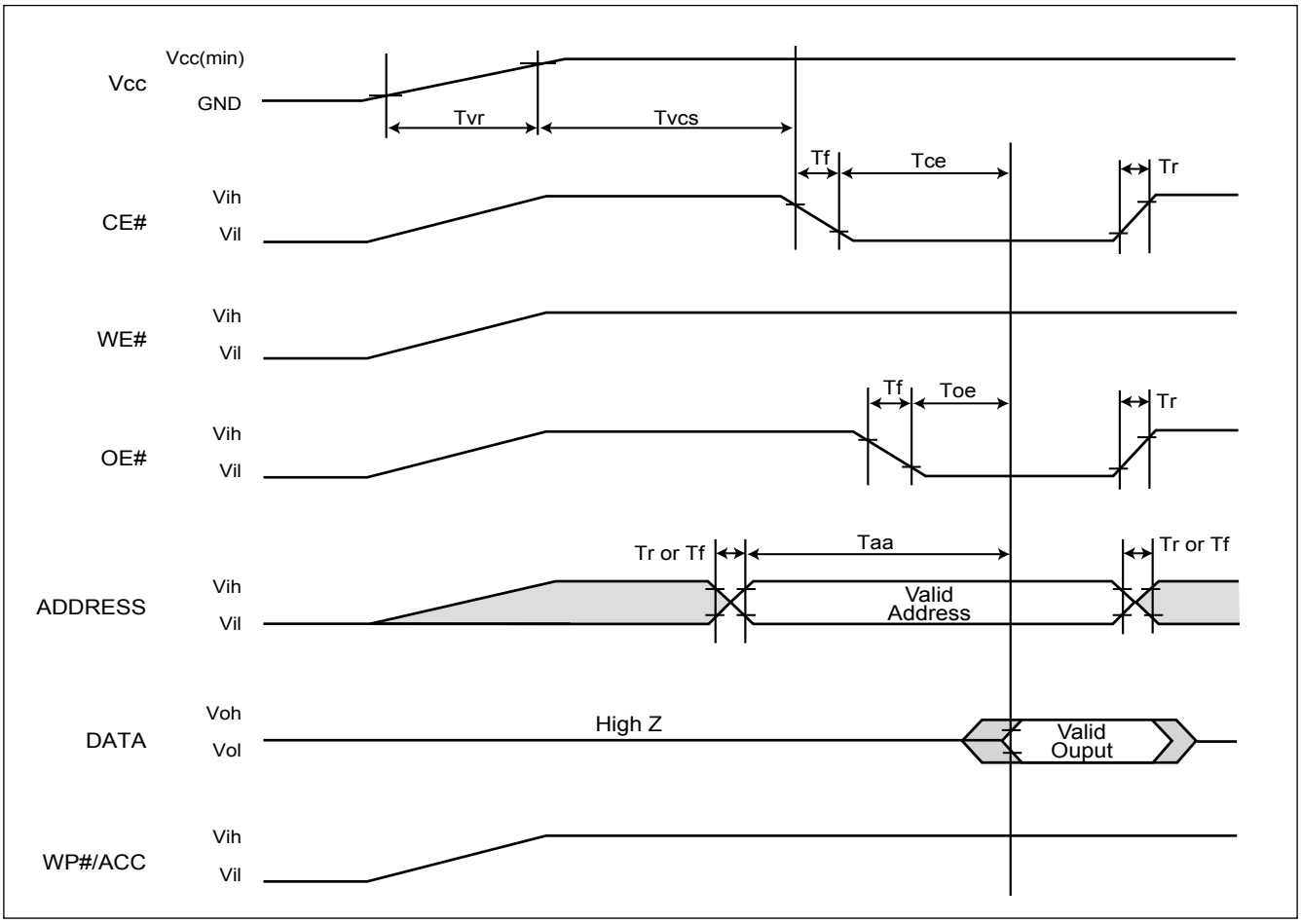



**Figure A. AC Timing at Device Power-Up**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| Tvr | Vcc Rise Time | 20 | 500000 | us/V |
| Tr | Input Signal Rise Time | | 20 | us/V |
| Tf | Input Signal Fall Time | | 20 | us/V |

## ERASE AND PROGRAMMING PERFORMANCE

| PARAMETER | | LIMITS | | | UNITS |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| Byte Programming Time | | | 9 | 300 | us |
| Word Programming Time | | | 11 | 360 | us |
| Sector Erase Time | | | 0.7 | 8 | sec |
| Chip Erase Time | | | 4 | 32 | sec |
| Chip Programming Time | Byte Mode | | 4.5 | 13.5 | sec |
| | Word Mode | | 3 | 9 | sec |
| Erase/Program Cycles | | 100,000 | | | Cycles |

Note: 1. Typical condition means 25°C, 5V.
2. Maximum condition means 90°C, 4.5V, 100K cycles.

## DATA RETENTION

| PARAMETER | Condition | Min. | Max. | UNIT |
|---|---|---|---|---|
| Data retention | 55˚C | 20 | | years |

## LATCH-UP CHARACTERISTICS

| | MIN. | MAX. |
|---|---|---|
| Input Voltage difference with GND on all pins except I/O pins | -1.0V | 13.5V |
| Input Voltage difference with GND on all I/O pins | -1.0V | Vcc + 1.0V |
| Vcc Current | -100mA | +100mA |
| Includes all pins except Vcc. Test conditions: VCC = 5V, one pin per testing | | |

## TSOP AND SOP PIN CAPACITANCE

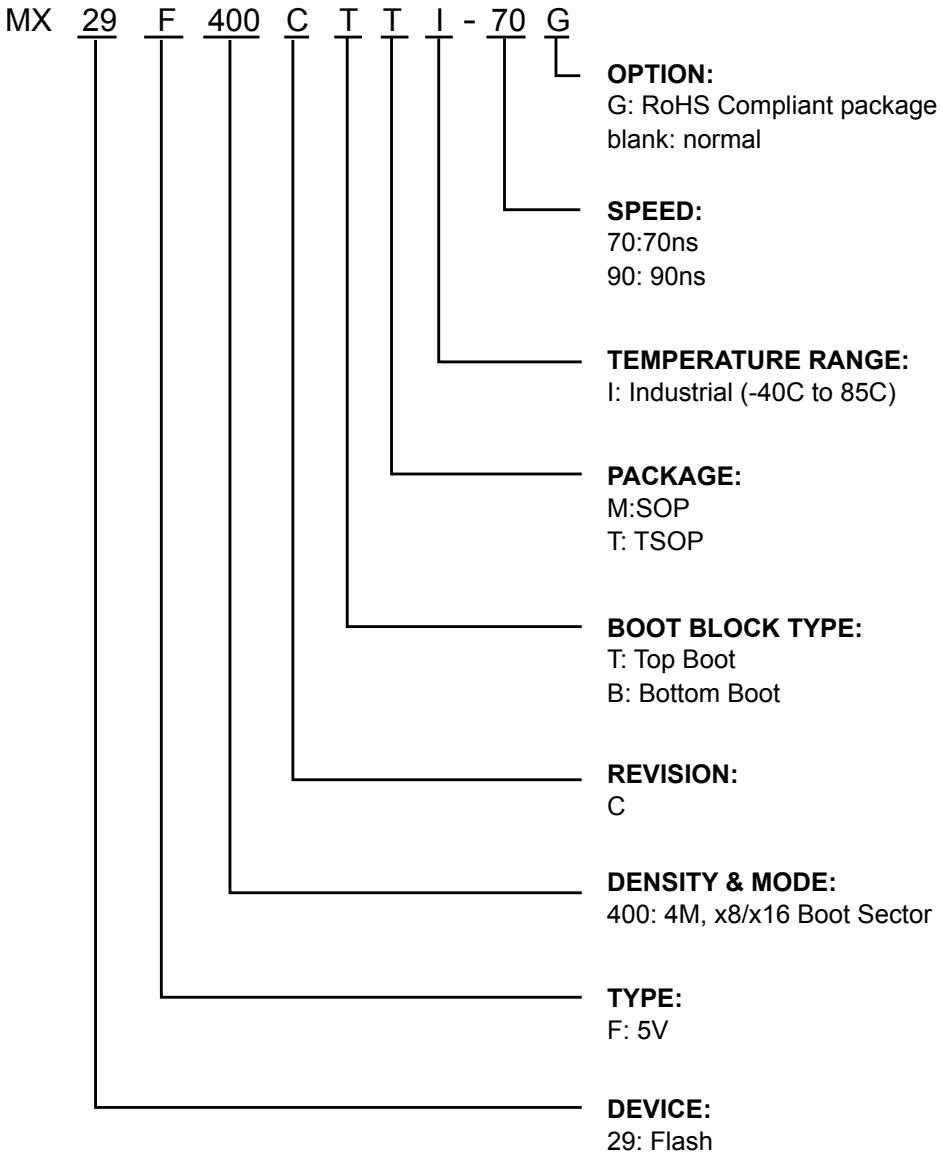
| Parameter Symbol | Parameter Description | Test Set | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| CIN2 | Control Pin Capacitance | VIN=0 | | 12 | pF |
| COUT | Output Capacitance | VOUT=0 | | 12 | pF |
| CIN | Input Capacitance | VIN=0 | | 8 | pF |

## ORDERING INFORMATION

| PART NO. | Access Time (ns) | Operating Current MAX.(mA) | Standby Current MAX.(uA) | Temperature Range | PACKAGE | Remark |
|---|---|---|---|---|---|---|
| MX29F400CTMI-70 | 70 | 40 | 5 | -40°C~85°C | 44 Pin SOP | Note 1 |
| MX29F400CTMI-90 | 90 | 40 | 5 | -40°C~85°C | 44 Pin SOP | Note 1 |
| MX29F400CTTI-70 | 70 | 40 | 5 | -40°C~85°C | 48 Pin TSOP (Normal Type) | Note 1 |
| MX29F400CTTI-90 | 90 | 40 | 5 | -40°C~85°C | 48 Pin TSOP (Normal Type) | Note 1 |
| MX29F400CBMI-70 | 70 | 40 | 5 | -40°C~85°C | 44 Pin SOP | Note 1 |
| MX29F400CBMI-90 | 90 | 40 | 5 | -40°C~85°C | 44 Pin SOP | Note 1 |
| MX29F400CBTI-70 | 70 | 40 | 5 | -40°C~85°C | 48 Pin TSOP (Normal Type) | Note 1 |
| MX29F400CBTI-90 | 90 | 40 | 5 | -40°C~85°C | 48 Pin TSOP (Normal Type) | Note 1 |
| MX29F400CTMI-70G | 70 | 40 | 5 | -40°C~85°C | 44 Pin SOP | RoHS Compliant |
| MX29F400CTMI-90G | 90 | 40 | 5 | -40°C~85°C | 44 Pin SOP | RoHS Compliant |
| MX29F400CTTI-70G | 70 | 40 | 5 | -40°C~85°C | 48 Pin TSOP (Normal Type) | RoHS Compliant |
| MX29F400CTTI-90G | 90 | 40 | 5 | -40°C~85°C | 48 Pin TSOP (Normal Type) | RoHS Compliant |
| MX29F400CBMI-70G | 70 | 40 | 5 | -40°C~85°C | 44 Pin SOP | RoHS Compliant |
| MX29F400CBMI-90G | 90 | 40 | 5 | -40°C~85°C | 44 Pin SOP | RoHS Compliant |
| MX29F400CBTI-70G | 70 | 40 | 5 | -40°C~85°C | 48 Pin TSOP (Normal Type) | RoHS Compliant |
| MX29F400CBTI-90G | 90 | 40 | 5 | -40°C~85°C | 48 Pin TSOP (Normal Type) | RoHS Compliant |

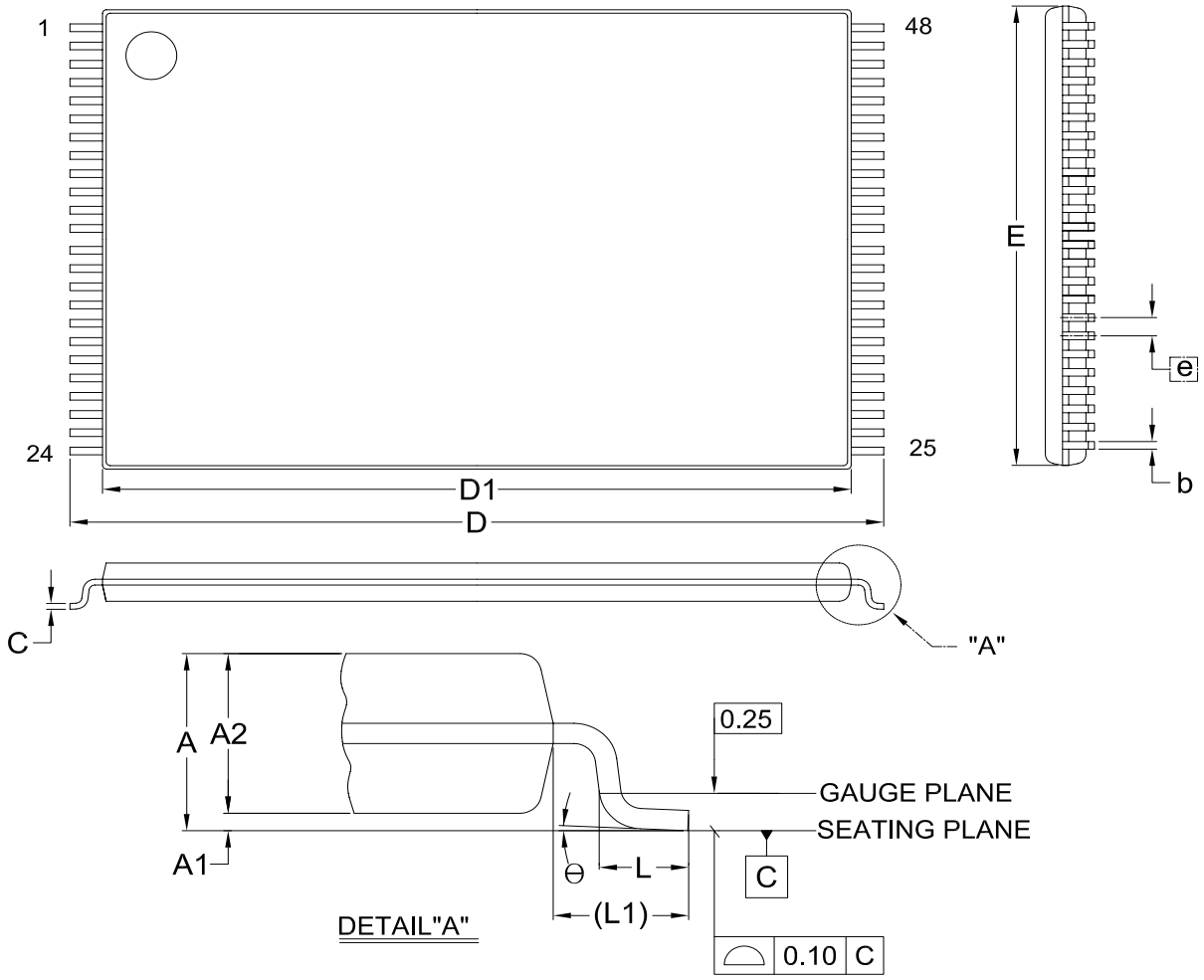
Note 1: The part no. is not recommended for new design in.

## PART NAME DESCRIPTION



## PACKAGE INFORMATION

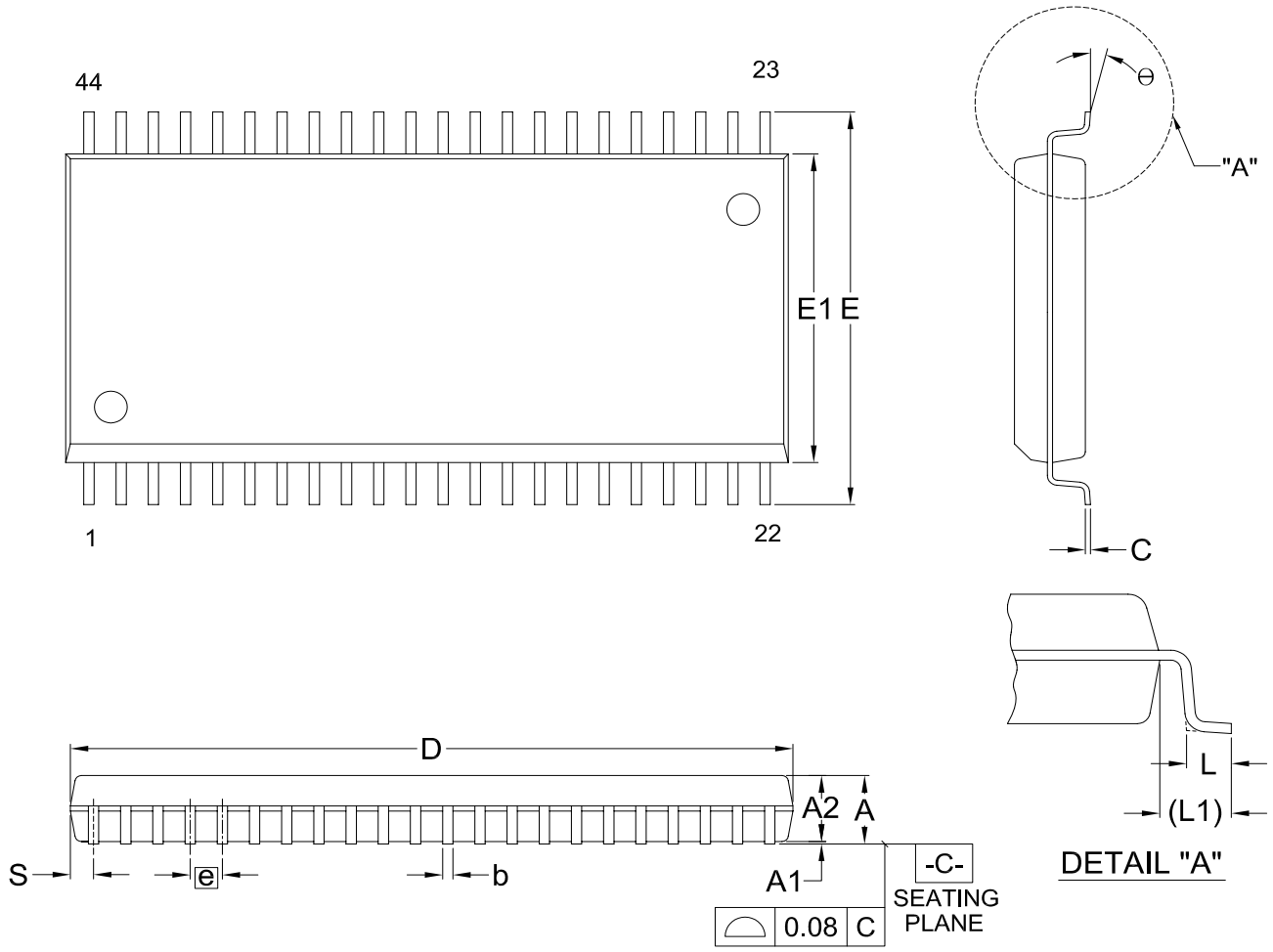
Doc. Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | D1 | E | e | L | L1 | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | — | 0.05 | 0.95 | 0.17 | 0.10 | 19.80 | 18.30 | 11.90 | — | 0.50 | 0.70 | 0° |
| | Nom. | — | 0.10 | 1.00 | 0.20 | 0.13 | 20.00 | 18.40 | 12.00 | 0.50 | 0.60 | 0.80 | 5° |
| | Max. | 1.20 | 0.15 | 1.05 | 0.27 | 0.21 | 20.20 | 18.50 | 12.10 | — | 0.70 | 0.90 | 8° |
| Inch | Min. | — | 0.002 | 0.037 | 0.007 | 0.004 | 0.780 | 0.720 | 0.469 | — | 0.020 | 0.028 | 0° |
| | Nom. | — | 0.004 | 0.039 | 0.008 | 0.005 | 0.787 | 0.724 | 0.472 | 0.020 | 0.024 | 0.031 | 5° |
| | Max. | 0.047 | 0.006 | 0.041 | 0.011 | 0.008 | 0.795 | 0.728 | 0.476 | — | 0.028 | 0.035 | 8° |

Doc. Title: Package Outline for SOP 44L (500MIL)




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.10 | 2.59 | 0.36 | 0.15 | 28.37 | 15.83 | 12.47 | --- | 0.56 | 1.51 | 0.78 | 0° |
| | Nom. | --- | 0.15 | 2.69 | 0.41 | 0.20 | 28.50 | 16.03 | 12.60 | 1.27 | 0.76 | 1.71 | 0.91 | 5° |
| | Max. | 3.00 | 0.20 | 2.80 | 0.51 | 0.25 | 28.63 | 16.23 | 12.73 | --- | 0.96 | 1.91 | 1.04 | 10° |
| Inch | Min. | --- | 0.004 | 0.102 | 0.014 | 0.006 | 1.117 | 0.623 | 0.491 | --- | 0.022 | 0.059 | 0.031 | 0° |
| | Nom. | --- | 0.006 | 0.106 | 0.016 | 0.008 | 1.122 | 0.631 | 0.496 | 0.050 | 0.030 | 0.067 | 0.036 | 5° |
| | Max. | 0.118 | 0.008 | 0.110 | 0.020 | 0.010 | 1.127 | 0.639 | 0.501 | --- | 0.038 | 0.075 | 0.041 | 10° |

## REVISION HISTORY

| Revision No. | Description | Page | Date |
|---|---|---|---|
| 1.0 | 1. Removed "Preliminary" title | P1 | DEC/20/2005 |
| | 2. Removed commercial grade | All | |
| | 3. Added access time: 55ns; Removed access time: 120ns | All | |
| 1.1 | 1. Removed access time : 55ns | P1,19,21,22 P38,39 | JUN/20/2006 |
| | 2. Removed sector protect/ chip unprotect without 12V | P1,7,17,31~34 | |
| | 3. Added in-system sector protect/ chip unprotect | P33~35 | |
| | 4. Added data# polling, toggle bit algorithm | P26,27 | |
| | 5. Added RY/BY# timing waveform | P24,28,30 | |
| 1.2 | 1. Datasheet format changed | All | AUG/15/2006 |
| 1.3 | 1. Data modification | All | AUG/17/2006 |
| | 2. Changed maximum condition as 90°C, 4.5V 100K cycles | P41 | |
| 1.4 | 1. Added statement | P47 | NOV/06/2006 |
| 1.5 | 1. Data modification | P2 | DEC/11/2006 |
| 1.6 | 1. Added recommendation for non RoHS compliant devices | P1,42 | MAR/19/2007 |
| | 2. Changed test condition : 30PF loading for 70ns | P17 | |
| 1.7 | 1. Added note 4 into table 3. Command Definitions | P10 | JAN/22/2008 |
| 1.8 | 1. Modified Figure 10. CE# Controlled Write Timing Waveform | P28 | FEB/25/2008 |
| 1.9 | 1. Modified Figure 10. CE# Controlled Write Timing Waveform (Changed "Twhwh1 or Twhwh2" into "Tavt or Taetb") | P28 | MAR/09/2009 |
| | 2. Modified Figure 12. DATA# POLLING TIMING WAVEFORM | P36 | |
| 2.0 | 1. Added Note into DC characteristics | P15 | MAY/25/2009 |
| | 2. Added Icw/Trc/Twp/Twph/Tghwl spec | P16, 18 | |
| | 3. Added Note for voltage undershooting | P15 | |
| | 4. Revised Figure 14. TEMPORARY UNPROTECT WAVEFORMS | P33 | |
| 2.1 | 1. Added data retention table | P41 | JUN/30/2009 |
| | 2. Modified the sector erase time max from 15s to 8s | P18,41 | |
| 2.2 | 1. Modified AC CHARACTERISTICS | P18 | NOV/29/2010 |
| | 2. Modified description wording for "RoHS Compliant" | P1,42,43 | |
| 2.3 | 1. Added Tws & Twh values | P18,28 | DEC/14/2017 |
| | 2. Content and format modifications for package outline | P44,45 | |

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