Stereo Class D Amplifier with Integrated Boost Controller For 2-cell 20W or 3-cell 30W Battery Application

General Description

The VA9201 is a multi-function, high-power Class D stereo audio power amplifier featured with integrated of one current-mode boost controller. VA9201 is capable of delivering continuous 20W stereo output at 18V boosted supply and 30W/8Ω output at 22.5V boosted supply per channel within 10% distortion. With the filter-less output filter design and fully differential input, VA9201 is ideal to provide excellent sound quality with good RF noise immunity on portable electronics devices.

VA9201 integrates a current-mode boost controller with fast response and high efficiency. With 6V to 13.2V input voltage, it could boost the lower input voltage such as single cell Li-ion battery output to higher and then makes the audio amplifier operates at higher voltage to reduce the distortion.

The VA9201 is available in TQFP-48 green package with exposed pad.

Features

Stereo Class D Amplifier

- Operating Voltage from 6V to 22.5V
- 8Ω Speaker:
  - 20W@17.5V with 7% THD+N (heat-sink)
  - 30W@22.5V with 2% THD+N (heat-sink)
- Fully Differential Input
- Programmable Gain by External Resistors
- Excellent EMI Performance
- Fixed 400kHz Operation
- BD/1SPW Mode Operation
- Short Circuit and Thermal protection

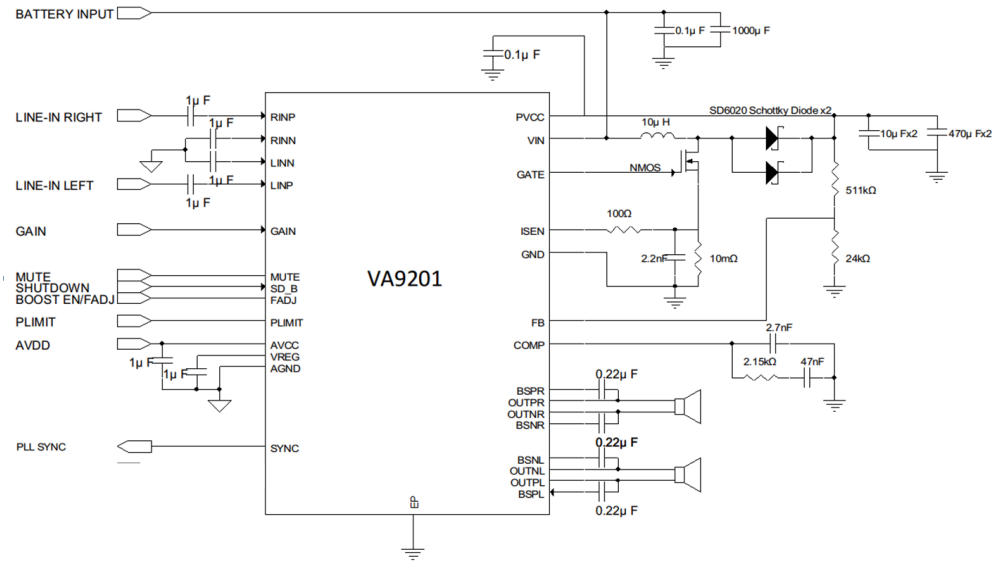
Boost Controller

- Recommended Input and Output Configuration:
  a. 6V~13.2V Input for 18V Audio PVDD
  b.9V~13.2V Input for 22.5V Audio PVDD

Package

- RoHS 2.0 compliant TQFP-48 Green Package with Exposed Pad

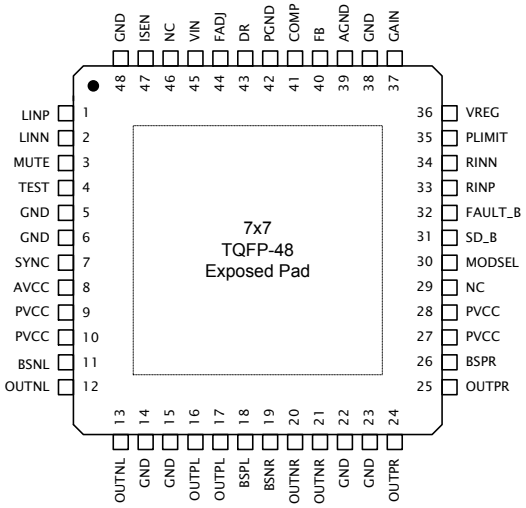
Typical Application



Applications

- Battery Powered Portable Speakers

Pin Assignments And Descriptions



Pin No.	Pin	I/O/P	Function Description
1	LINP	I	Left channel positive audio signal input.
2	LINN	I	Left channel negative audio signal input.
3	MUTE	I	Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). Low voltage level compliance to VREG.
4	TEST	-	Test Pin. No use. Left it floating.
5	GND	I	Ground. Connect this pin to ground.
6	GND	I	Ground. Connect this pin to ground.
7	SYNC	I	Clock Synchronization. I/O pin for synchronizing multiple Class D amplifiers.
8	AVCC	P	Class D Analog power supply. Connect to boosted voltage output.
9	PVCC	P	Class D Power Stage supply. Connect to boosted voltage output.
10	PVCC	P	Class D Power Stage supply. Connect to boosted voltage output.
11	BSNL	-	Bootstrap I/O for left channel negative high-side switch.
12	OUTNL	O	Left channel negative output.
13	OUTNL	O	Left channel negative output.
14	GND	P	Class D Driver stage power ground.
15	GND	P	Class D Driver stage power ground.
16	OUTPL	O	Left channel positive output
17	OUTPL	O	Left channel positive output.
18	BSPL	-	Bootstrap I/O for left channel positive high-side switch.
19	BSNR	-	Bootstrap I/O for right channel negative high-side switch.
20	OUTNR	O	Right channel negative output.
21	OUTNR	O	Right channel negative output.
22	GND	P	Class D Driver stage power ground.
23	GND	P	Class D Driver stage power ground.
24	OUTPR	O	Right channel positive output
25	OUTPR	O	Right channel positive output.
26	BSPR	-	Bootstrap I/O for right channel positive high-side switch.
27	PVCC	P	Class D Power Stage supply. Connect to boosted voltage output.
28	PVCC	P	Class D Power Stage supply. Connect to boosted voltage output.

Pin Assignments And Descriptions

Pin No.	Pin	I/O/P	Function Description
29	NC	-	No internal connection.
30	MODSEL	I	Mode selection. Low for BD mode, HIGH for 1SPW mode. TTL Logic levels with compliance to PVCC. this pin is pulled down.
31	SD_B	I	Amplifier shutdown control terminal. Low active. TTL Logic levels with compliance to AVCC.
32	FAULT_B	I	Amplifier shutdown control terminal. Low active. TTL Logic levels with compliance to AVCC.
33	RINP	I	Right channel positive audio signal input.
34	RINN	I	Right channel negative audio signal input.
35	PLIMIT	I	Power Limit Level Adjust. Connect a resistor divider from VREG to AGND to set power limit. Connect to VREG directly for no power limit.
36	VREG	O	Internal Regulated Voltage Output. Need to connect a 1μF capacitor to ground to achieve good gate driver performance.
37	GAIN	I	Gain selection. Use recommended voltage divider network to specify proper gain.
38	GND	P	Class D Driver stage power ground.
39	AGND	P	Analog Power Ground.
40	FB	I	Output Feedback. Connect the external resistor divider network from output to this pin to sense output voltage. The FB pin voltage is regulated to internal 1.26V reference voltage.
41	COMP	-	Compensation. Use a RC/C network to do proper loop compensation.
42	PGND	P	Boost Gate Driver Power Ground.
43	GATE	O	Power Stage Drive Pin. The gate of the external MOSFET should be connected to this pin.
44	FADJ	I	Boost Frequency Adjust/Synchronization/Shutdown. A resistor connected from this pin to ground simply sets the oscillator frequency. An external clock signal at this pin will synchronize the controller to the clock. Pull on this pin for ≥ 30 μs will turn the device off and the boost controller will then very few current about 10μA from the supply.
45	VIN	P	Power Supply Input. Boost controller is powered through this pin. Add a 0.1μF bypass capacitor is recommended.
46	NC	-	No internal connection.
47	ISEN	P	Current Sense. Use an external resistor in series with ground to measure the voltage drop.
48	GND	P	Boost Driver Power Ground.

Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (* 1)

Symbol	Parameter	Limit	Unit
V_{IN}(VIN)	Boost controller supply voltage	-0.3 to 30	V
V_{CC}(PVCC, AVCC)	Amplifier supply voltage	-0.3 to 30	V
V_{IN} (COMP, FADJ, FB, GAIN, LINN, LINP, PLIMIT, RINN, RINP, SYNC)	Low voltage input range	0 to 6	V
$V_{IN(HIGH)}$(MODESEL, MUTE, SD_B)	High voltage input range	0 to VDD+0.3	V
V_{ISEN}	Current Sense Input	-0.4 to 0.6	V
T_A	Operating free-air temperature range	-40 ~ +85	ºC
T_J	Operating junction temperature range	-40 to +150	ºC
T_{STG}	Storage temperature range	-65 to 150	ºC
$R_{(LOAD)}$	Amplifier minimum load resistance	8	Ω
Electrostatic discharge	Human body model	±2	kV
Electrostatic discharge	Machine model	±200	V

(*1): Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise specified.

Symbol	Parameter	Test Condition	Specification		Unit
			Min	Max	
V_{IN}	Boost Controller Supply Voltage	PV_{DD}=18V	6	13.2	V
V_{IN}	Boost Controller Supply Voltage	PV_{DD}=22.5V	9	13.2	V
V_{CC}	Amplifier Supply Voltage		6	22.5	V
$V_{IH(HIGH)}$	High level input voltage (high voltage)	PV_{DD}=6V	2.0	AV_{DD}	V
$V_{IH(LOW)}$	High level input voltage (low voltage)	PV_{DD}=6V	2.0	5	V
V_{IL}	Low Level Input Voltage	PV_{DD}=6V	-	0.4	V

Electrical Characteristics

T_A = 25℃, V_{IN} = 12V, Vcc(A_{VCC}/P_{VCC}) = 22.5V, R_L=8Ω, GAIN=26dB, unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ.	Max	
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I=0V			1.5	15	mV
I_Q	Quiescent current	SD_B=2V, No load			25	40	mA
I_{SD}	Shutdown current	SD_B=0.8V, No load			250	500	μA
t_{ON}	Shutdown turn-on time	SD_B=2V			15		ms
t_{OFF}	Shutdown turn-off time	SD_B=0.8V			2		μs
f_{OSC}	Internal oscillation frequency				400		kHz
A	Amplifier gain	R_{DOWN}=5.6kΩ, R_{UP}=Open			20		dB
		R_{DOWN}=27kΩ, R_{UP}=100kΩ			26		
		R_{DOWN}=39kΩ, R_{UP}=100kΩ			32		
		R_{DOWN}=47kΩ, R_{UP}=75kΩ			36		
$R_{DS(ON)}$	Drain-Source ON resistance[1]	V_{CC}=12V, I_{OUT}=500mA	High Side		100		mΩ
			Low Side		100		
V_{REG}	Regulator output	I_{VREG} = 100μA, V_{DD}=6~22.5V		5.55	5.75	6.05	V
t_{DC-DET}	DC detect time				420		ms
t_{TRIP}	Over-temperature threshold				170		℃
$t_{HYSTERSIS}$	OTP hysteresis				20		℃
I_{OCP}	Over-current trap threshold				8		A

(1) Design center value.

Operating Characteristics

T_A = 25℃, V_{IN} = 12V, Vcc(A_{VCC}/P_{VCC}) = 22.5V, R_L=8Ω, GAIN=26dB, unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ.	Max	
P_O	Output power	V_{IN} = 8V, V_{CC} = 17.5V , f=1kHz, R_L=8Ω *	THD+N=7%		20		W
		V_{IN} = 12V, V_{CC} = 22.5V , f=1kHz, R_L=8Ω *	THD+N=2%		30		
THD+N	Total harmonic distortion plus noise	V_{CC}=17.5V, P_O=10W, R_L=8Ω, f=1kHz			<0.15		%
$\|V_{OS}\|$	Offset voltage				20		mV
$\|K_{SVR}\|$	Supply ripple rejection ration	Input AC-Grounded, C_i=1μF, f=1kHz			70		dB
|SNR|	Signal-to-Noise ratio	A-weighted, THD+N=1%, R_L=8Ω			97		dB
V_n	Output voltage noise	C_i=1μF, A=26dB, f=20Hz to 20kHz, A-weighted, Input AC-Grounded			80		μV_{RMS}
|CMRR|	Common mode rejection ratio	V_{CC}=12V, V_{IC}=1V_{PP}	f=120Hz		68		dB
Z_I	Input impedance	Gain=20dB			60		kΩ
Crosstalk	Channel separation	V_O=1W, f=1kHz, Gain=20dB			99		dB

(*) Heat-sink is required.

Functional Descriptions

The basic structure of VA9201 is a differential amplifier with differential inputs and BTL outputs plus a built-in asynchronous boost control.

Gain Settings

The gain of the VA9201 amplifier can be set by GAIN pin. The gain ratios listed in Table 1 are implemented by changing the taps on the feedback resistors in the preamplifier stage.
The input resistance is depended on the gain setting. Since the gain setting is determined by the ratio of the internal feedback resistive network, the variation of the gain is small. But the absolute value of the input resistance may shift by ±20% at the same gain. In actual design cases, 80% of nominal value should be assumed as the input resistance of VA9201 in the input network of whole amplifier.

Gain	R_{DOWN}	R_{UP}	Input Impedance
20dB	5.6kΩ	OPEN	60kΩ
26dB	27kΩ	100kΩ	30kΩ
32db	39kΩ	100kΩ	15kΩ
36dB	47kΩ	75kΩ	9kΩ

Table 1. Gain Setting

Amplifier Input Impedance

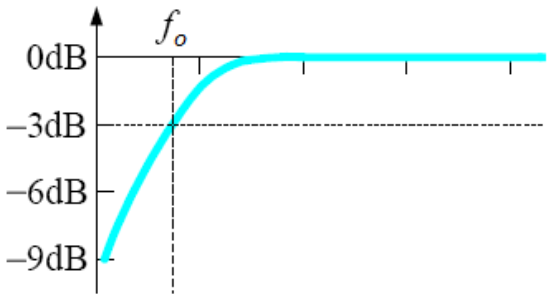


Figure 1. Cut-off point of high-pass filter

In most cases, no extra resistor needs to be added on the input of VA9201. The actual input resistor is already determined while selecting the gain. If a single capacitor is used in the input high-pass filter, the cut-off frequency *fo* may vary with the change of gain setting. The -3dB point of the cut-off frequency can be calculated by the following equation,

$$fo = \frac{1}{2\pi \times R_I \times C_I} \quad \text{(Hz)} \quad \text{Equation (2)}$$

,where the R_I values is given in Table 1.

Shutdown Operation

The VA9201 employs a state of shutdown mode to reduce supply current to the absolute minimum level during periods of nonuse for power conservation. This terminal should be held high during normal operation when the amplifier is in normal operating. Pulling low causes the output drivers shutdown and the amplifier to enter a low-current state. Do not leave it unconnected, because there is no weakly pulling resistor inside the amplifier.

Remember that to place the amplifier in the shutdown state prior to removing the power supply voltage so that power-off pop noise can be eliminated.

VREG Supply

The V_{REG} Supply is used to bias the gates of the output full-bridge upper half MOSFETs. It could be used to supply the PLIMIT pin and related voltage divider circuit. Add at least 1μF capacitor to ground at this pin.

Speaker Protection

Due to the nature of Class D amplifiers, the speakers may have DC current if the audio inputs

Functional Descriptions (cont.)

get DC voltage in any case. An output DC fault will make internal fault function in low state and shuts down the audio amplifier and change the state of output into high impedance.

To resolve the case of DC input, it is good to treat it as very low frequency sine wave much lower than audio band such as 2Hz. Based on this criteria, a DC detect fault shall be issued when the output differential duty-cycle of either channel exceeds 14% for more than 420ms at the same polarity. This feature protects the speakers away from large currents.

The minimum differential input DC voltages required to trigger the DC detection fault are listed in Table 2.

A_V (dB)	V_{IN} (mV, Differential)
36	17
32	28
26	56
20	112

Table 2. DC detect fault threshold

To resume the normal operation, it is necessary to power off the amplifier and then power on, cycling SD_B can not resume normal operation.

Short Circuit Protection

VA9201 has protection from over-current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the internal fault function to low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch would be cleared automatically or cycling the SD_B pin through the low state.

Thermal Protection

Thermal protection on the VA9201 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±30°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. VA9201 will be back to normal operation at this point with no external system interaction.

Thermal protection fault will not be reported on the internal fault function terminal.

Power Limit Operation

The voltage at PLIMIT terminal (pin 35) can be used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from VREG to ground to set the voltage at the PLIMIT terminal. An external reference may also be used if precise limitation is required. Also add a 1μF capacitor from this pin to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to power rail. This "virtual" rail is 5 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L}$$

V_P=5 x PLIMIT voltage if PLIMIT<5 x V_P

Functional Descriptions (cont.)

P_{OUT} (with 10% THD) = 1.25 x P_{OUT}

where R_S is the total series resistance including $R_{DS(ON)}$ and any resistance in the output filter. R_L is the load resistance. V_P is the peak amplifier of the output possible within the supply rail.

Due to the VREG driving ability limitation, it is not recommended to use this pin to drive other circuits except PLIMIT resistor network. The recommended resistor network is shown on Figure 2.

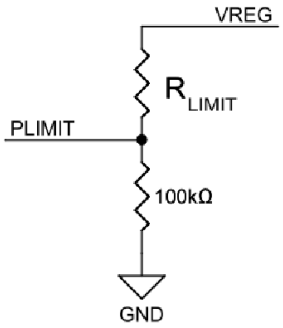


Figure 2. PLIMIT Pin Voltage Divider

Use the simple voltage divider to determine the voltage on PLIMIT pin from VREG pin by the following equation:

$$V_{PLIMIT} = V_{VREG} \frac{100\,k\Omega}{100\,k\Omega + R_{LIMIT}}$$

In order to maintain the regulation of VREG pin well please apply higher resistor value such as 100kΩ on low side resistor but should not less than 50kΩ.

Application Information

Output Filter

Design the VA9201 without the filter if the traces from amplifier to speaker are short (< 10cm), where the speaker is in the same enclosure as the amplifier is a typical application for class D without a filter. Many applications require a ferrite bead filter at least. The ferrite filter reduces EMI above 30MHz. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies, be aware of its maximum current limitation.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and there are long wires from the amplifier to the speaker.

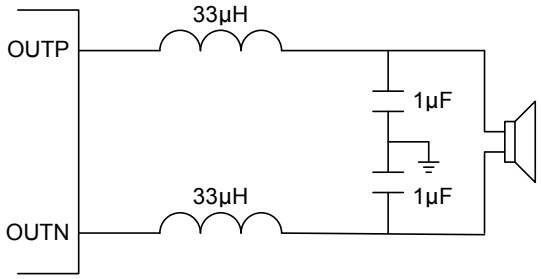


Figure 3. Typical LC Output Filter, Speaker Impedance=8Ω

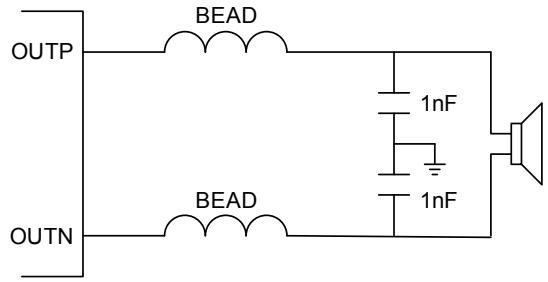


Figure 4. Typical Ferrite Chip Bead Output Filter

Inductors used in LC filters must be selected carefully. A significant change in inductance at the peak output current of the VA9201 will cause increased distortion. The change of inductance at currents up to the peak output current must be less than 0.1µH per amp to avoid this. Also note that smaller inductors than 33µH may cause an increase in distortion above what is shown in preceding graphs of THD versus frequency and output power.

Like the selection of the inductor in LC filters, the capacitor must be selected carefully, too. A significant change in capacitance at the peak output voltage of the VA9201 will cause increased distortion. LC filter capacitors should be double of DC voltage ratings of the peak application voltage (the power supply voltage) at least. In general, it is strongly recommended using capacitors with good temperature performance like X7R series.

Output Snubbers

In Figure 5, the 330pF capacitors in series with 10Ω resistors connected with the outputs of the VA9201 are snubber circuits. They smooth switching transitions and reduce overshoot and ringing. With these networks, THD+N can be improved at lower power levels and EMC can be reduced 2~4 dB at middle frequencies. They increase quiescent current by 3mA~11mA depending on supply voltage.

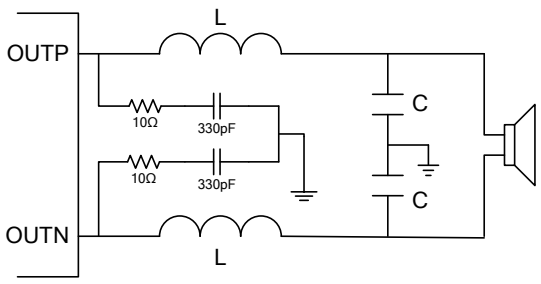


Figure 5. Output Snubber Circuits

Application Information (cont.)

Low ESR Capacitors

Low ESR capacitors are high recommended for this application. In general, a practical capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this unwanted resistor can eliminate the effects of the ideal capacitor. Place low ESR capacitors on supply circuitry can improve THD+N performance.

Boot-Strap Capacitors

The full H-bridge output stages use only MOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22μF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding boot-strap input. Specifically, one 0.22μF capacitor must be connected from OUTP to BSP, and one 0.22μF capacitor must be connected from OUTN to BSN.

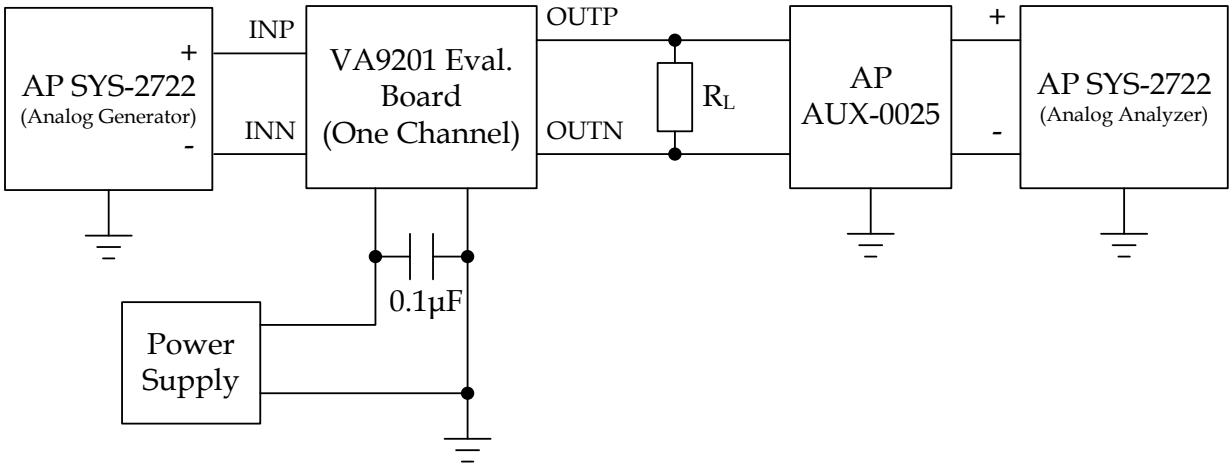
The bootstrap capacitors connected between the BSP or BSN pins and corresponding output function as a floating power supply for the high side N-channel power MOSFET gate drive circuitry. During each high side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Decoupling Capacitors

VA9201 requires appropriate power decoupling to minimize the output total harmonic distortion (THD) and improves EMC performance. Power supply decoupling also prevents intrinsic oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling can be achieved by using two different types of capacitors which target different types of noise on the power supply lines. For higher frequency spikes, or digital hash on the rail, a good low ESR ceramic capacitor, for example 0.1μF to 10μF, placed as close as possible to PVCC pins works best. For filtering lower frequency noise, a larger low ESR aluminum electrolytic capacitor of 470μF or greater placed near the audio power amplifier is suggested. The 470μF capacitor also serves as local storage capacitor for supplying current during heavy power output on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 470μF or larger capacitor should be placed by PVCC terminals as near as possible. And 0.1uF, 10μF ceramic capacitor on each PVCC terminal is also recommended.

Typical Characteristic

Test Setup Connection Diagram



* Remove all L/C (BEAD) filter components on board before performing all measurements.

Figure No.	Description
6	Frequency Response (8V to 17.5V)
7	Frequency Response (12V to 22.5V)
8	Noise Floor (8V to 17.5V)
9	Noise Floor (8V to 22.5V)
10	Noise Floor (8V to 22.5V)
11	THD+N vs. Freq. (8 to 17.5V 20dB)
12	THD+N vs. Freq. (8 to 17.5V 26dB)
13	THD+N vs. Freq. (8 to 17.5V 32dB)
14	THD+N vs. Freq. (8 to 17.5V 36dB)
15	THD+N vs. Freq. (12 to 22.5V 20dB)
16	THD+N vs. Freq. (12 to 22.5V 26dB)
17	THD+N vs. Freq. (12 to 22.5V 32dB)
18	THD+N vs. Freq. (12 to 22.5V 36dB)
19	Crosstalk (8 to 17.5V/8Ω/1W)
20	THD+N vs. Output Power (8V to 17.5V/8Ω)
21	THD+N vs. Output Power (12V to 22.5V/8Ω)

Typical Characteristic (cont.)

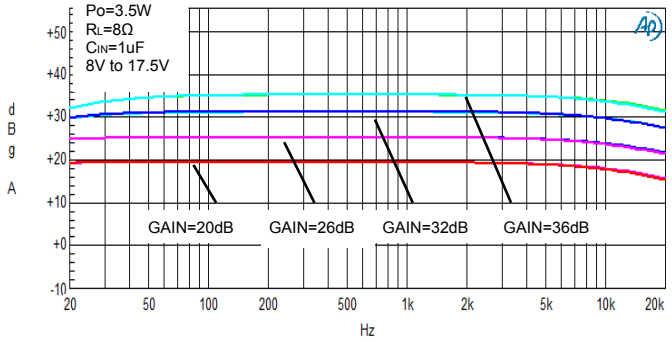


Figure 6. Frequency Response (8V to 17.5V)

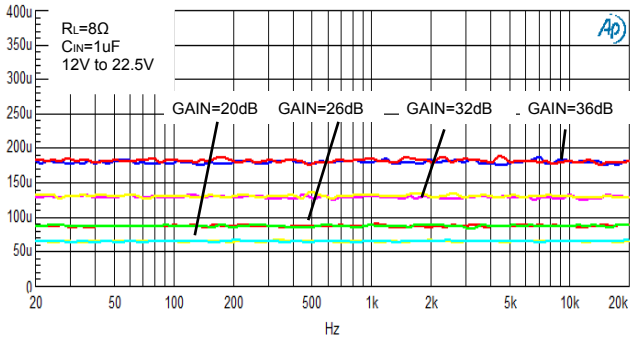


Figure 10. Noise Floor (12V to 22.5V)

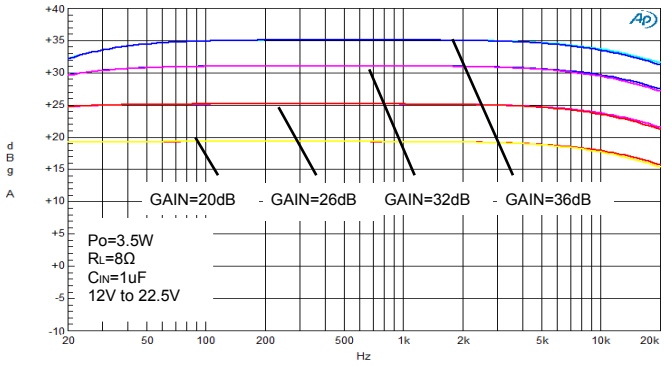


Figure 7. Frequency Response (12V to 22.5V)

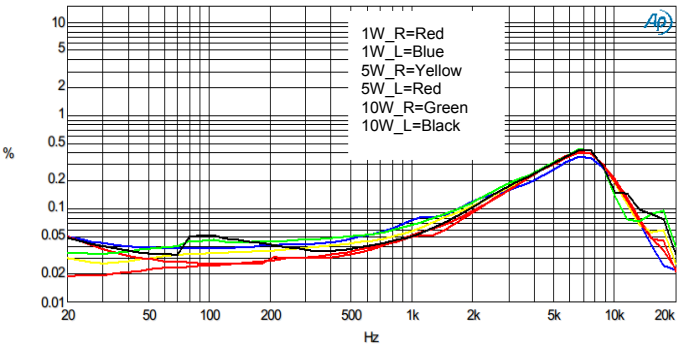


Figure 11. THD+N vs. Freq. (8 to 17.5V 20dB)

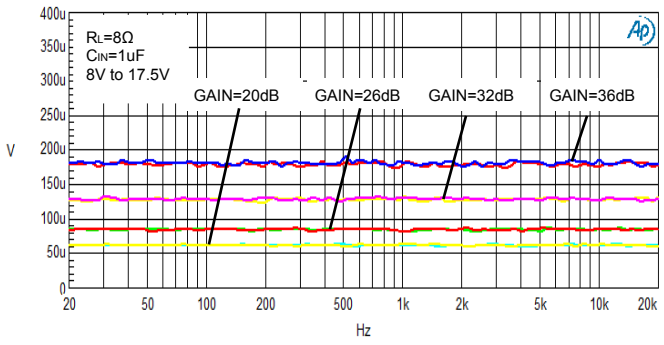


Figure 8. Noise Floor (8V to 17.5V)

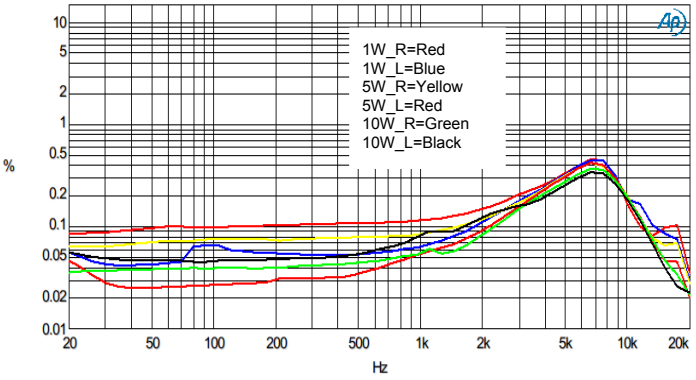


Figure 12. THD+N vs. Freq. (8 to 17.5V 26dB)

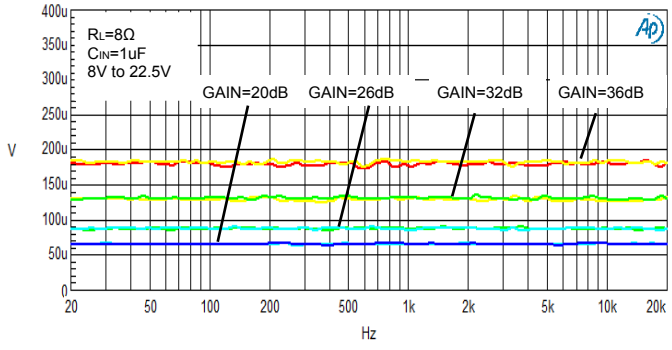


Figure 9. Noise Floor (8V to 22.5V)

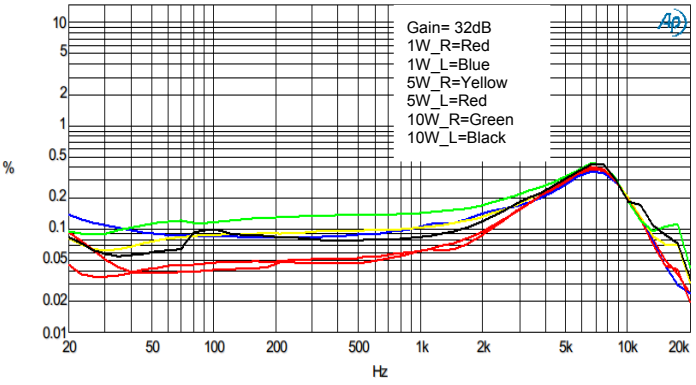


Figure 13. THD+N vs. Freq. (8 to 17.5V 32dB)

Typical Characteristic (cont.)

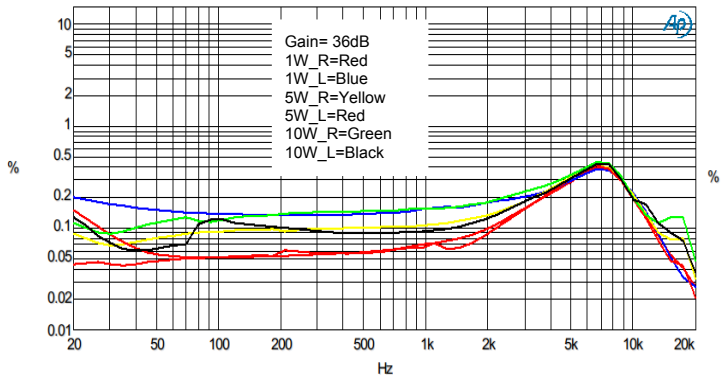


Figure 14. THD+N vs. Freq. (8 to 17.5V 36dB)

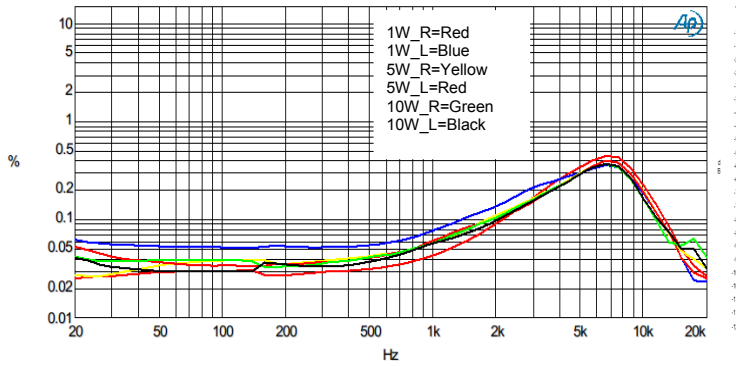


Figure 15. THD+N vs. Freq. (12 to 22.5V 20dB)

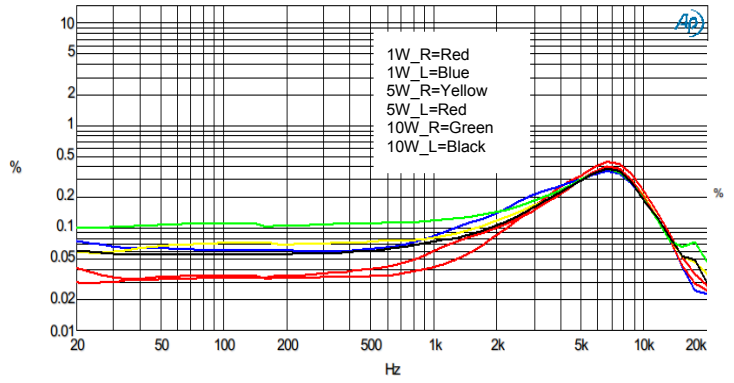


Figure 16. THD+N vs. Freq. (12 to 22.5V 26dB)

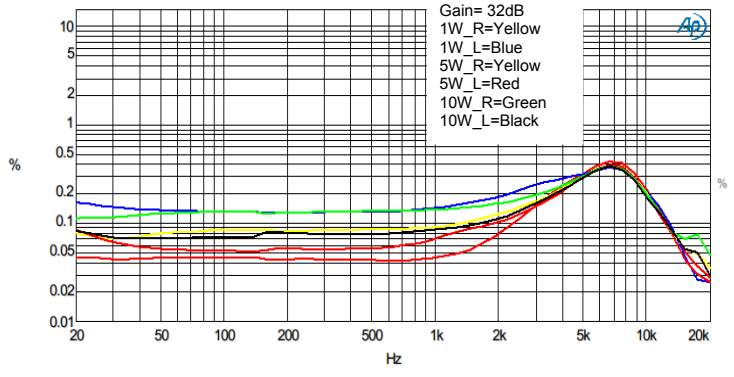


Figure 17. THD+N vs. Freq. (12 to 22.5V 32dB)

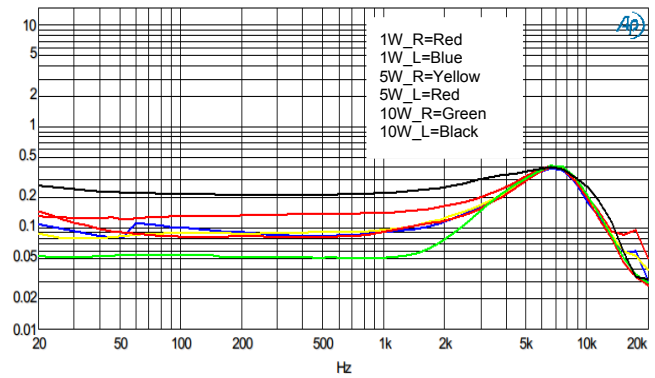


Figure 18. THD+N vs. Freq. (12 to 22.5V 36dB)

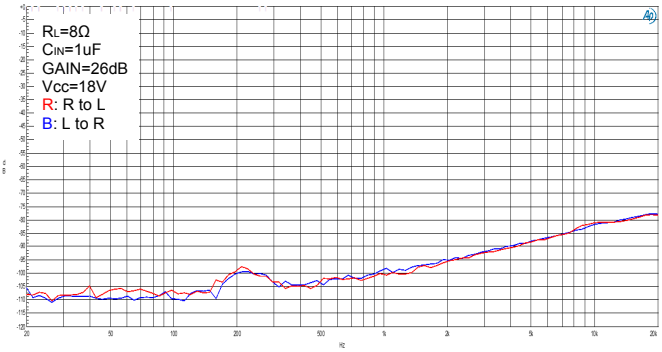


Figure 19. Crosstalk (8 to 17.5V/8Ω/1W)

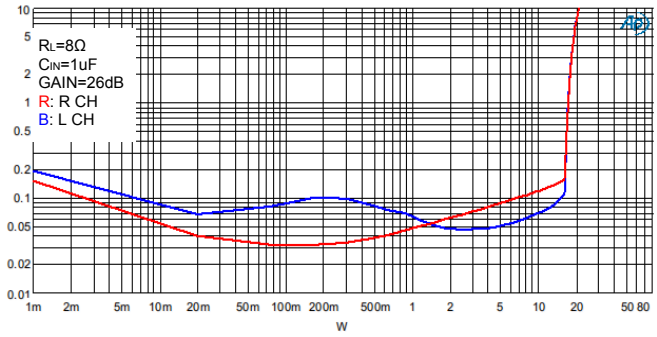


Figure 20. THD+N vs. Output Power (8V to 17.5V/8Ω)

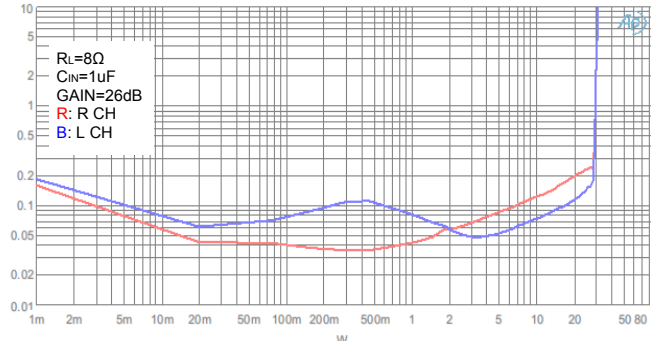
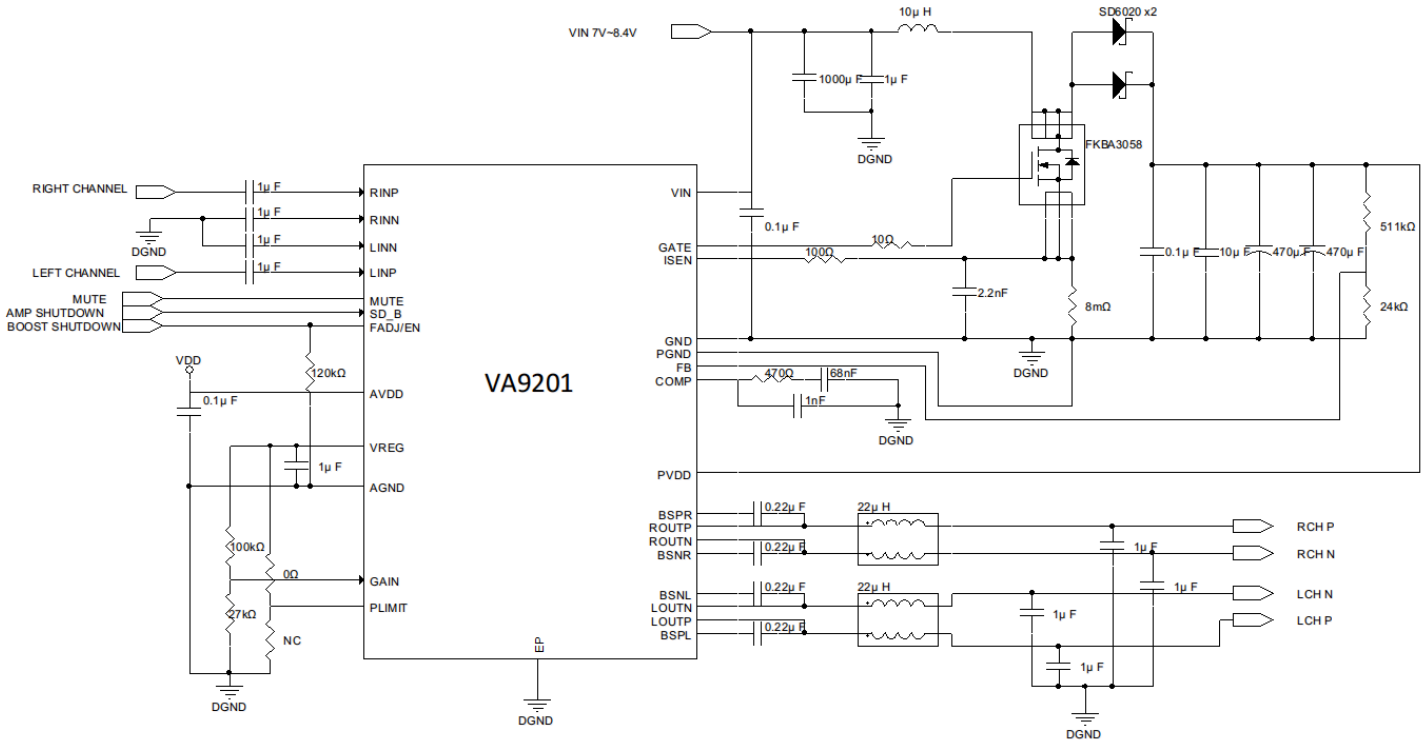


Figure 21. THD+N vs. Output Power (12V to 22.5V/8Ω)

Application Circuit 1: 20W Stereo Class D at 8Ω for 2-cell Li-ion Battery



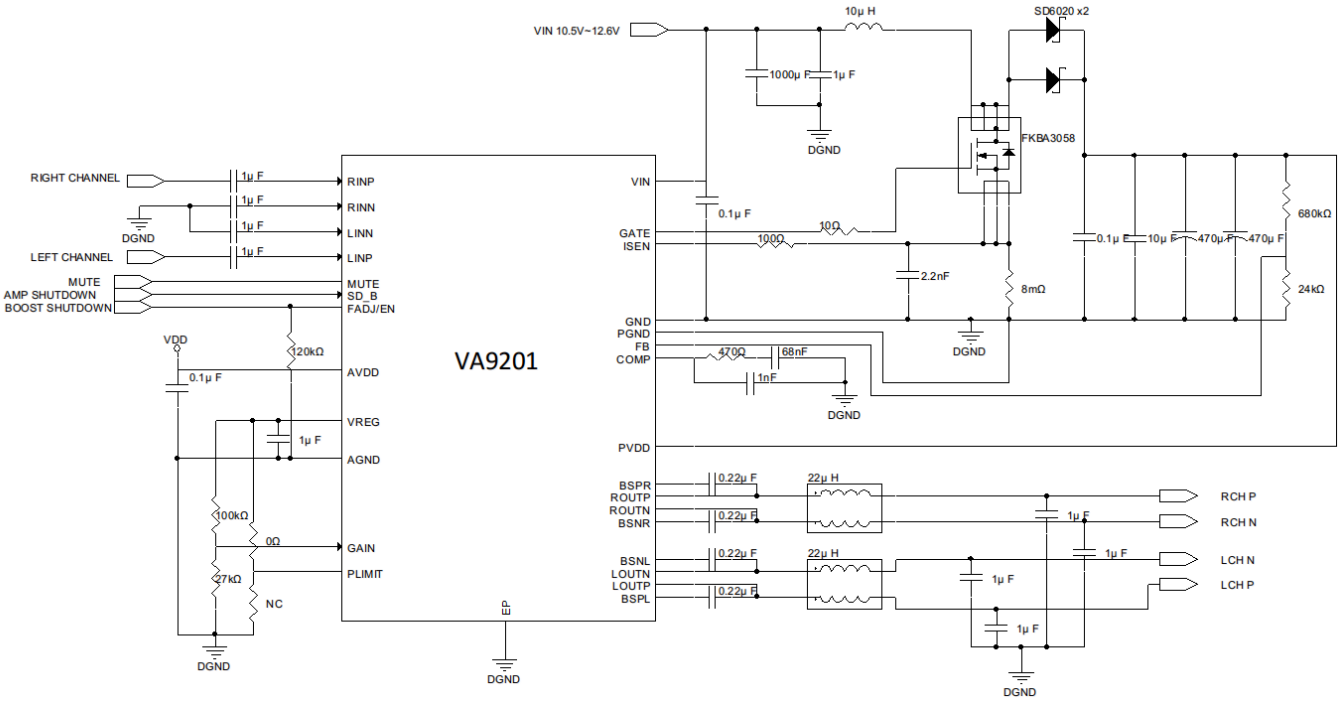
Reference Input:

V_{IN}=8V (Nominal), V_{CC}= 17.5V, Load=8Ω, Gain=26dB

Result:

Po=20Wx2, I_{IN}=5.85A, THD+N=7.6%

Application Circuit 2: 30W Stereo Class D at 8Ω for 3-cell Li-ion Battery



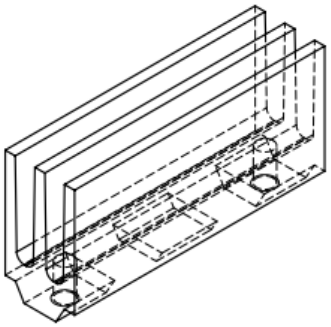
Reference Input:

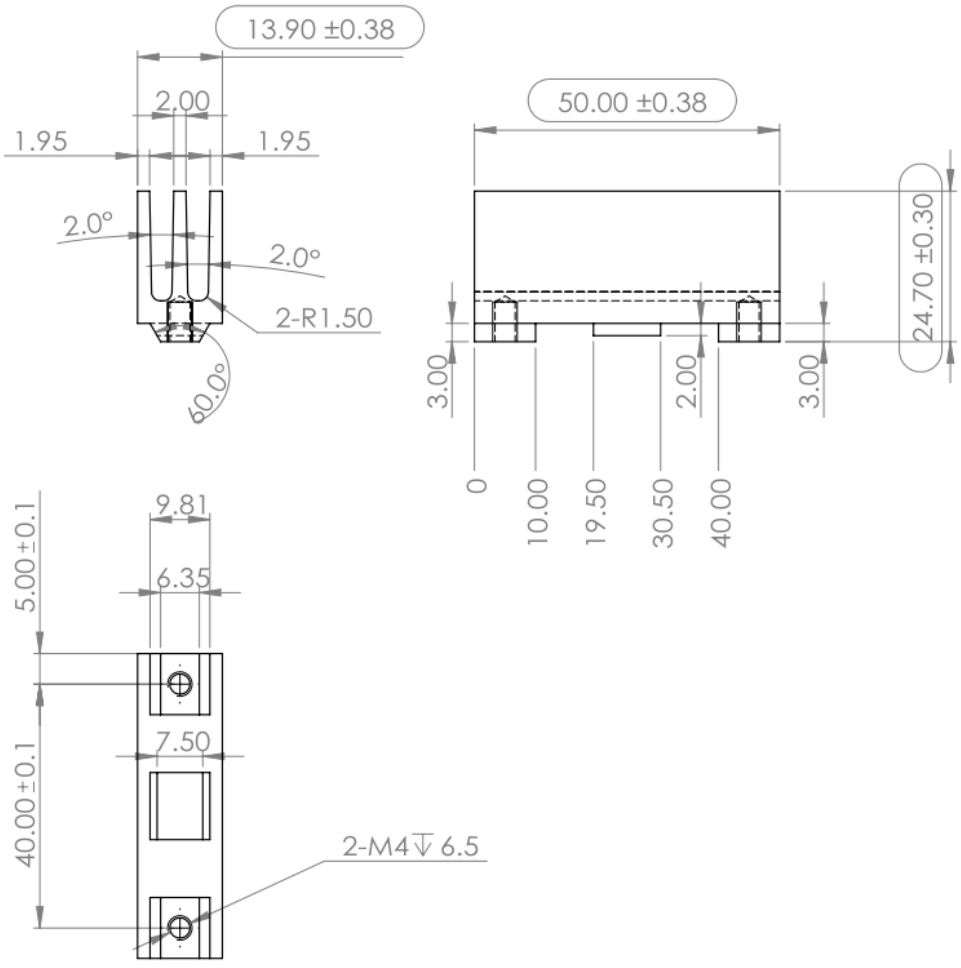
V_{IN}=12V (Nominal), V_{CC}= 22.5V, Load=8Ω, Gain=26dB

Result:

Po=30Wx2, I_{IN}=8.5A, THD+N=1.9%

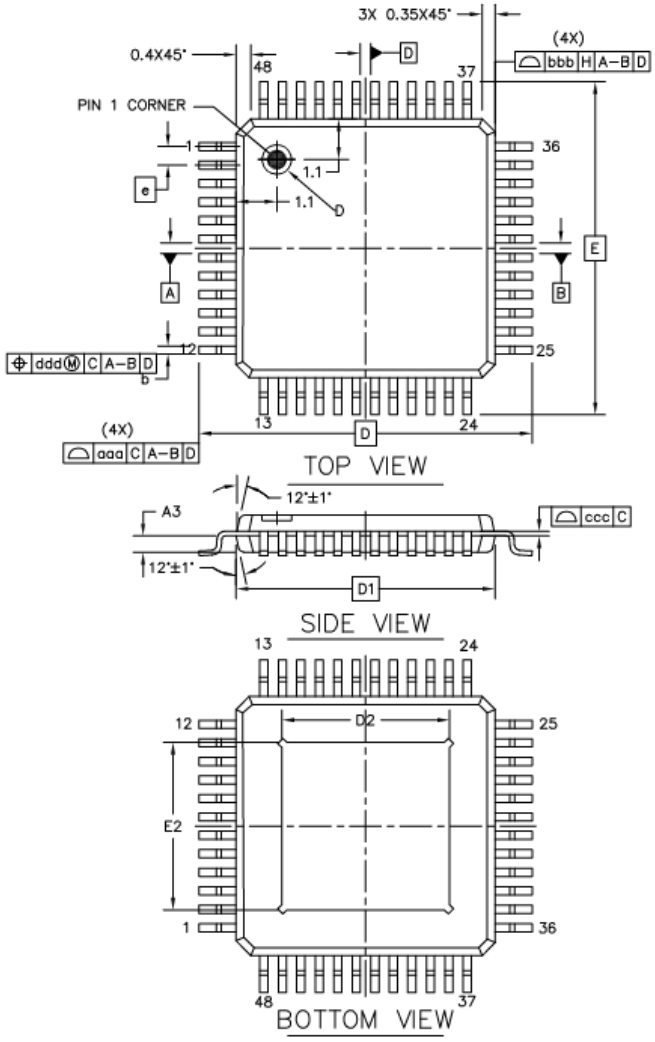
Heatsink Information

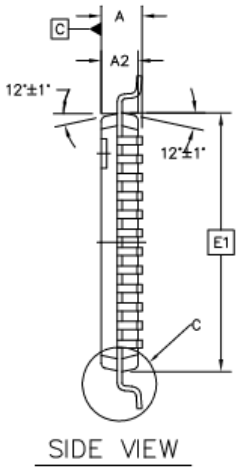


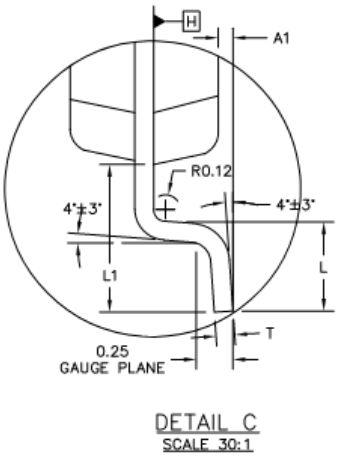


Package Information

TQFP-48 EP







		SYMBOL	MIN	NOM	MAX
OVER HEIGHT		A	---	---	1.20
STAND OFF		A1	0.05	0.10	0.15
MOLD THICKNESS		A2	0.95	1.00	1.05
		A3	0.411	0.436	0.461
LEAD WIDTH		b	0.17	---	0.27
LEAD THICKNESS		T	0.09	---	0.20
LEAD PITCH		e		0.5 BSC	
FOOT LENGTH		L	0.5	0.6	0.7
LEAD LENGTH		L1		1.0 REF	
LEAD TIP TO TIP	X	D		9 BSC	
	Y	E		9 BSC	
BODY SIZE	X	D1		7 BSC	
	Y	E1		7 BSC	
EXPOSED PAD SIZE	X	D2	4.43	4.53	4.63
	Y	E2	4.43	4.53	4.63
PROFILE OF LEAD TIPS		aaa		0.2	
PROFILE OF MOLD SURFACE		bbb		0.2	
FOOT COPLANARITY		ccc		0.08	
FOOT POSITION		ddd		0.08	

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