# MX29GL128F

# DATASHEET

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## SINGLE VOLTAGE 3V ONLY FLASH MEMORY

# FEATURES

### GENERAL FEATURES

- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
  - MX29GL128F H/L: VI/O=VCC=2.7V~3.6V, VI/O voltage must tight with VCC
  - MX29GL128F U/D: VI/O=1.65V~3.6V for Input/Output
- Byte/Word mode switchable
  - 16,777,216 x 8 / 8,388,608 x 16
- 64KW/128KB uniform sector architecture
  - 128 equal sectors
- 16-byte/8-word page read buffer
- 64-byte/32-word write buffer
- Extra 128-word sector for security
  - Features factory locked and identifiable, and customer lockable
- Advanced sector protection function (Solid and Password Protect)
- Latch-up protected to 100mA from -1V to 1.5xVcc
- Low Vcc write inhibit : Vcc ≤ VLKO
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- Deep power down mode

### PERFORMANCE

- High Performance
  - Fast access time:
    - MX29GL128F H/L: 70/90ns (VCC=2.7~3.6V)
    - MX29GL128F U/D: 90/110ns (VCC=2.7~3.6V, V I/O=1.65V to Vcc)
  - Page access time:
    - MX29GL128F H/L: 25ns
    - MX29GL128F U/D: 30ns
  - Fast program time: 10us/word
  - Fast erase time: 0.5s/sector
- Low Power Consumption
  - Low active read current: 10mA (typical) at 5MHz
  - Low standby current: 20uA (typical)
- Minimum 100,000 erase/program cycle
- 20 years data retention

### SOFTWARE FEATURES

- Program/Erase Suspend & Program/Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
  - Suspends sector program operation to read data from another sector which is not being program
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

### HARDWARE FEATURES

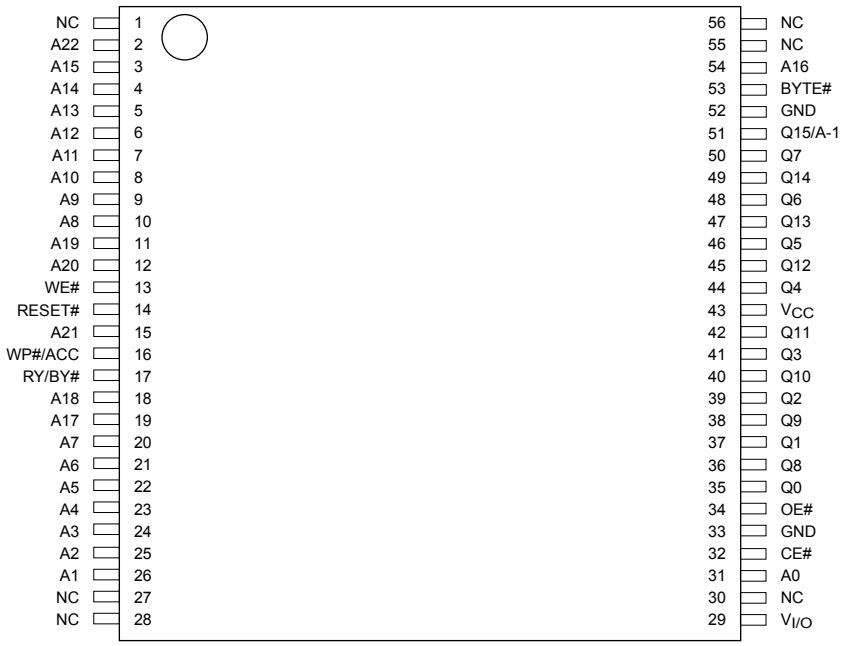
- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Hardware write protect pin/Provides accelerated program capability

### PACKAGE

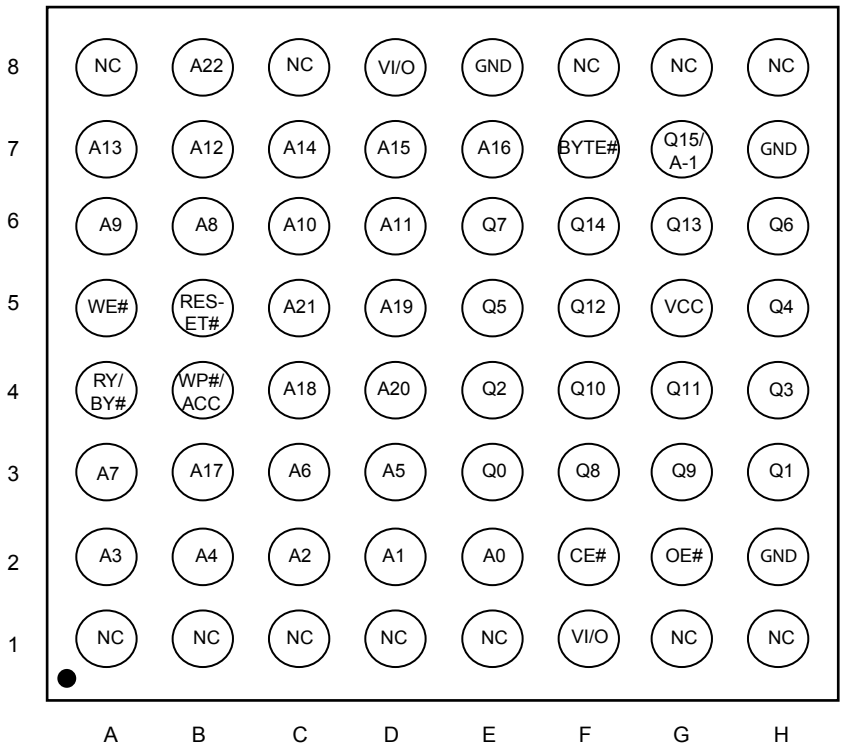
- 56-Pin TSOP
- 56-Ball FBGA (7mm x 9mm)
- 64-Ball LFBGA (11mm x 13mm)
- **All devices are RoHS Compliant and Halogen-free**

## PIN CONFIGURATION

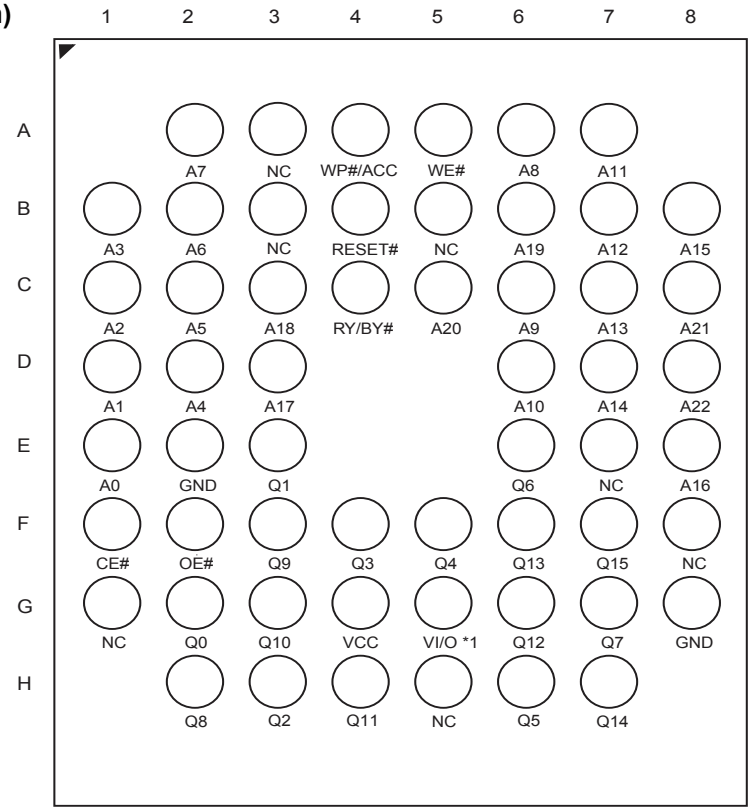
### 56 TSOP




### 64 LFBGA



**56 FBGA (7x9x1.2mm)**

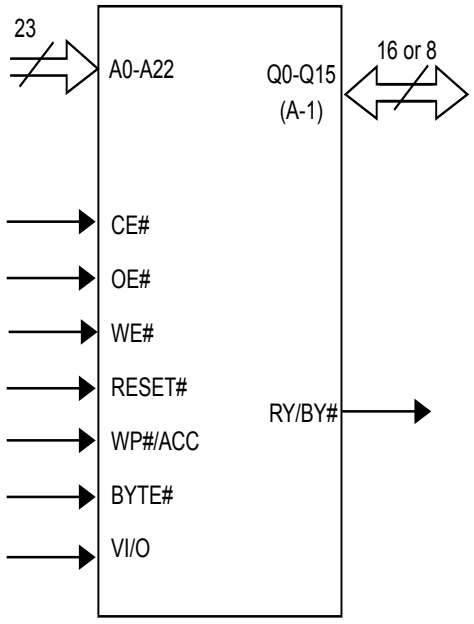



Note: *1. G5 pin is NC on MX29GL128F H/L.
*2. Only support word mode for 56-FBGA.

## PIN DESCRIPTION

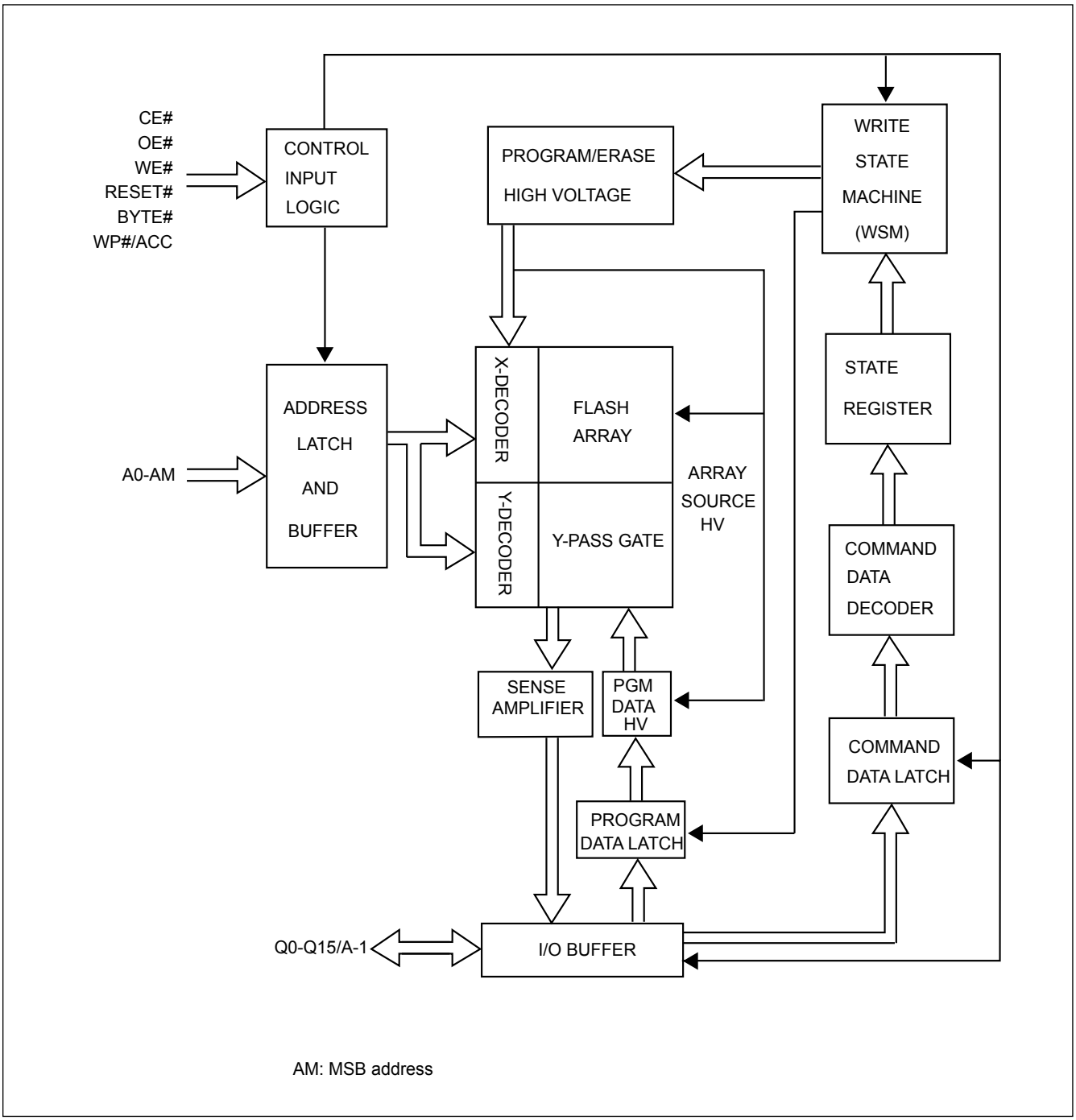
| SYMBOL | PIN NAME |
|---|---|
| A0~A22 | Address Input |
| Q0~Q14 | Data Inputs/Outputs |
| Q15/A-1 | Q15(Word Mode)/LSB addr(Byte Mode) |
| CE# | Chip Enable Input |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| RESET# | Hardware Reset Pin, Active Low |
| WP#/ACC* | Hardware Write Protect/Programming Acceleration input |
| RY/BY# | Ready/Busy Output |
| BYTE# | Selects 8 bits or 16 bits mode |
| VCC | +3.0V single power supply |
| GND | Device Ground |
| NC | Pin Not Connected Internally |
| VI/O | Power Supply for Input/Output |

## LOGIC SYMBOL




**Notes:**
1. WP#/ACC has internal pull up.
2. For MX29GL128F H/L VI/O voltage must tight with VCC.

## BLOCK DIAGRAM



## BLOCK DIAGRAM DESCRIPTION

The *block diagram* illustrates a simplified architecture of this device. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array.

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, BYTE#, and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM(A22). The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", AND "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the Y-PASS GATES. SENSE AMPLIFIERS are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15/A-1 pads. During read operation, the I/O BUFFER receives data from SENSE AMPLIFIERS and drives the output pads accordingly. In the last cycle of program command, the I/O BUFFER transmits the data on Q0-Q15/A-1 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word or byte according to the user input pattern.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER, FLASH ARRAY, and "PGM DATA HV" blocks. The logic control module comprises of the "WRITE STATE MACHINE, WSM", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-Q15/A-1 is latched in the COMMAND DATA LATCH and is decoded by the COMMAND DATA DECODER. The STATE REGISTER receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.

## ARRAY ARCHITECTURE

The main flash memory array can be organized as Byte mode (x8) or Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in *Table 1*.

## BLOCK STRUCTURE

**Table 1: SECTOR ARCHITECTURE**

| Sector Size | | Sector | Sector Address A22-A16 | (x16) Address Range |
|---|---|---|---|---|
| Kbytes | Kwords | | | |
| 128 | 64 | SA0 | 0000000xxx | 000000h-00FFFFh |
| 128 | 64 | SA1 | 0000001xxx | 010000h-01FFFFh |
| 128 | 64 | SA2 | 0000010xxx | 020000h-02FFFFh |
| 128 | 64 | SA3 | 0000011xxx | 030000h-03FFFFh |
| : | : | : | : | : |
| : | : | : | : | : |
| : | : | : | : | : |
| 128 | 64 | SA124 | 1111100xxx | 7C0000h-7CFFFFh |
| 128 | 64 | SA125 | 1111101xxx | 7D0000h-7DFFFFh |
| 128 | 64 | SA126 | 1111110xxx | 7E0000h-7EFFFFh |
| 128 | 64 | SA127 | 1111111xxx | 7F0000h-7FFFFFh |

## BUS OPERATION

**Table 2-1. BUS OPERATION**

| Mode Select | RE-SET# | CE# | WE# | OE# | Address (Note4) | Data I/O Q7~Q0 | Byte# Vil Data (I/O) Q15~Q8 | Byte# Vih Data (I/O) Q15~Q8 | WP#/ ACC |
|---|---|---|---|---|---|---|---|---|---|
| Device Reset | L | X | X | X | X | HighZ | HighZ | HighZ | L/H |
| Standby Mode | Vcc ± 0.3V | Vcc± 0.3V | X | X | X | HighZ | HighZ | HighZ | H |
| Output Disable | H | L | H | H | X | HighZ | HighZ | HighZ | L/H |
| Read Mode | H | L | H | L | AIN | DOUT | Q8-Q14= HighZ, Q15=A-1 | DOUT | L/H |
| Write | H | L | L | H | AIN | DIN | | DIN | Note1,2 |
| Accelerate Program | H | L | L | H | AIN | DIN | | DIN | Vhv |

**Notes:**
1. The first or last sector was protected if WP#/ACC=Vil.
2. When WP#/ACC = Vih, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the advanced protect feature.
3. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
4. In Word Mode (Byte#=Vih), the addresses are AM to A0, AM: MSB of address.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15), AM: MSB of address.

**Table 2-2. BUS OPERATION**

| Item | Control Input | | | AM to A12 | A11 to A10 | A9 | A8 to A7 | A6 | A5 to A4 | A3 to A2 | A1 | A0 | Q7 ~ Q0 | Q15 ~ Q8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CE# | WE# | OE# | | | | | | | | | | | |
| Sector Lock Status Verification | L | H | L | SA | X | $V_{hv}$ | X | L | X | L | H | L | 01h or 00h (Note 1) | X |
| Read Silicon ID Manufacturer Code | L | H | L | X | X | $V_{hv}$ | X | L | X | L | L | L | C2H | X |
| Read Silicon ID -- MX29GL128F | | | | | | | | | | | | | | |
| Cycle 1 | L | H | L | X | X | $V_{hv}$ | X | L | X | L | L | H | 7EH | 22H(Word), XXH(Byte) |
| Cycle 2 | L | H | L | X | X | $V_{hv}$ | X | L | X | H | H | L | 21H | 22H(Word), XXH(Byte) |
| Cycle 3 | L | H | L | X | X | $V_{hv}$ | X | L | X | H | H | H | 01H | 22H(Word), XXH(Byte) |

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: WP# protects high address sector: 99h.
   WP# protects low address sector: 89h
   Factory unlocked code: WP# protects high address sector: 19h.
   WP# protects low address sector: 09h
3. AM: MSB of address.

## FUNCTIONAL OPERATION DESCRIPTION

### READ OPERATION

To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving CE# & OE# LOW, and WE# HIGH. After the Tce and Toe timing requirements have been met, the system can read the contents of the addressed location by reading the Data (I/O) pins. If either the CE# or OE# is held HIGH, the outputs will remain tri-stated and no data will appear on the output pins.

### PAGE READ

This device is able to conduct Macronix MaskROM compatible high performance page read. Page size is 16 bytes or 8 words. The higher address Amax ~ A3 select the certain page, while A2~A0 for word mode, A2~A-1 for byte mode select the particular word or byte in a page. The page access time is Taa or Tce, following by Tpa for the rest of the page read time. When CE# toggles, access time is Taa or Tce. Page mode can be turned on by keeping "page-read address" constant and changing the "intra-read page" addresses.

### WRITE OPERATION

To perform a write operation, the system provides the desired address on the address pins, enables the chip by asserting CE# LOW, and disables the Data (I/O) pins by holding OE# HIGH. The system then places data to be written on the Data (I/O) pins and pulses WE# LOW. The device captures the address information on the falling edge of WE# and the data on the rising edge of WE#. To see an example, please refer to the timing diagram in *Figure 4*. The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device. Writing an invalid command may put the device in an undefined state.

### DEVICE RESET

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the middle of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode. Until the device does returns to Read mode, the RY/BY# pin will remain Low (Busy Status).

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

### STANDBY MODE

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (Isb) current.

## FUNCTIONAL OPERATION DESCRIPTION (cont'd)

### OUTPUT DISABLE

While in active mode (RESET# HIGH and CE# LOW), the OE# pin controls the state of the output pins. If OE# is held HIGH, all Data (I/O) pins will remain tri-stated. If held LOW, the Byte or Word Data (I/O) pins will drive data.

### BYTE/WORD SELECTION

The BYTE# input pin is used to select the organization of the array data and how the data is input/output on the Data (I/O) pins. If the BYTE# pin is held HIGH, Word mode will be selected and all 16 data lines (Q0 to Q15) will be active.

If BYTE# is forced LOW, Byte mode will be active and only data lines Q0 to Q7 will be active. Data lines Q8 to Q14 will remain in a high impedance state and Q15 becomes the A-1 address input pin.

### HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW. The highest or lowest was protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), these sectors revert to their previously protected/unprotected status.

### ACCELERATED PROGRAMMING OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Programming mode. This mode permits the system to skip the normal command unlock sequences and program byte/word locations directly. During accelerated programming, the current drawn from the WP#/ACC pin is no more than ICP1.

### WRITE BUFFER PROGRAMMING OPERATION

Programs 64bytes/32words in a programming operation. To trigger the Write Buffer Programming, start by the first two unlock cycles, then third cycle writes the Write Buffer Load command at the destined programming Sector Address. The forth cycle writes the "word locations subtract one" number.

Following above operations, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page.

The "write-buffer-page" is selected by choosing address Amax-A5.

"Write-Buffer-Page" address has to be the same for all address/ data write into the write buffer. If not, operation will ABORT.

To program the content of the write buffer page this command must be followed by a write to buffer Program confirm command.

The operation of write-buffer can be suspended or resumed by the standard commands, once the write buffer programming operation is finished, it'll return to normal READ mode.

## FUNCTIONAL OPERATION DESCRIPTION (cont'd)

### WRITE BUFFER PROGRAMMING OPERATION (cont'd)

ABORT will be executed for the Write Buffer Programming Sequence if following condition occurs:
- The value loaded is bigger than the page buffer size during "Number of Locations to Program"
- Address written in a sector is not the same as the one assigned during the Write-Buffer-Load command.
- Address/ Data pair written to a different write-buffer-page than the one assigned by the "Starting Address" during the "write buffer data loading" operation.
- Writing not "Confirm Command" after the assigned number of "data load" cycles.

At Write Buffer Abort mode, the status register will be Q1=1, Q7=DATA# (last address written), Q6=toggle.
A Write-to-Buffer-Abort Reset command sequence has to be written to reset the device for the next operation.

Write buffer programming can be conducted in any sequence. However the CFI functions, autoselect, Secured Silicon sector are not functional when program operation is in progress. Multiple write buffer programming operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can't be programmed from 0 back to 1.

### SECTOR PROTECT OPERATION

The device provides user programmable protection operations for selected sectors. Please refer to *Table 1* which show all Sector assignments.

During the protection operation, the sector address of any sector may be used to specify the Sector being protected.

### AUTOMATIC SELECT BUS OPERATIONS

The following five bus operations require A9 to be raised to Vhv. Please see AUTOMATIC SELECT COMMAND SEQUENCE in the COMMAND OPERATIONS section for details of equivalent command operations that do not require the use of Vhv.

### SECTOR LOCK STATUS VERIFICATION

To determine the protected state of any sector using bus operations, the system performs a READ OPERATION with A9 raised to Vhv, the sector address applied to address pins A22 to A12, address pins A6, A3, A2 & A0 held LOW, and address pin A1 held HIGH. If data bit Q0 is LOW, the sector is not protected, and if Q0 is HIGH, the sector is protected.

## FUNCTIONAL OPERATION DESCRIPTION (cont'd)

### READ SILICON ID MANUFACTURER CODE

To determine the Silicon ID Manufacturer Code, the system performs a READ OPERATION with A9 raised to Vhv and address pins A6, A3, A2, A1, & A0 held LOW. The Macronix ID code of C2h should be present on data bits Q7 to Q0.

### READ INDICATOR BIT (Q7) FOR SECURITY SECTOR

To determine if the Security Sector has been locked at the factory, the system performs a READ OPERATION with A9 raised to Vhv, address pin A6, A3 & A2 held LOW, and address pins A1 & A0 held HIGH. If the Security Sector has been locked at the factory, the code 99h(H)/89h(L) will be present on data bits Q7 to Q0. Otherwise, the factory unlocked code of 19h(H)/09h(L) will be present.

### INHERENT DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to Read mode during power up. Additionally, the following design features protect the device from unintended data corruption.

### COMMAND COMPLETION

Only after the successful completion of the specified command sets will the device begin its erase or program operation. The failure in observing valid command sets will result in the memory returning to read mode.

### LOW VCC WRITE INHIBIT

The device refuses to accept any program/erase command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and program/erase commands are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

### WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

### LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.

## FUNCTIONAL OPERATION DESCRIPTION (cont'd)

### POWER-UP SEQUENCE

Upon power up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

### POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

### POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

## COMMAND OPERATIONS

### READING THE MEMORY ARRAY

Read mode is the default state after power up or after a reset operation. To perform a read operation, please refer to READ OPERATION in the BUS OPERATIONS section above.

If the device receives an Erase Suspend command while in the Sector Erase state, the erase operation will pause (after a time delay not exceeding 20us) and the device will enter Erase-Suspended Read mode. While in the Erase-Suspended Read mode, data can be programmed or read from any sector not being erased. Reading from addresses within sector (s) being erased will only return the contents of the status register, which is in fact how the current status of the device can be determined.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the device will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where is was suspended and will continue until it completes successfully or another Erase Suspend command is received.

After the memory device completes an embedded operation (automatic Chip Erase, Sector Erase, or Program) successfully, it will automatically return to Read mode and data can be read from any address in the array. If the embedded operation fails to complete, as indicated by status register bit Q5 (exceeds time limit flag) going HIGH during the operations, the system must perform a reset operation to return the device to Read mode.

There are several states that require a reset operation to return to Read mode:

1. A program or erase failure--indicated by status register bit Q5 going HIGH during the operation. Failures during either of these states will prevent the device from automatically returning to Read mode.

2. The device is in Auto Select mode or CFI mode. These two states remain active until they are terminated by a reset operation.

In the two situations above, if a reset operation (either hardware reset or software reset command) is not performed, the device will not return to Read mode and the system will not be able to read array data.

### AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY

The device provides the user the ability to program the memory array in Byte mode or Word mode. As long as the users enters the correct *cycle* defined in the *Table 3* (including 2 unlock cycles and the A0H program command), any byte or word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, the user only needs to enter the program command and data once.

## COMMAND OPERATIONS (cont'd)

### AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY (cont'd)

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset or program suspend. Hard ware reset will terminate the program operation after a period of time no more than 10us. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode. Program suspend ready, the device will enter program suspend read mode.

After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register:

| Status | Q7*1 | Q6*1 | Q5 | Q1 | RY/BY# (Note) |
|---|---|---|---|---|---|
| In progress | Q7# | Toggling | 0 | 0 | 0 |
| Exceed time limit | Q7# | Toggling | 1 | N/A | 0 |

**Note:** RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

### ERASING THE MEMORY ARRAY

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, one or more selected sectors may be erased simultaneously. In the Chip Erase operation, the complete memory array is erased except for any protected sectors. More details of the protected sectors are explained in section *Advanced Sector Protection/Un-protection*.

### SECTOR ERASE

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command. After the sector erase command sequence has been issued, an internal 50us time-out counter is started. Until this counter reaches zero, additional sector addresses and Sector Erase commands may be issued thus allowing multiple sectors to be selected and erased simultaneously. After the 50us time-out counter has expired, no new commands will be accepted and the embedded sector erase operation will begin. *Note that the 50us timer-out counter is restarted after every erase command sequence.* If the user enters any command other than Sector Erase or Erase Suspend during the time-out period, the erase operation will abort and the device will return to Read mode.

After the embedded sector erase operation begins, all commands except Erase Suspend will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode.

**COMMAND OPERATIONS (cont'd)**

**SECTOR ERASE (cont'd)**

The system can determine the status of the embedded sector erase operation by the following methods:

| Status | Q7 | Q6 | Q5 | Q3*1 | Q2 | RY/BY#*2 |
|---|---|---|---|---|---|---|
| Time-out period | 0 | Toggling | 0 | 0 | Toggling | 0 |
| In progress | 0 | Toggling | 0 | 1 | Toggling | 0 |
| Exceeded time limit | 0 | Toggling | 1 | 1 | Toggling | 0 |

**Notes:**
1. The Q3 status bit is the 50us time-out indicator. When Q3=0, the 50us time-out counter has not yet reached zero and a new Sector Erase command may be issued to specify the address of another sector to be erased. When Q3=1, the 50us time-out counter has expired and the Sector Erase operation has already begun. Erase Suspend is the only valid command that may be issued once the embedded erase operation is underway.
2. RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.
3. When an attempt is made to erase only protected sector (s), the erase operation will abort thus preventing any data changes in the protected sector (s). Q7 will output "0" and Q6 will toggle briefly (100us or less) before aborting and returning the device to Read mode. If unprotected sectors are also specified, however, they will be erased normally and the protected sector (s) will remain unchanged.
4. Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode).

**CHIP ERASE**

The Chip Erase operation is used erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase, the chip will automatically return to Read mode.

The system can determine the status of the embedded chip erase operation by the following methods:

| Status | Q7 | Q6 | Q5 | Q2 | RY/BY#*1 |
|---|---|---|---|---|---|
| In progress | 0 | Toggling | 0 | Toggling | 0 |
| Exceed time limit | 0 | Toggling | 1 | Toggling | 0 |

*1: RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.

## COMMAND OPERATIONS (cont'd)

### ERASE SUSPEND/RESUME

After beginning a sector erase operation, Erase Suspend is the only valid command that may be issued. If system issues an Erase Suspend command during the 50us time-out period following a Sector Erase command, the time-out period will terminate immediately and the device will enter Erase-Suspended Read mode. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until 20us time has elapsed. The system can determine if the device has entered the Erase-Suspended Read mode through Q6, Q7, and RY/BY#.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector (s) except those being erased by the suspended erase operation. Reading any sector being erased or programmed will return the contents of the status register. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. The system can use the status register bits shown in the following table to determine the current state of the device:

| Status | Q7 | Q6 | Q5 | Q3 | Q2 | Q1 | RY/BY# |
|---|---|---|---|---|---|---|---|
| Erase suspend read in erase suspended sector | 1 | No toggle | 0 | N/A | toggle | N/A | 1 |
| Erase suspend read in non-erase suspended sector | Data | Data | Data | Data | Data | Data | 1 |
| Erase suspend program in non-erase suspended sector | Q7# | Toggle | 0 | N/A | N/A | N/A | 0 |

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

### SECTOR ERASE RESUME

The sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase resumes, the user can issue another Ease Suspend command, but there should be a 400us interval between Ease Resume and the next Erase Suspend command.

## COMMAND OPERATIONS (cont'd)

### PROGRAM SUSPEND/RESUME

After beginning a program operation, Program Suspend is the only valid command that may be issued. The system can determine if the device has entered the Program-Suspended Read mode through Q6 and RY/BY#.

After the device has entered Program-Suspended mode, the system can read any sector (s) except those being programmed by the suspended program operation. Reading the sector being program suspended is invalid. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another program command. The system can use the status register bits shown in the following table to determine the current state of the device:

| Status | Q7 | Q6 | Q5 | Q3 | Q2 | Q1 | RY/BY# |
|---|---|---|---|---|---|---|---|
| Program suspend read in program suspended sector | Invalid | | | | | | 1 |
| Program suspend read in non-program suspended sector | Data | Data | Data | Data | Data | Data | 1 |

When the device has Program/Erase suspended, user can execute read array, auto-select, read CFI, read security silicon.

### PROGRAM RESUME

The Program Resume command is valid only when the device is in Program-Suspended mode. After program resumes, the user can issue another Program Suspend command, but there should be a 5us interval between Program Resume and the next Program Suspend command.

### BUFFER WRITE ABORT

Q1 is the indicator of Buffer Write Abort. When Q1=1, the device will abort from buffer write and go back to read status register shown as following table:

| Status | Q7 | Q6 | Q5 | Q3 | Q2 | Q1 | RY/BY# |
|---|---|---|---|---|---|---|---|
| Buffer Write Busy | Q7# | Toggle | 0 | N/A | N/A | 0 | 0 |
| Buffer Write Abort | Q7# | Toggle | 0 | N/A | N/A | 1 | 0 |
| Buffer Write Exceeded Time Limit | Q7# | Toggle | 1 | N/A | N/A | 0 | 0 |

## COMMAND OPERATIONS (cont'd)

### AUTOMATIC SELECT OPERATIONS

When the device is in Read mode, Program Suspended mode, Erase-Suspended Read mode, or CFI mode, the user can issue the *Automatic Select* command shown in *Table 3* (two unlock cycles followed by the Automatic Select command 90h) to enter Automatic Select mode. After entering Automatic Select mode, the user can query the Manufacturer ID, Device ID, Security Sector locked status, or Sector protected status multiple times without issuing a new Automatic Select command.

While In Automatic Select mode, issuing a Reset command (F0h) will return the device to Read mode (or Ease-Suspended Read mode if Erase-Suspend was active) or Program Suspended Read mode if Program Suspend was active.

Another way to enter Automatic Select mode is to use one of the bus operations shown in *Table 2-2. BUS OPERATION*. After the high voltage (Vhv) is removed from the A9 pin, the device will automatically return to Read mode or Erase-Suspended Read mode.

### AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not secured silicon is locked and whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The Reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

| | Address | | Data (Hex) | Representation |
|---|---|---|---|---|
| Manufacturer ID | Word | X00 | C2 | |
| | Byte | X00 | C2 | |
| Device ID | Word | X01/0E/0F | 227E/2221/2201 | |
| | Byte | X02/1C/1E | 7E/21/01 | |
| Secured Silicon | Word | X03 | 99/19 (H) | Factory locked/unlocked |
| | | | 89/09 (L) | |
| | Byte | X06 | 99/19 (H) | Factory locked/unlocked |
| | | | 89/09 (L) | |
| Sector Protect Verify | Word | (Sector address) X 02 | 00/01 | Unprotected/protected |
| | Byte | (Sector address) X 04 | 00/01 | Unprotected/protected |

After entering automatic select mode, no other commands are allowed except the reset command.

**COMMAND OPERATIONS (cont'd)**

**READ MANUFACTURER ID OR DEVICE ID**

The Manufacturer ID (identification) is a unique hexadecimal number assigned to each manufacturer by the JEDEC committee. Each company has its own manufacturer ID, which is different from the ID of all other companies. The number assigned to Macronix is C2h.

After entering Automatic Select mode, performing a read operation with A1 & A0 held LOW will cause the device to output the Manufacturer ID on the Data I/O (Q7 to Q0) pins.

**RESET**

In the following situations, executing reset command will reset device back to Read mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Auto-select mode
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in Auto-Select mode or CFI mode, user must issue reset command to reset device back to read array mode.

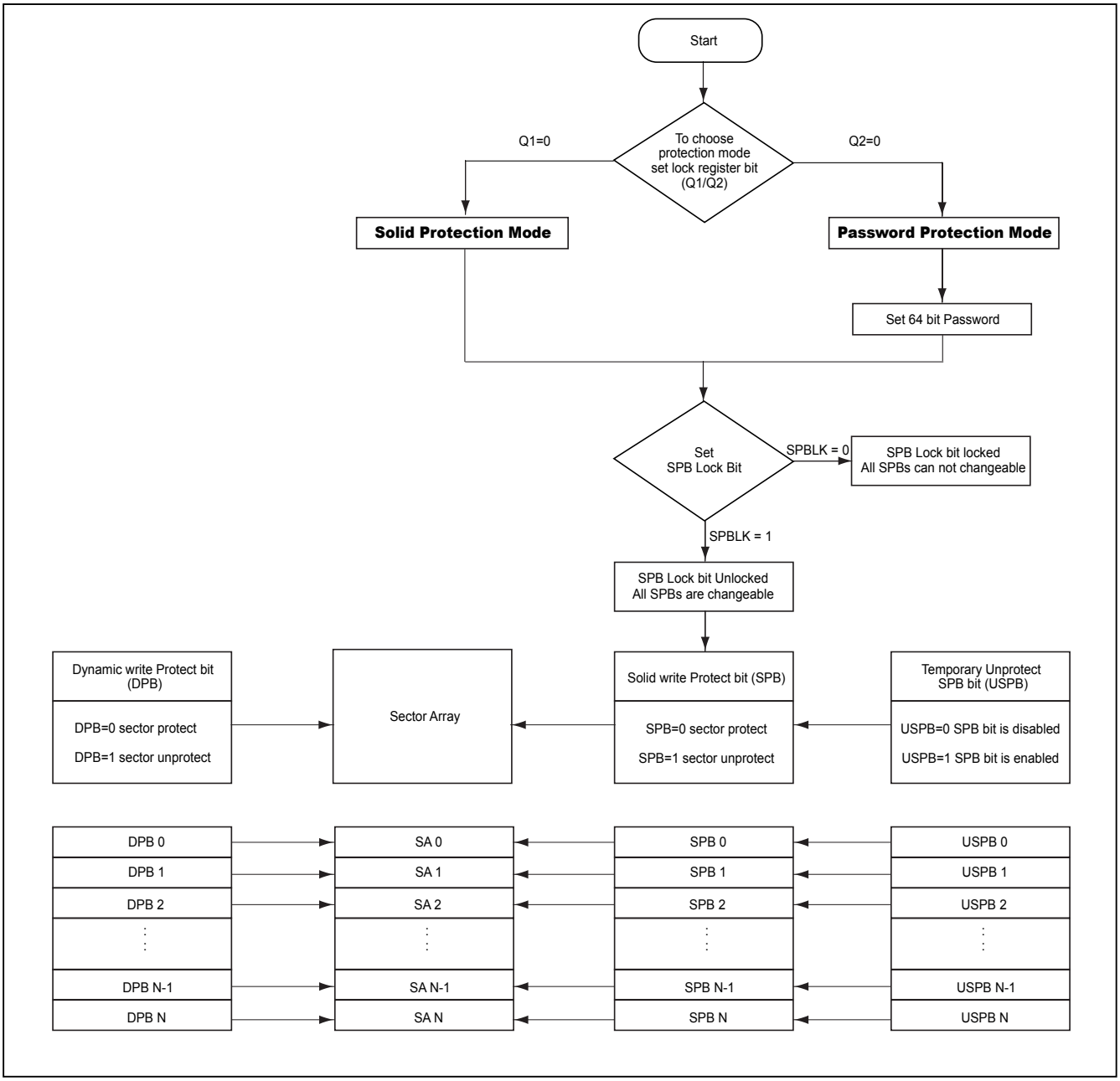
When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

## ADVANCED SECTOR PROTECTION/UN-PROTECTION

There are two ways to implement software Advanced Sector Protection on this device: Password method or Solid methods. Through these two protection methods, user can disable or enable the programming or erasing operation to any individual sector or the whole chip. The figure below helps to describe an overview of these methods.

The device is default to the Solid mode. All sectors are default as unprotected when shipped from factory.
The detailed algorithm of advance sector protection is shown as follows:

**Figure 1. Advance Sector Protection/Unprotection SPB Program Algorithm**



### 1. Lock Register

User can choose the sector protecting method via setting Lock Register bits as Q1 and Q2. Lock Register is a 16-bit one-time programmable register. Once programming either Q1 or Q2, they will be locked in that mode and the others will be disabled permanently. Q1 and Q2 can not be programmed at the same time, otherwise the device will abort the operation.

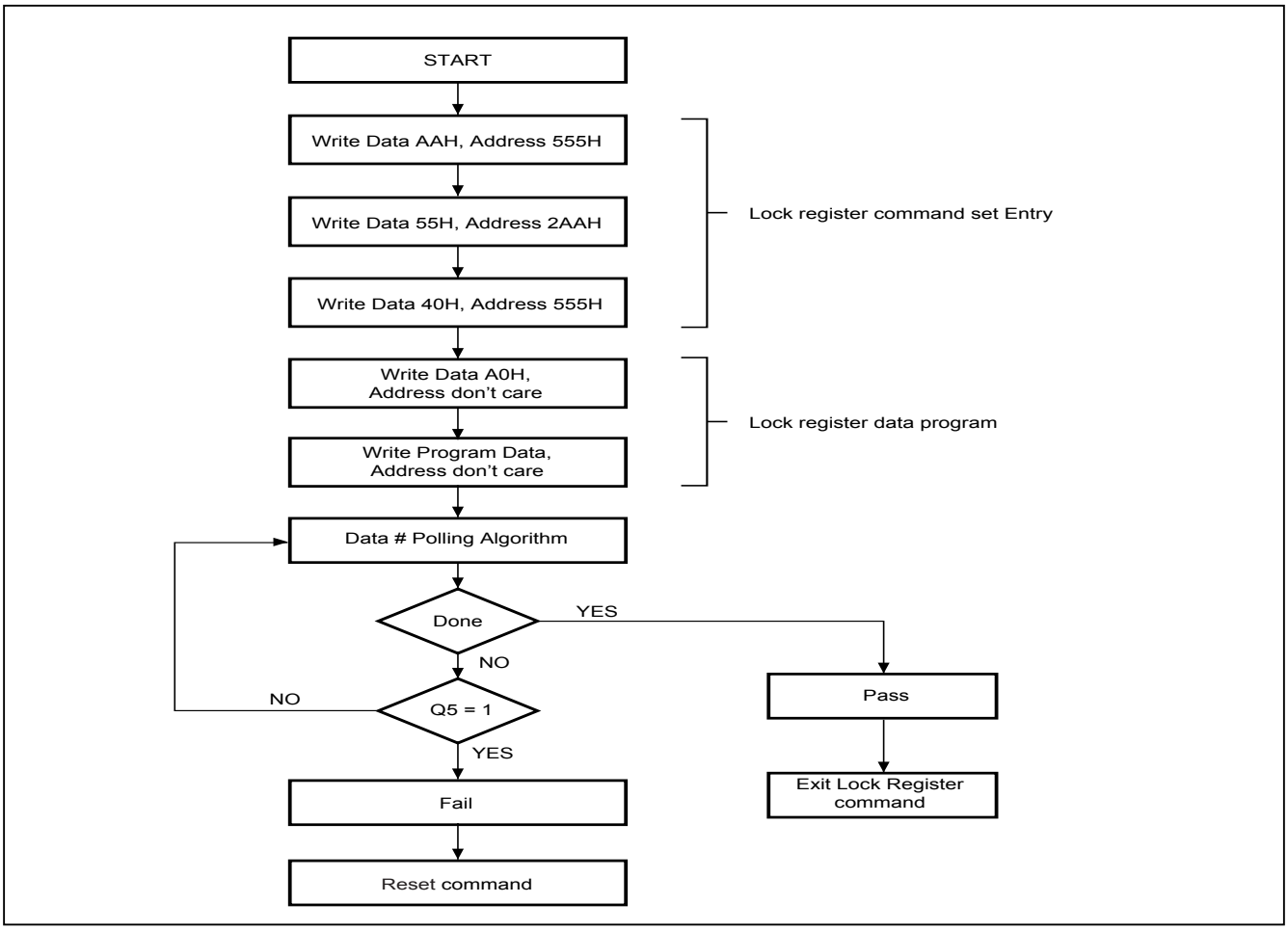
If users select Password Protection mode, the password setting is required. Users can set password by issuing password program command.

**Lock Register bits**

| Q15-Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|
| Don't care | Password Protection Mode Lock Bit | Solid Protection Mode Lock Bit | Secured Silicon Sector Protection Bit |

Please refer to the command for Lock Register command set about how to read and program the Lock Register bits.

**Figure 2. Lock Register Program Algorithm**



## 2. Solid Protection Mode

### 2.1 Solid write Protection Bits (SPB)

The Solid write Protection bits (SPB) are nonvolatile bit with the same endurances as the Flash memory. Each SPB is assigned to each sector individually. The SPB is preprogrammed, and verified prior to erasure are managed by the device, so system monitoring is not necessary.

When SPB is set to “0”, the associated sector may be protected, preventing any program or erase operation on this sector. Whether the sector is protected depends also upon the value of the USPB, as described elsewhere. The SPB bits are set individually by SPB program command. However, it cannot be cleared individually. Issuing the All SPB Erase command will erase all SPB in the same time. During SPB programming period, the read and write operations are disabled for normal sector until exiting this mode.

To unprotect a protected sector, the SPB lock bit must be cleared first by using a hardware reset or a power-up cycle. After the SPB lock bit is cleared, the SPB status can be changed to the desired settings. To lock the Solid Protection Bits after the modification has finished, the SPB Lock Bit must be set once again.

To verify the state of the SPB for a given sector, issuing a SPB Status Read Command to the device is required. Refer to the flow chart for details in Figure 3.

### 2.2 Dynamic write Protection Bits (DPB)

The Dynamic Protection features a volatile type protection to each individual sector. It can protect sectors from being unintentionally changed, and is easy to disable.

All Dynamic write Protection bit (DPB) can be modified individually. DPBs protect the unprotected sectors with their SPBs cleared. To modify the DPB status by issuing the DPB Set (programmed to “0”) or DPB Clear (erased to “1”) commands, and place each sector in the protected or unprotected state seperately. After the DPB Clear command is issued (erased to “1”), the sector may be modified depending on the SPB state of that sector.

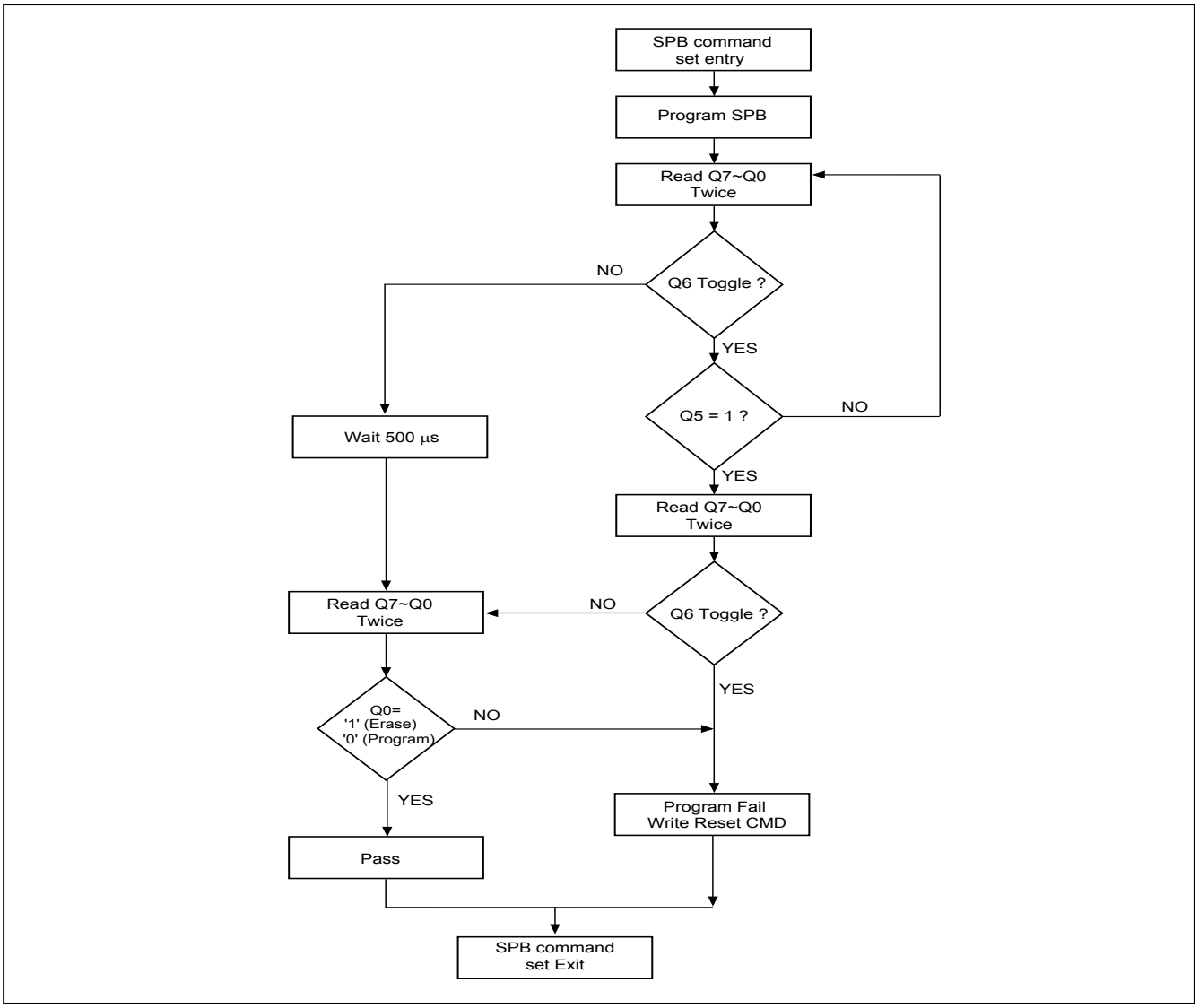
The DPBs are default to be erased to “1” when first shipped from factory.

### 2.3 Temporary Un-protect Solid write Protect Bits (USPB)

Temporary Un-protect Solid write Protect Bits are volatile. They are unique for each sector and can be individually modified. Software can temporarily unprotect write protect sectors despite of SPB's property when DPBs are cleared. While the USPB is set (to “0”), the corresponding sector's SPB property is masked.

**Notes:**
1. Upon power up, the USPBs are cleared (all “1”). The USPBs can be set (to “0”) or cleared (to “1”) as often as needed. The hardware reset will reset USPB/DPB to their default values.
2. To change the protected sector status of solid write protect bit, users don't need to clear all SPBs. The users can just implement software to set corresponding USPB to "0", in which the corresponding DPB status is cleared too. Consequently, the original solid write protect status of protected sectors can be temporarily changed.

**Figure 3. SPB Program Algorithm**




Note: SPB program/erase status polling flowchart: check Q6 toggle, when Q6 stop toggle, the read status is 00H /01H (00H for program/ 01H for erase), otherwise, the status is “fail” and “exit”.

### 3. Solid Protection Bit Lock Bit

The Solid Protection Bit Lock Bit (SPBLK) is assigned to control all SPB status. It is an unique and volatile. When SPBLK=0 (set), all SPBs are locked and can not be changed. When SPBLK=1 (cleared), all SPBs are allowed to be changed.

There is no software command sequence requested to unlock this bit, unless the device is in the password protection mode. To clear the SPB Lock Bit, just execute a hardware reset or a power-up cycle. In order to prevent modification, the SPB Lock Bit must be set (SPBLK=0) after all SPBs are set to desired status.

### 4. Password Protection Method

The security level of Password Protection Method is higher than the Solid protection mode. The 64 bit password is requested before modifying SPB lock bit status. When device is under password protection mode, the SPB lock bit is set as “0”, after a power-up cycle or Reset Command.

A correct password is required for password Unlock command to unlock the SPB lock bit. Await 2us is necessary to unlock the device after a valid password is given. After that, the SPB bits are allowed to be changed. The Password Unlock command is issued slower than 2 μs every time, to prevent hacker from trying all the 64-bit password combinations.

There are a few steps to start password protection mode:
(1). Set a 64-bit password for verification before entering the password protection mode. This verification is only allowed in password programming.
(2). Set the Password Protection Mode Lock Bit to”0” to activate the password protection mode.

Once the password protection mode lock bit is programmed, the programmed Q2 bit can not be erased any more and the device will remain permanently in password protection mode. The previous set 64-bit password can not be retrieved or programmed. All the commands to the password-protected address will also be disabled.

All the combinations of the 64-bit password can be used as a password, and programming the password does not require special address. The password is defaulted to be all “1” when shipped from the factory. Under password program command, only "0" can be programmed. In order to prevent access, the Password Mode Locking Bit must be set after the Password is programmed and verified. To set the Password Mode Lock Bit will prevent this 64-bits password to be read on the data bus. Any modification is impossible then, and the password can not be checked anymore after the Password Mode Lock Bit is set.

**Sector Protection Status Table**

| Protection Bit Status | | | Sector Status |
|---|---|---|---|
| DPB | SPB | USPB | |
| clear | clear | clear | Unprotect |
| clear | clear | set | Unprotect |
| clear | set | clear | Protect |
| clear | set | set | Unprotect |
| set | clear | clear | Protect |
| set | clear | set | Protect |
| set | set | clear | Protect |
| set | set | set | Protect |

Notes: If SPBLK is set, SPB will be unchangeable.
If SPBLK is cleared, SPB will be changeable.

## SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra OTP memory space of 128 words in length. The security sector can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device.

In factory-locked device, security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the security silicon indicator bit is set to "0".

### Factory Locked: Security Sector Programmed and Protected at the Factory

In a factory locked device, the Security Sector is permanently locked before shipping from the factory. The device will have a 16-byte (8-word) ESN in the security region. The ESN occupies addresses 000000h to 00000Fh in byte mode or 000000h to 000007h in word mode.

| Secured Silicon Sector Address Range | Standard Factory Locked | Express Flash Factory Locked | Customer Lockable |
|---|---|---|---|
| 000000h-000007h | ESN | ESN or Determined by Customer | Determined by Customer |
| 000008h-00007Fh | Unavailable | Determined by Customer | |

### Customer Lockable: Security Sector NOT Programmed or Protected at the Factory

When the security feature is not required, the security region can act as an extra memory space.

Security silicon sector can also be protected by two methods. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.

After the security silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

## TABLE 3. COMMAND DEFINITIONS

| Comm-and | | Read Mode | Reset Mode | Automatic Select | | | | | | | | Security Sector Region | | Exit Security Sector | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Silicon ID | | Device ID | | Factory Protect Verify | | Sector Protect Verify | | | | | |
| | | | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | Addr | XXX | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA |
| | Data | Data | F0 | AA | AA | AA | AA | AA | AA | AA | AA | AA | AA | AA | AA |
| 2nd Bus Cycle | Addr | | | 2AA | 555 | 2AA | 555 | 2AA | 555 | 2AA | 555 | 2AA | 555 | 2AA | 555 |
| | Data | | | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 | 55 |
| 3rd Bus Cycle | Addr | | | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA |
| | Data | | | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 88 | 88 | 90 | 90 |
| 4th Bus Cycle | Addr | | | X00 | X00 | X01 | X02 | X03 | X06 | (Sector) X02 | (Sector) X04 | | | XXX | XXX |
| | Data | | | C2h | C2h | ID1 | ID1 | 99/19(H) 89/09(L) | | 00/01 | 00/01 | | | 00 | 00 |
| 5th Bus Cycle | Addr | | | | | X0E | X1C | | | | | | | | |
| | Data | | | | | ID2 | ID2 | | | | | | | | |
| 6th Bus Cycle | Addr | | | | | X0F | X1E | | | | | | | | |
| | Data | | | | | ID3 | ID3 | | | | | | | | |

| Comm-and | | Program | | Write to Buffer Program | | Write to Buffer Program Abort Reset | | Write to Buffer Program confirm | | Chip Erase | | Sector Erase | | CFI Read | | Program/ Erase Suspend | | Program/ Erase Resume | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | 555 | AAA | 555 | AAA | 555 | AAA | SA | SA | 555 | AAA | 555 | AAA | 55 | AA | xxx | xxx | xxx | xxx |
| | Data | AA | AA | AA | AA | AA | AA | 29 | 29 | AA | AA | AA | AA | 98 | 98 | B0 | B0 | 30 | 30 |
| 2nd Bus Cycle | Addr | 2AA | 555 | 2AA | 555 | 2AA | 555 | | | 2AA | 555 | 2AA | 555 | | | | | | |
| | Data | 55 | 55 | 55 | 55 | 55 | 55 | | | 55 | 55 | 55 | 55 | | | | | | |
| 3rd Bus Cycle | Addr | 555 | AAA | SA | SA | 555 | AAA | | | 555 | AAA | 555 | AAA | | | | | | |
| | Data | A0 | A0 | 25 | 25 | F0 | F0 | | | 80 | 80 | 80 | 80 | | | | | | |
| 4th Bus Cycle | Addr | Addr | Addr | SA | SA | | | | | 555 | AAA | 555 | AAA | | | | | | |
| | Data | Data | Data | N-1 | N-1 | | | | | AA | AA | AA | AA | | | | | | |
| 5th Bus Cycle | Addr | | | WA | WA | | | | | 2AA | 555 | 2AA | 555 | | | | | | |
| | Data | | | WD | WD | | | | | 55 | 55 | 55 | 55 | | | | | | |
| 6th Bus Cycle | Addr | | | WBL | WBL | | | | | 555 | AAA | Sec-tor | Sec-tor | | | | | | |
| | Data | | | WD | WD | | | | | 10 | 10 | 30 | 30 | | | | | | |

WA= Write Address
WD= Write Data
SA= Sector Address
N-1= Word Count
WBL= Write Buffer Location
PWD= Password
PWDn=Password word 0, word 1, word n
ID1/ID2/ID3: Refer to *Table 2-2* for detail ID.

| Command | | Deep Power Down | | | | Password Protection | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Enter | | Exit | | Password Command Set Entry | | Password Program | | Password Read | | Password Unlock | | Password Command Set Exit | |
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | 555 | AAA | XXX | XXX | 555 | AAA | XXX | XXX | X00 | X00 | 00 | 00 | XXX | XXX |
| | Data | AA | AA | AB | AB | AA | AA | A0 | A0 | PWD0 | PWD0 | 25 | 25 | 90 | 90 |
| 2nd Bus Cycle | Addr | 2AA | 555 | | | 2AA | 555 | PWA | PWA | X01 | X01 | 00 | 00 | XXX | XXX |
| | Data | 55 | 55 | | | 55 | 55 | PWD | PWD | PWD1 | PWD1 | 03 | 03 | 00 | 00 |
| 3rd Bus Cycle | Addr | XXX | XXX | | | 555 | AAA | | | X02 | X02 | X00 | X00 | | |
| | Data | B9 | B9 | | | 60 | 60 | | | PWD2 | PWD2 | PWD0 | PWD0 | | |
| 4th Bus Cycle | Addr | | | | | | | | | X03 | X03 | X01 | X01 | | |
| | Data | | | | | | | | | PWD3 | PWD3 | PWD1 | PWD1 | | |
| 5th Bus Cycle | Addr | | | | | | | | | | X04 | X02 | X02 | | |
| | Data | | | | | | | | | | PWD4 | PWD2 | PWD2 | | |
| 6th Bus Cycle | Addr | | | | | | | | | | X05 | X03 | X03 | | |
| | Data | | | | | | | | | | PWD5 | PWD3 | PWD3 | | |
| 7th Bus Cycle | Addr | | | | | | | | | | X06 | 00 | X04 | | |
| | Data | | | | | | | | | | PWD6 | 29 | PWD4 | | |
| 8th Bus Cycle | Addr | | | | | | | | | | X07 | | X05 | | |
| | Data | | | | | | | | | | PWD7 | | PWD5 | | |
| 9th Bus Cycle | Addr | | | | | | | | | | | | X06 | | |
| | Data | | | | | | | | | | | | PWD6 | | |
| 10th Bus Cycle | Addr | | | | | | | | | | | | X07 | | |
| | Data | | | | | | | | | | | | PWD7 | | |
| 11th Bus Cycle | Addr | | | | | | | | | | | | 00 | | |
| | Data | | | | | | | | | | | | 29 | | |

| Command | | Lock Register | | | | | | | | Global Non-Volatile | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Lock register Command Set Entry | | Program | | Read | | Lock register Command Set Exit | | SPB Command Set Entry | | SPB Program | | All SPB Erase | | SPB Status Read | |
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | 555 | AAA | XXX | XXX | XXX | XXX | XXX | XXX | 555 | AAA | XXX | XXX | XXX | XXX | SA | SA |
| | Data | AA | AA | A0 | A0 | DATA | DATA | 90 | 90 | AA | AA | A0 | A0 | 80 | 80 | 00/01 | 00/01 |
| 2nd Bus Cycle | Addr | 2AA | 555 | XXX | XXX | | | XXX | XXX | 2AA | 555 | SA | SA | 00 | 00 | | |
| | Data | 55 | 55 | Data | Data | | | 00 | 00 | 55 | 55 | 00 | 00 | 30 | 30 | | |
| 3rd Bus Cycle | Addr | 555 | AAA | | | | | | | 555 | AAA | | | | | | |
| | Data | 40 | 40 | | | | | | | C0 | C0 | | | | | | |
| 4th Bus Cycle | Addr | | | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | | | |
| 5th Bus Cycle | Addr | | | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | | | |

| Command | | Global Non-Volatile | | Global Volatile Freeze | | | | | | | | Volatile | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SPB Command Set Exit | | SPB Lock Command Set Entry | | SPB Lock Set | | SPB Lock Status Read | | SPB Lock Command Set Exit | | DPB Command Set Entry | | DPB Set | | DPB Clear | |
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | XXX | XXX | 555 | AAA | XXX | XXX | XXX | XXX | XXX | XXX | 555 | AAA | XXX | XXX | XXX | XXX |
| | Data | 90 | 90 | AA | AA | A0 | A0 | 00/01 | 00/01 | 90 | 90 | AA | AA | A0 | A0 | A0 | A0 |
| 2nd Bus Cycle | Addr | XXX | XXX | 2AA | 555 | XXX | XXX | | | XXX | XXX | 2AA | 555 | SA | SA | SA | SA |
| | Data | 00 | 00 | 55 | 55 | 00 | 00 | | | 00 | 00 | 55 | 55 | 00 | 00 | 01 | 01 |
| 3rd Bus Cycle | Addr | | | 555 | AAA | | | | | | | 555 | AAA | | | | |
| | Data | | | 50 | 50 | | | | | | | E0 | E0 | | | | |
| 4th Bus Cycle | Addr | | | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | | | |
| 5th Bus Cycle | Addr | | | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | | | |

| Command | | Volatile | | | |
|---|---|---|---|---|---|
| | | DPB Status Read | | DPB Command Set Exit | |
| | | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | SA | SA | XXX | XXX |
| | Data | 00/01 | 00/01 | 90 | 90 |
| 2nd Bus Cycle | Addr | | | XXX | XXX |
| | Data | | | 00 | 00 |
| 3rd Bus Cycle | Addr | | | | |
| | Data | | | | |
| 4th Bus Cycle | Addr | | | | |
| | Data | | | | |
| 5th Bus Cycle | Addr | | | | |
| | Data | | | | |

**Notes:**

* It is not recommended to adopt any other code not in the command definition table which will potentially enter the hidden mode.
* For the SPB Lock and DPB Status Read "00" means lock (protect), "01" means unlock (unprotect).

## COMMON FLASH MEMORY INTERFACE (CFI) MODE

### QUERY COMMAND AND COMMAND FLASH MEMORY INTERFACE (CFI) MODE

The device features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/"AAh" (depending on Word/Byte mode), the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in *Table 4*.

Once user enters CFI query mode, user can issue reset command to exit CFI mode and return to read array mode. The unused CFI area is reserved by Macronix.

**Table 4-1. CFI mode: Identification Data Values** (Note 1)
(All values in these tables are in hexadecimal)

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Query-unique ASCII string "QRY" | 10 | 20 | 0051 |
| | 11 | 22 | 0052 |
| | 12 | 24 | 0059 |
| Primary vendor command set and control interface ID code | 13 | 26 | 0002 |
| | 14 | 28 | 0000 |
| Address for primary algorithm extended query table | 15 | 2A | 0040 |
| | 16 | 2C | 0000 |
| Alternate vendor command set and control interface ID code | 17 | 2E | 0000 |
| | 18 | 30 | 0000 |
| Address for alternate algorithm extended query table | 19 | 32 | 0000 |
| | 1A | 34 | 0000 |

Note 1. Query data are always presented on the lowest data output Q7~Q0 only, Q8~Q15 are "0".

**Table 4-2. CFI mode: System Interface Data Values**

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Vcc supply minimum program/erase voltage | 1B | 36 | 0027 |
| Vcc supply maximum program/erase voltage | 1C | 38 | 0036 |
| VPP supply minimum program/erase voltage | 1D | 3A | 0000 |
| VPP supply maximum program/erase voltage | 1E | 3C | 0000 |
| Typical timeout per single word/byte write, $2^n$ us | 1F | 3E | 0003 |
| Typical timeout for maximum-size buffer write, $2^n$ us (00h, not support) | 20 | 40 | 0006 |
| Typical timeout per individual block erase, $2^n$ ms | 21 | 42 | 0009 |
| Typical timeout for full chip erase, $2^n$ ms (00h, not support) | 22 | 44 | 0013 |
| Maximum timeout for word/byte write, $2^n$ times typical | 23 | 46 | 0003 |
| Maximum timeout for buffer write, $2^n$ times typical | 24 | 48 | 0005 |
| Maximum timeout per individual block erase, $2^n$ times typical | 25 | 4A | 0003 |
| Maximum timeout for chip erase, $2^n$ times typical (00h, not support) | 26 | 4C | 0002 |

**Table 4-3. CFI mode: Device Geometry Data Values**

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Device size = $2^n$ in number of bytes | 27 | 4E | 0018 |
| Flash device interface description (02=asynchronous x8/x16) | 28 | 50 | 0002 |
| | 29 | 52 | 0000 |
| Maximum number of bytes in buffer write = $2^n$ (00h, not support) | 2A | 54 | 0006 |
| | 2B | 56 | 0000 |
| Number of erase regions within device (01h:uniform, 02h:boot) | 2C | 58 | 0001 |
| Index for Erase Bank Area 1:<br>[2E,2D] = # of same-size sectors in region 1-1<br>[30, 2F] = sector size in multiples of 256K-bytes | 2D | 5A | 007F |
| | 2E | 5C | 0000 |
| | 2F | 5E | 0000 |
| | 30 | 60 | 0002 |
| Index for Erase Bank Area 2 | 31 | 62 | 0000 |
| | 32 | 64 | 0000 |
| | 33 | 66 | 0000 |
| | 34 | 68 | 0000 |
| Index for Erase Bank Area 3 | 35 | 6A | 0000 |
| | 36 | 6C | 0000 |
| | 37 | 6E | 0000 |
| | 38 | 70 | 0000 |
| Index for Erase Bank Area 4 | 39 | 72 | 0000 |
| | 3A | 74 | 0000 |
| | 3B | 76 | 0000 |
| | 3C | 78 | 0000 |

**Table 4-4. CFI mode: Primary Vendor-Specific Extended Query Data Values**

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Query - Primary extended table, unique ASCII string, PRI | 40 | 80 | 0050 |
| | 41 | 82 | 0052 |
| | 42 | 84 | 0049 |
| Major version number, ASCII | 43 | 86 | 0031 |
| Minor version number, ASCII | 44 | 88 | 0033 |
| Unlock recognizes address (0= recognize, 1= don't recognize) | 45 | 8A | 0014 |
| Erase suspend (2= to both read and program) | 46 | 8C | 0002 |
| Sector protect (N= # of sectors/group) | 47 | 8E | 0001 |
| Temporary sector unprotect (1=supported) | 48 | 90 | 0000 |
| Sector protect/Chip unprotect scheme | 49 | 92 | 0008 |
| Simultaneous R/W operation (0=not supported) | 4A | 94 | 0000 |
| Burst mode (0=not supported) | 4B | 96 | 0000 |
| Page mode (0=not supported, 01 = 4 word page, 02 = 8 word page) | 4C | 98 | 0002 |
| Minimum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV | 4D | 9A | 0095 |
| Maximum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV | 4E | 9C | 00A5 |
| WP# Protection<br>04=Uniform sectors bottom WP# protect<br>05=Uniform sectors top WP# protect | 4F | 9E | 0004/<br>0005 |
| Program Suspend (0=not supported, 1=supported) | 50 | A0 | 0001 |

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM STRESS RATINGS

| | | |
|---|---|---|
| Storage Temperature | | -65°C to +150°C |
| Voltage Range | VCC | -0.5V to +4.0V |
| | VI/O | -0.5V to +4.0V |
| | A9 , WP#/ACC | -0.5V to +10.5V |
| | The other pins. | -0.5V to Vcc +0.5V |
| Output Short Circuit Current (less than one second) | | 200 mA |

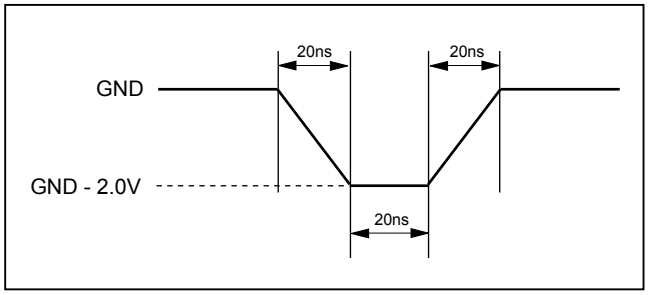
### OPERATING TEMPERATURE AND VOLTAGE

| | | |
|---|---|---|
| **Industrial (I) Grade** | Surrounding Temperature ($T_A$) | -40°C to +85°C |
| **VCC Supply Voltages** | Full VCC range | +2.7V to 3.6V |
| | Regulated VCC range | +3.0V to 3.6V |
| | VI/O range | 1.65V to VCC |

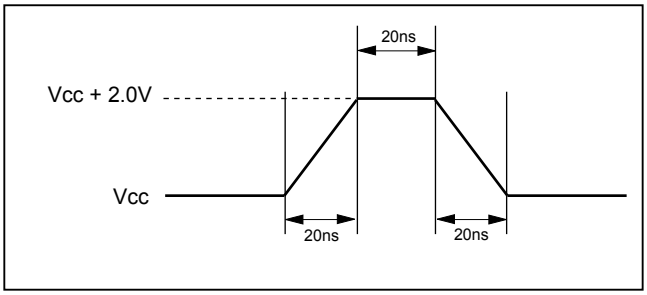
**NOTICE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot GND to -2.0V and Vcc to +2.0V for periods up to 20ns, see Figures below.

**Maximum Negative Overshoot Waveform**




**Maximum Positive Overshoot Waveform**

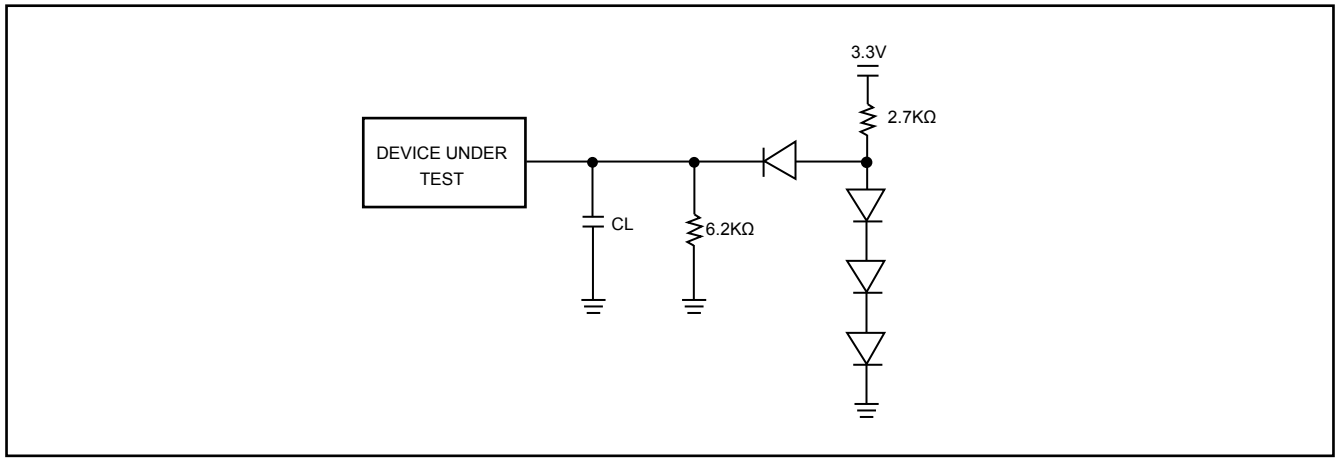


## DC CHARACTERISTICS

| Symbol | Description | Min. | Typ. | Max. | Remark |
|---|---|---|---|---|---|
| Iilk | Input Leak | | | ±2.0uA | |
| Iilk9 | A9 Leak | | | 35uA | A9=10.5V |
| Iolk | Output Leak | | | ±1.0uA | |
| Icr1 | Read Current | | 5mA | 15mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=1MHz, Byte Mode |
| | | | 10mA | 20mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=5MHz, Byte Mode |
| | | | 15mA | 30mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=10MHz |
| Icr2 | VCC Page Read Current | | 1.5mA | 5mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=10MHz |
| | | | 3mA | 10mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=33MHz |
| Iio | VI/O non-active current | | 0.2mA | 10mA | |
| Icw | Write Current | | 14mA | 30mA | CE#=Vil, OE#=Vih |
| Isb | Standby Current | | 20uA | 50uA | VCC=VCCmax, other pin disable |
| Isbr | Reset Current | | 20uA | 50uA | VCC=VCCmax, RESET# enable, other pin disable |
| Isbs | Sleep Mode Current *1 | | 20uA | 50uA | |
| Idpd | Vcc deep power down current | | 1uA | 10uA | |
| Icp1 | Accelerated Pgm Current, WP#/ACC pin (Word/Byte) | | 1mA | 3mA | CE#=Vil, OE#=Vih |
| Icp2 | Accelerated Pgm Current, VCC pin, (Word/Byte) | | 7mA | 14mA | CE#=Vil, OE#=Vih |
| Vil | Input Low Voltage | -0.1V | | 0.3xVI/O | |
| Vih | Input High Voltage | 0.7xVI/O | | VI/O+0.3V | |
| Vhv | Very High Voltage for Auto Select/ Accelerated Program | 9.5V | | 10.5V | |
| Vol | Output Low Voltage | | | 0.45V | Iol=100uA |
| Voh | Ouput High Voltage | 0.85xVI/O | | | Ioh=-100uA |
| Vlko | Low VCC Lock-out voltage *2 | 2.1V | | 2.4V | |

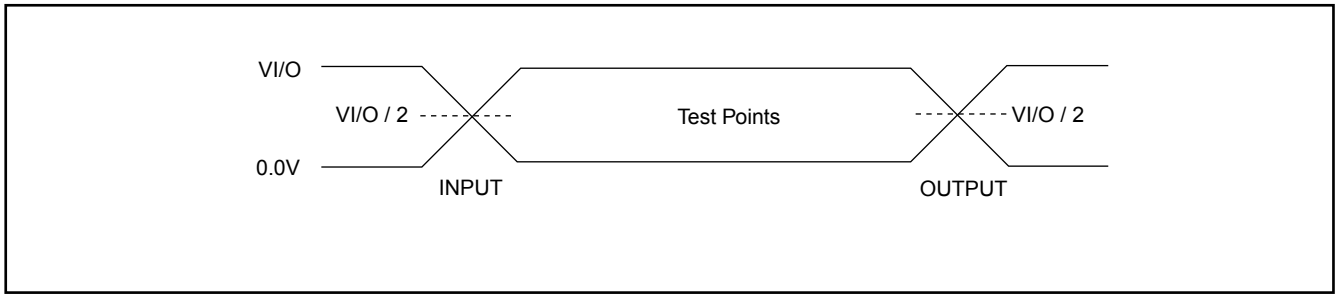
**Note:**
1. Sleep mode enables the lower power when address remain stable for taa+30ns.
2. Not 100% tested.

## SWITCHING TEST CIRCUITS




Test Condition
Output Load Capacitance, CL : 1TTL gate, 30pF
Rise/Fall Times : 5ns
Input Pulse levels :0.0 ~ VI/O
In/Out reference levels :0.5VI/O

## SWITCHING TEST WAVEFORMS



## AC CHARACTERISTICS

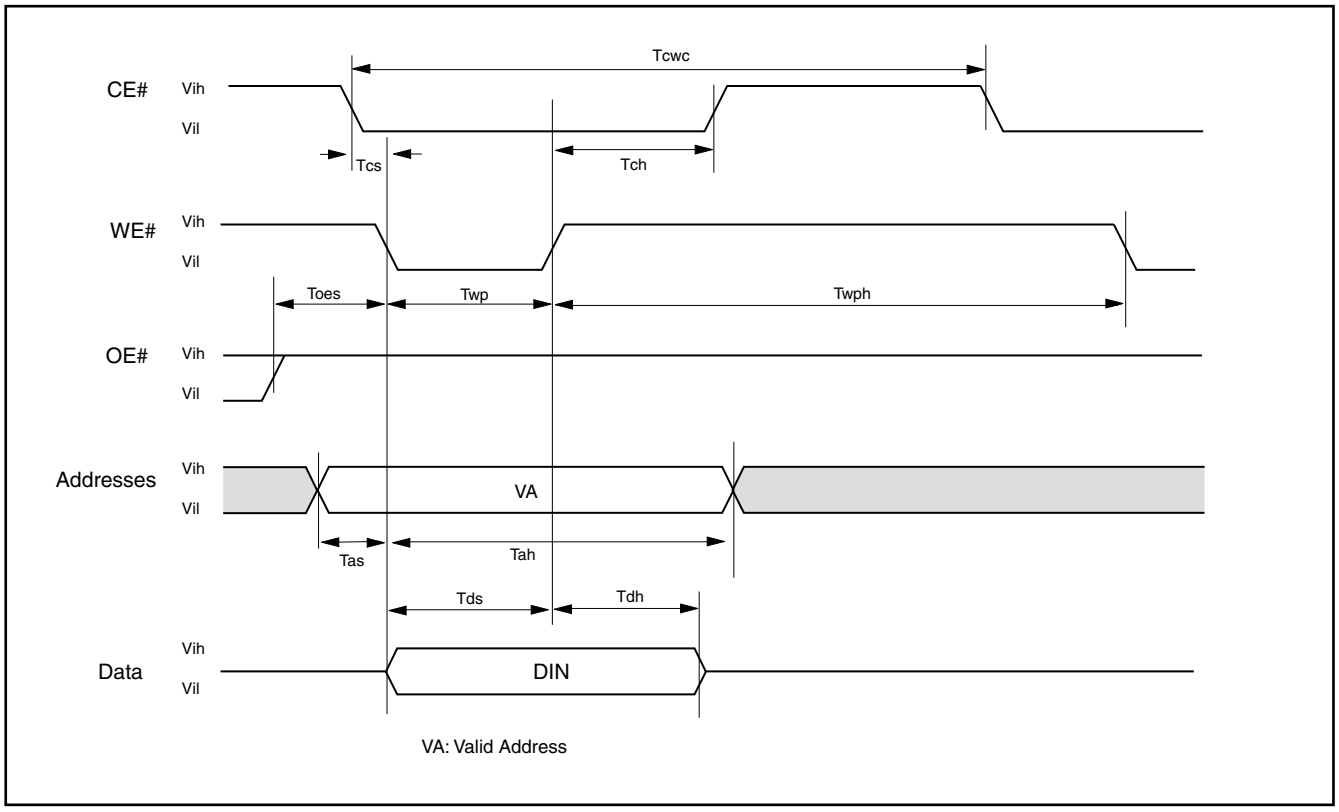
| Symbol | Description | | 29GL128F (VCC=2.7V~3.6V) | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Taa | Valid data output after address | VI/O=VCC | | | 70/90 | ns |
| | | VI/O=1.65 toVCC | | | 90/110 | ns |
| Tpa | Page access time | VI/O=VCC | | | 25 | ns |
| | | VI/O=1.65 toVCC | | | 30 | ns |
| Tce | Valid data output after CE# low | VI/O=VCC | | | 70/90 | ns |
| | | VI/O=1.65 toVCC | | | 90/110 | ns |
| Toe | Valid data output after OE# low | VI/O=VCC | | | 25 | ns |
| | | VI/O=1.65 toVCC | | | 30 | ns |
| Tdf | Data output floating after OE# high or CE# high | | | | 20 | ns |
| Tsrw | Latency between read and write operation (Note) | | 35 | | | ns |
| Toh | Output hold time from the earliest rising edge of address,CE#, OE# | | 0 | | | ns |
| Trc | Read period time | VI/O=VCC | 70/90 | | | ns |
| | | VI/O=1.65 toVCC | 90/110 | | | ns |
| Twc | Write period time | VI/O=VCC | 70/90 | | | ns |
| | | VI/O=1.65 toVCC | 90/110 | | | ns |
| Tcwc | Command write period time | VI/O=VCC | 70/90 | | | ns |
| | | VI/O=1.65 toVCC | 90/110 | | | ns |
| Tas | Address setup time | | 0 | | | ns |
| Taso | Address setup time to OE# low during toggle bit polling | | 15 | | | ns |
| Tah | Address hold time | | 45 | | | ns |
| Taht | Address hold time from CE# or OE# high during toggle bit polling | | 0 | | | ns |
| Tds | Data setup time | | 30 | | | ns |
| Tdh | Data hold time | | 0 | | | ns |
| Tvcs | Vcc setup time | | 500 | | | us |
| Tcs | Chip enable Setup time | | 0 | | | ns |
| Tch | Chip enable hold time | | 0 | | | ns |
| Toes | Output enable setup time | | 0 | | | ns |
| Toeh | Output enable hold time | Read | 0 | | | ns |
| | | Toggle & Data# Polling | 10 | | | ns |
| Tws | WE# setup time | | 0 | | | ns |
| Twh | WE# hold time | | 0 | | | ns |
| Tcepw | CE# pulse width | | 35 | | | ns |
| Tcepwh | CE# pulse width high | | 30 | | | ns |
| Twp | WE# pulse width | | 35 | | | ns |
| Twph | WE# pulse width high | | 30 | | | ns |
| Tbusy | Program/Erase active time by RY/BY# | VI/O=VCC | | | 70/90 | ns |
| | | VI/O=1.65 toVCC | | | 90/110 | ns |
| Tghwl | Read recover time before write | | 0 | | | ns |
| Tghel | Read recover time before write | | 0 | | | ns |

| Symbol | Description | | 29GL128F (VCC=2.7V~3.6V) | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Twhwh1 | Program operation | Byte | | 10 | | us |
| Twhwh1 | Program operation | Word | | 10 | | us |
| Twhwh1 | Acc program operation (Word/Byte) | | | 10 | | us |
| Twhwh2 | Sector erase operation | | | 0.5 | 3.5 | sec |
| Tbal | Sector add hold time | | | | 50 | us |
| Trdp | Release from deep power down mode | | | | 200 | us |

**Note :** Not 100% tested.

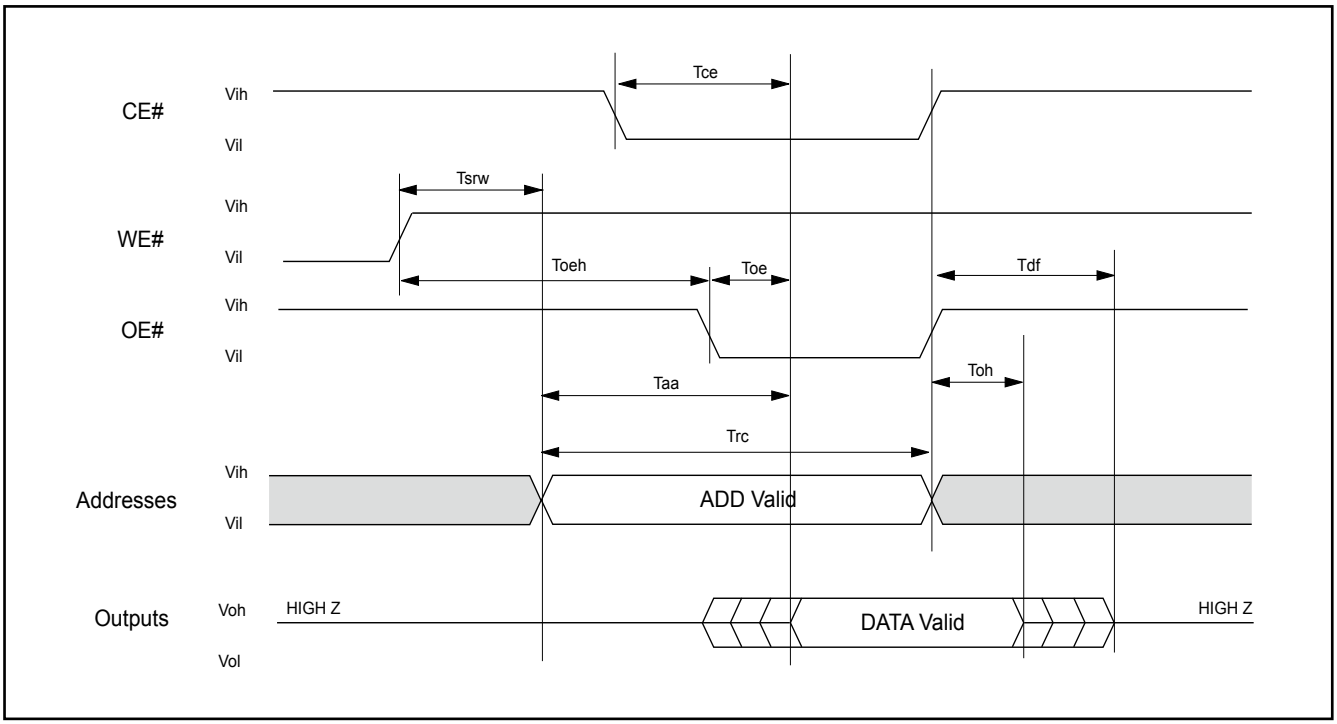
## WRITE OPERATION

### Figure 4. COMMAND WRITE OPERATION



## READ/RESET OPERATION

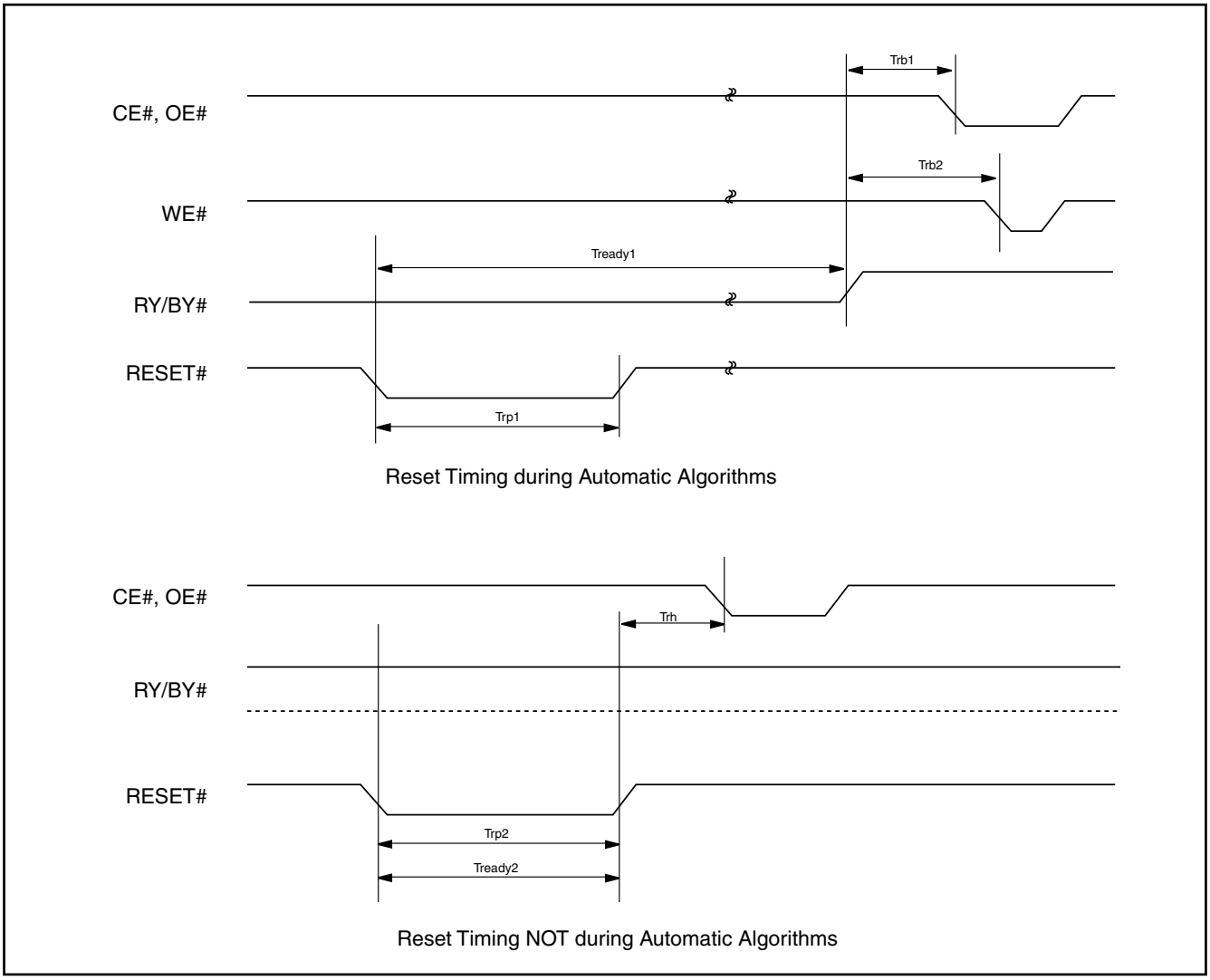
### Figure 5. READ TIMING WAVEFORMS



## AC CHARACTERISTICS

| Item | Description | Setup | Speed | Unit |
|---|---|---|---|---|
| Trp1 | RESET# Pulse Width (During Automatic Algorithms) | MIN | 10 | us |
| Trp2 | RESET# Pulse Width (NOT During Automatic Algorithms) | MIN | 500 | ns |
| Trh | RESET# High Time Before Read | MIN | 200 | ns |
| Trb1 | RY/BY# Recovery Time (to CE#, OE# go low) | MIN | 0 | ns |
| Trb2 | RY/BY# Recovery Time (to WE# go low) | MIN | 50 | ns |
| Tready1 | RESET# PIN Low (During Automatic Algorithms) to Read or Write | MAX | 20 | us |
| Tready2 | RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write | MAX | 500 | ns |

**Figure 6. RESET# TIMING WAVEFORM**



## ERASE/PROGRAM OPERATION

### Figure 7. AUTOMATIC CHIP ERASE TIMING WAVEFORM

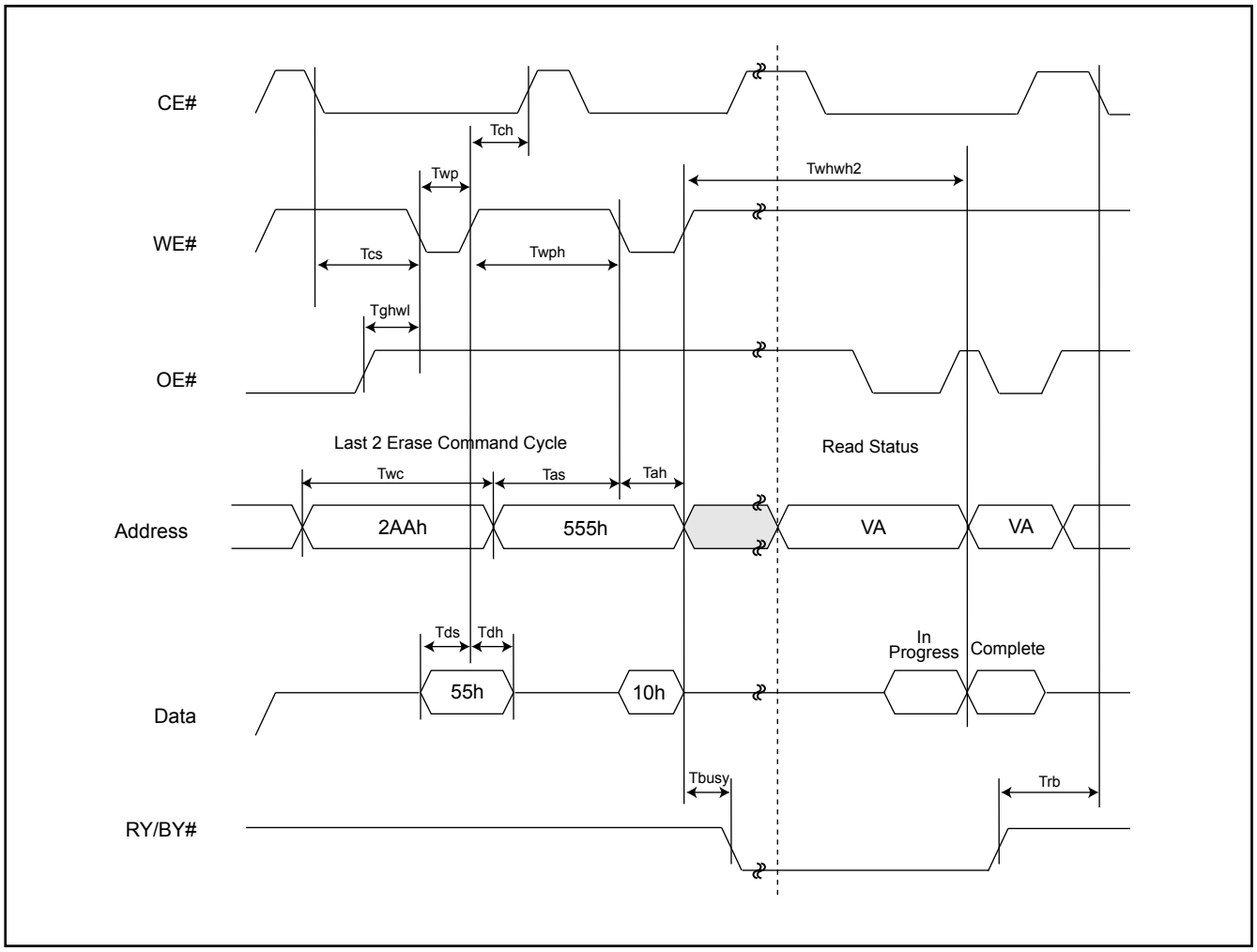


**Figure 8. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART**

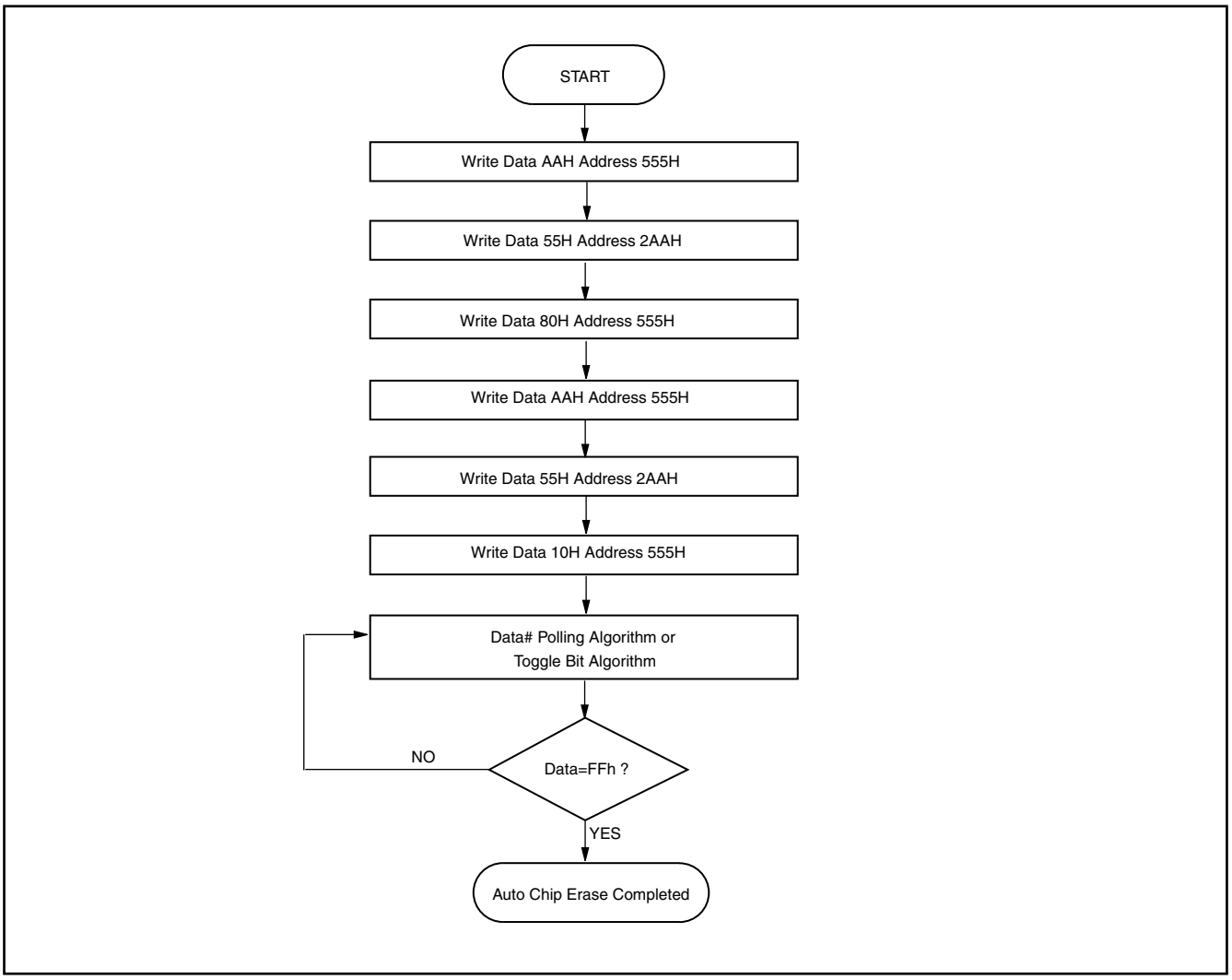


**Figure 9. AUTOMATIC SECTOR ERASE TIMING WAVEFORM**

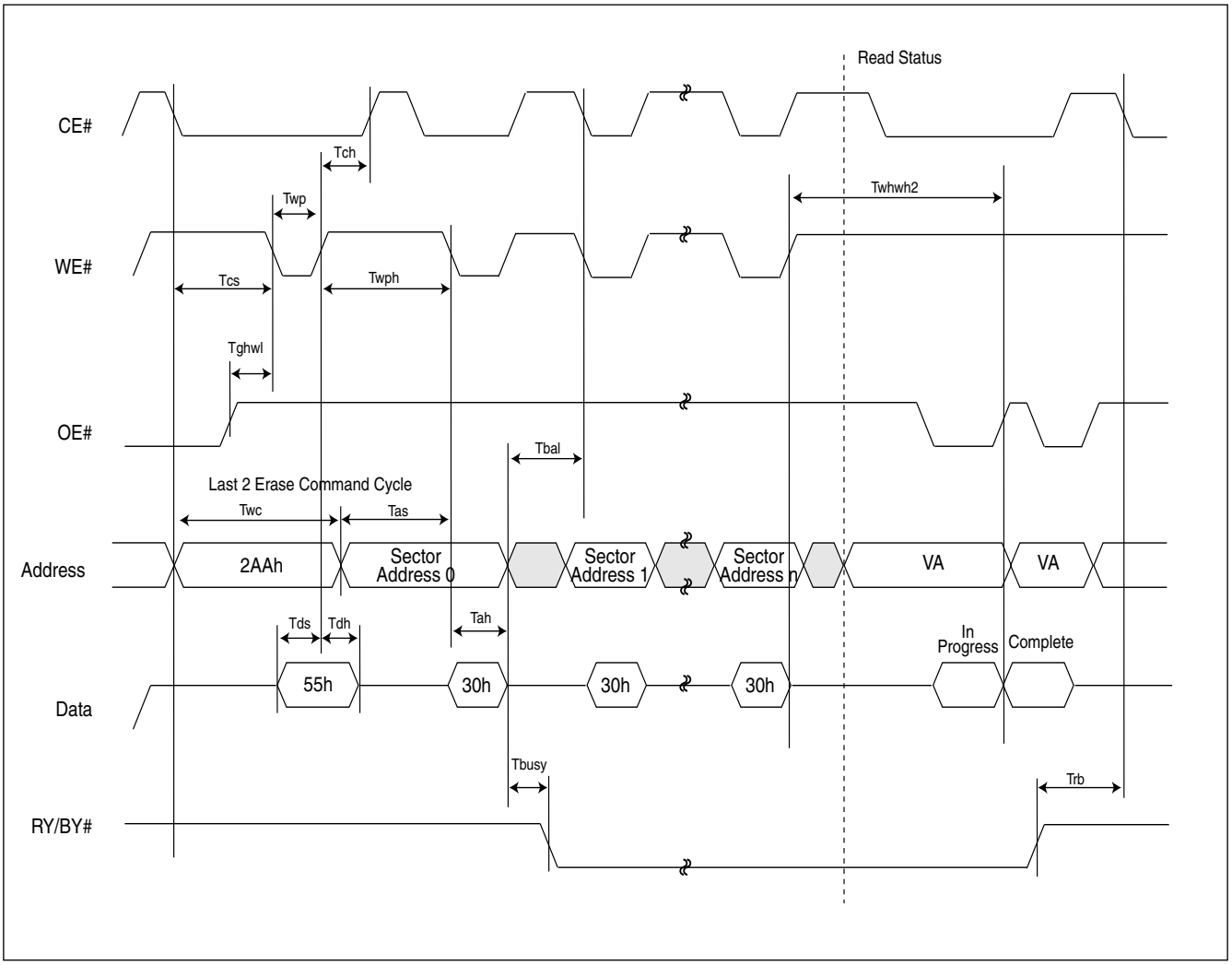


**Figure 10. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART**

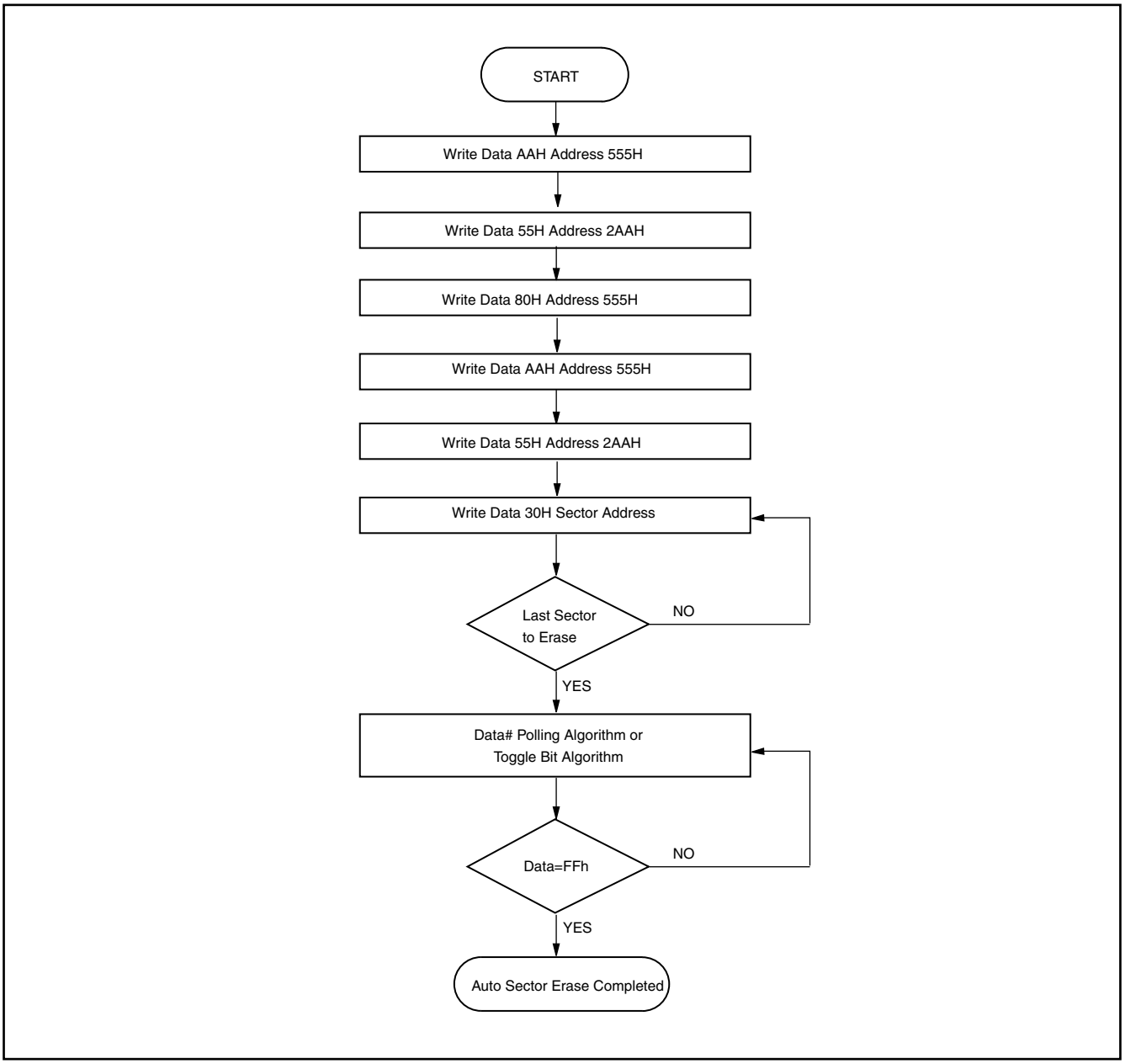


**Figure 11. ERASE SUSPEND/RESUME FLOWCHART**

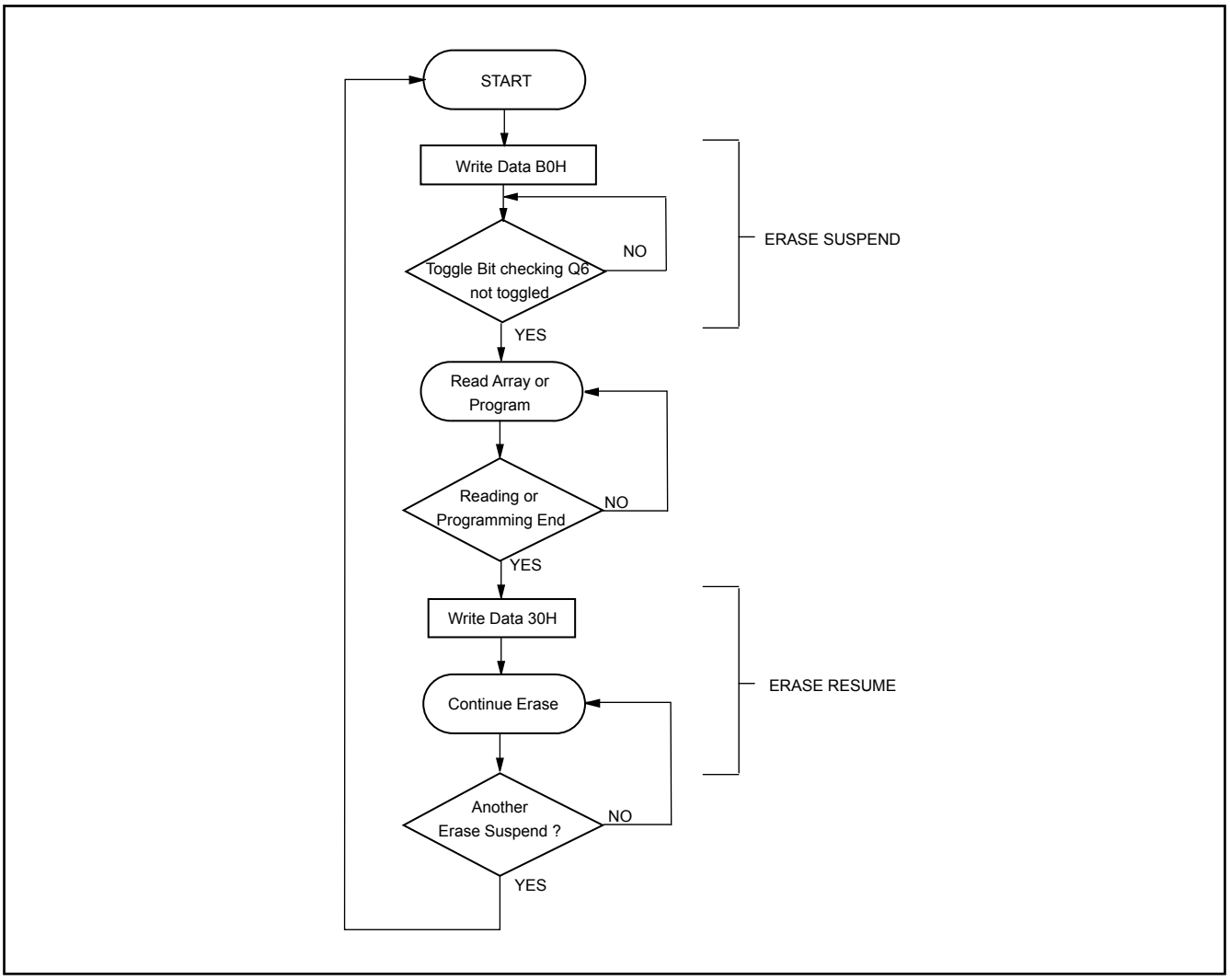


**Figure 12. AUTOMATIC PROGRAM TIMING WAVEFORMS**

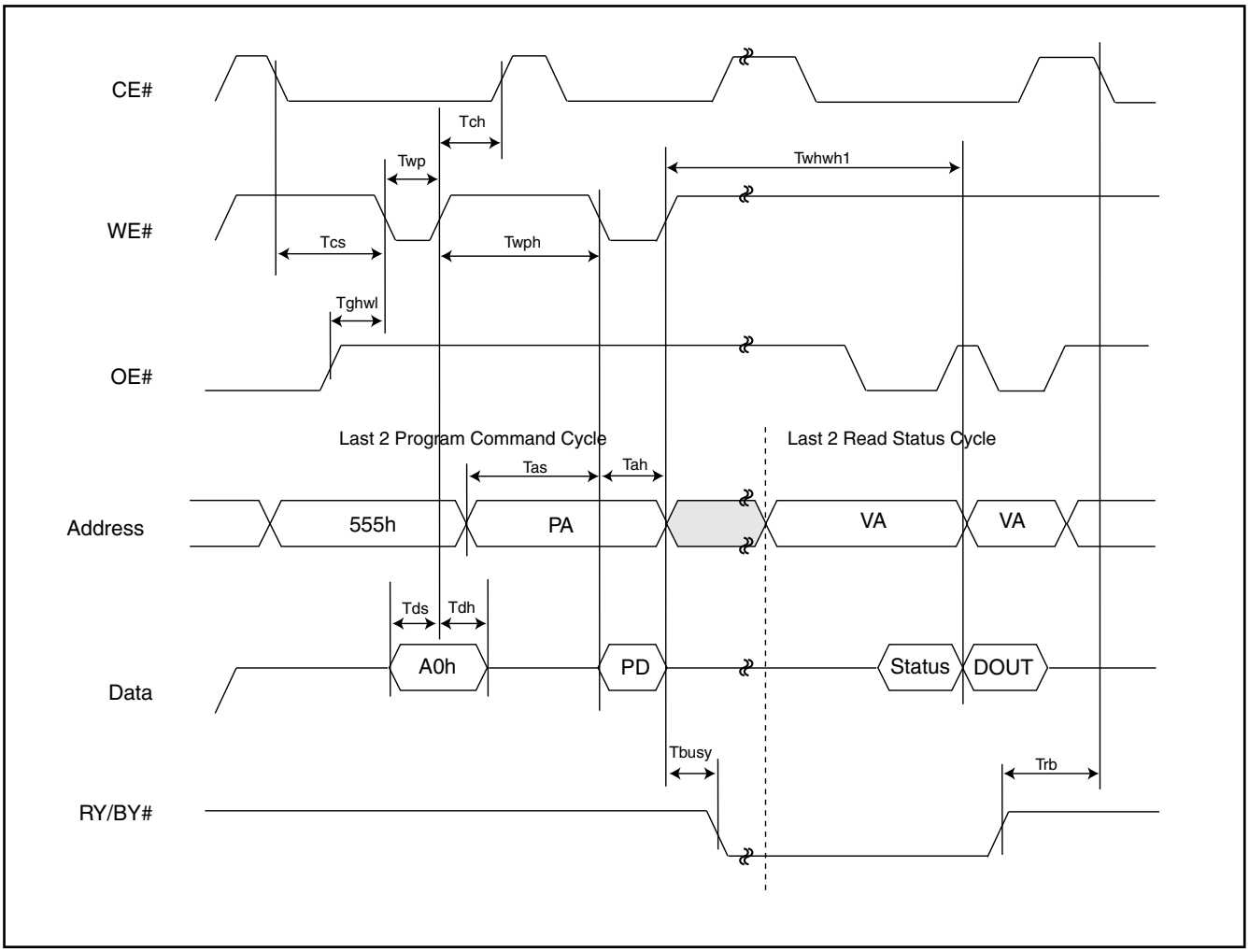



**Figure 13. ACCELERATED PROGRAM TIMING DIAGRAM**

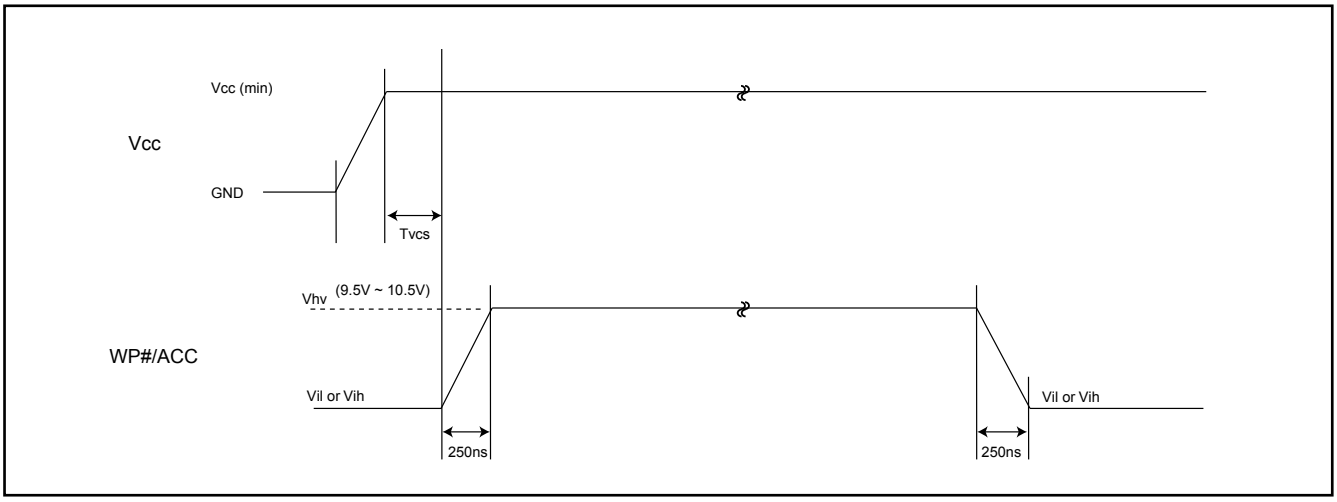


**Figure 14. CE# CONTROLLED WRITE TIMING WAVEFORM**

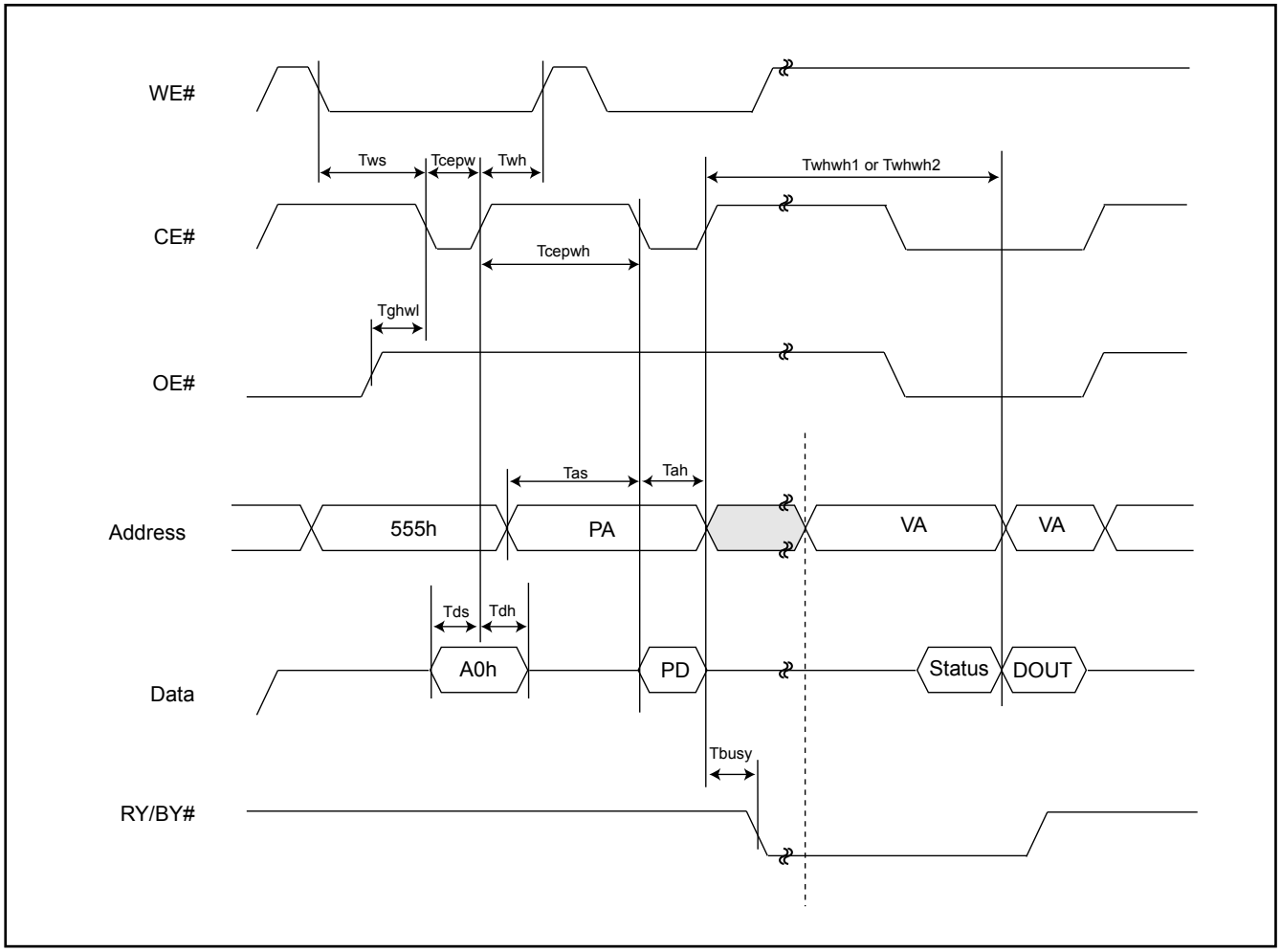


**Figure 15. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART**

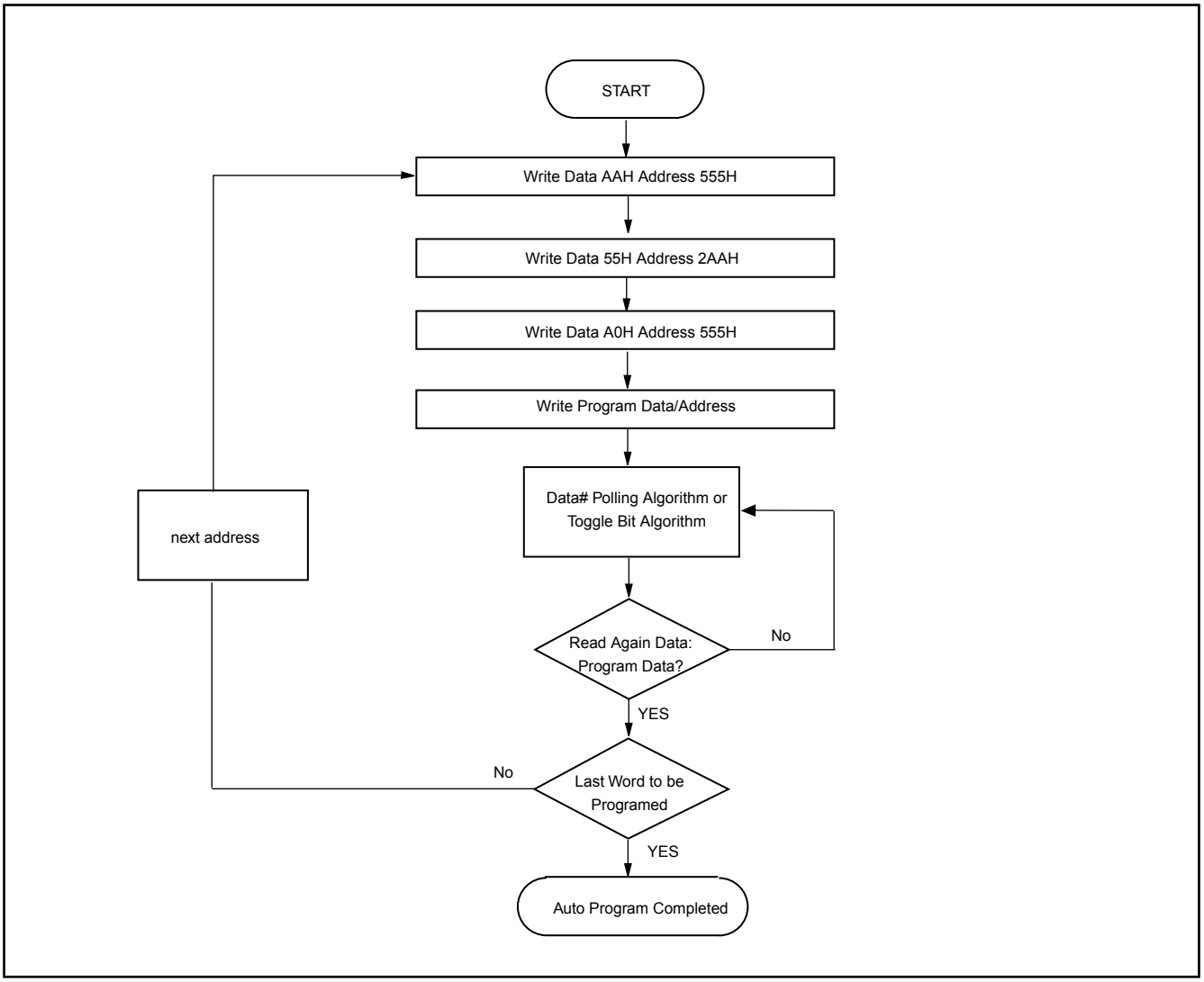
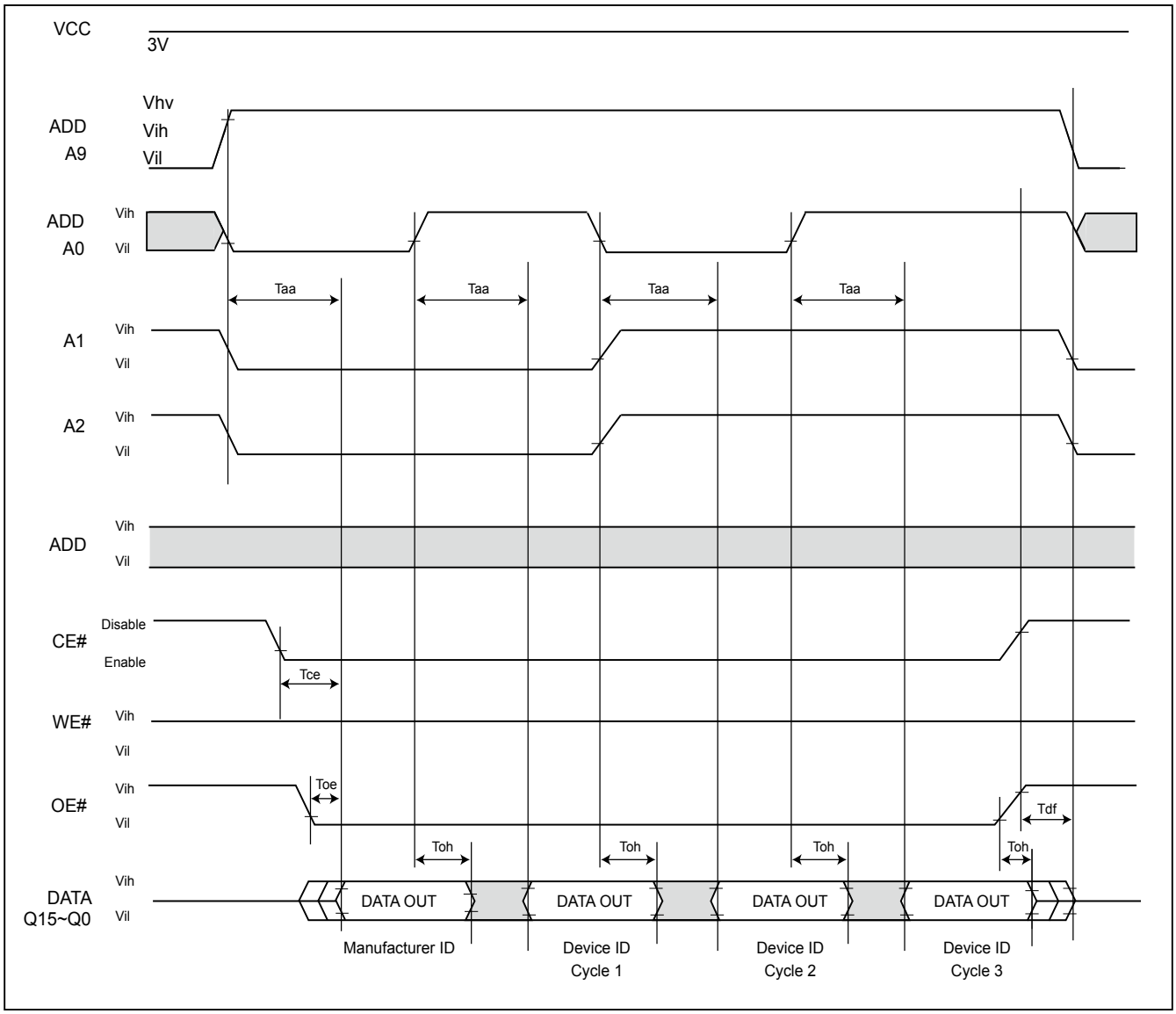


**Figure 16. SILICON ID READ TIMING WAVEFORM**



## WRITE OPERATION STATUS

**Figure 17. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)**

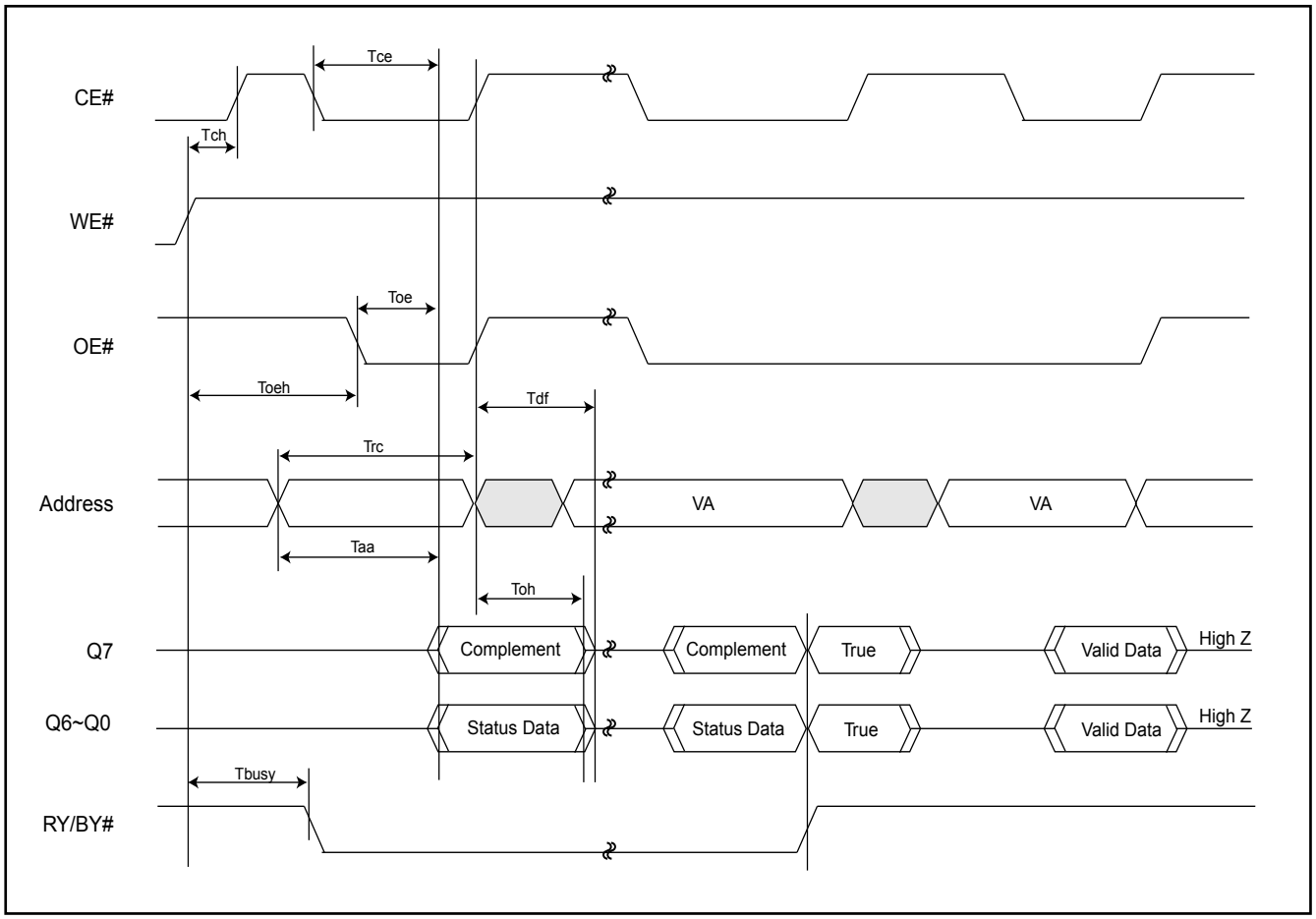
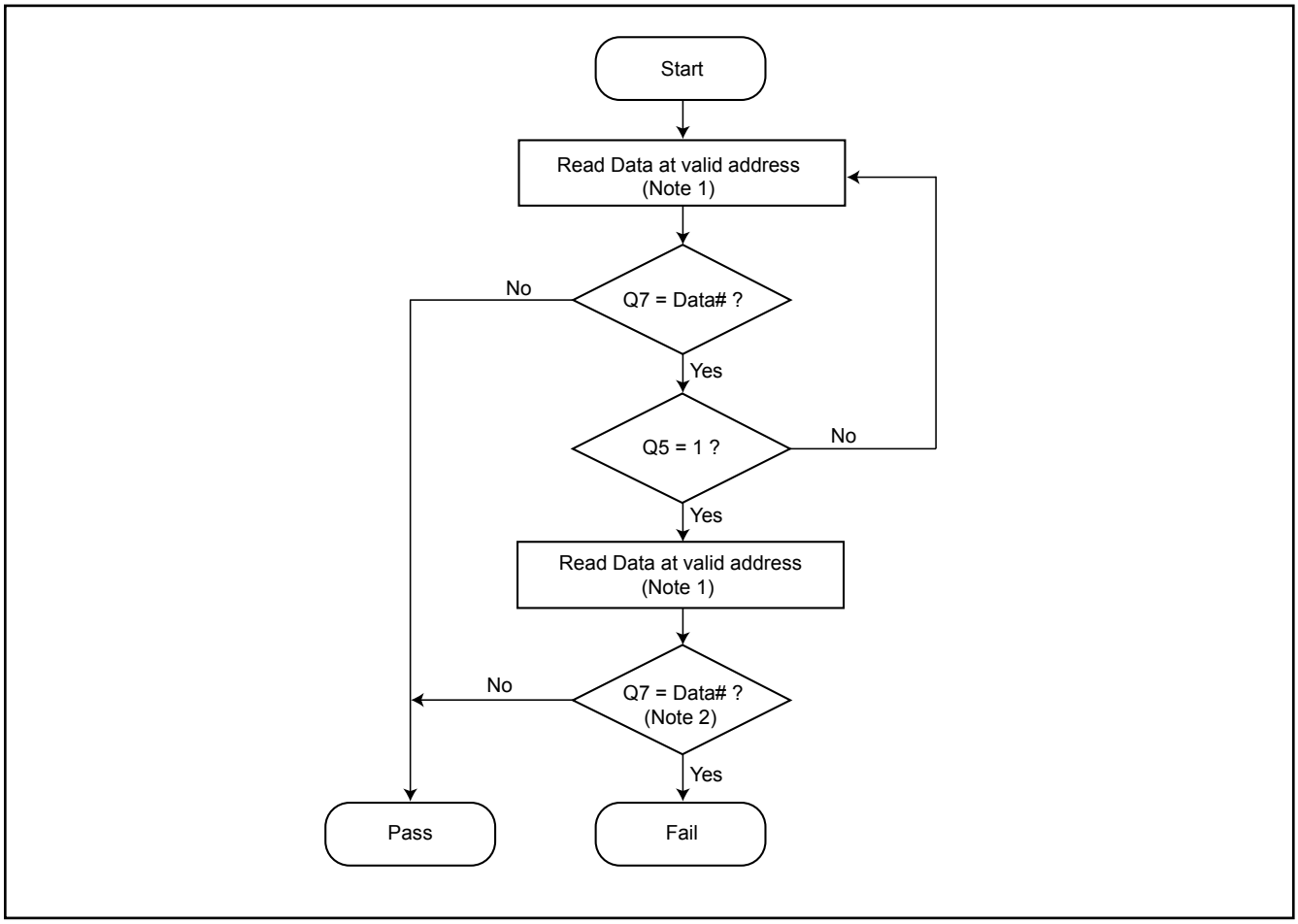
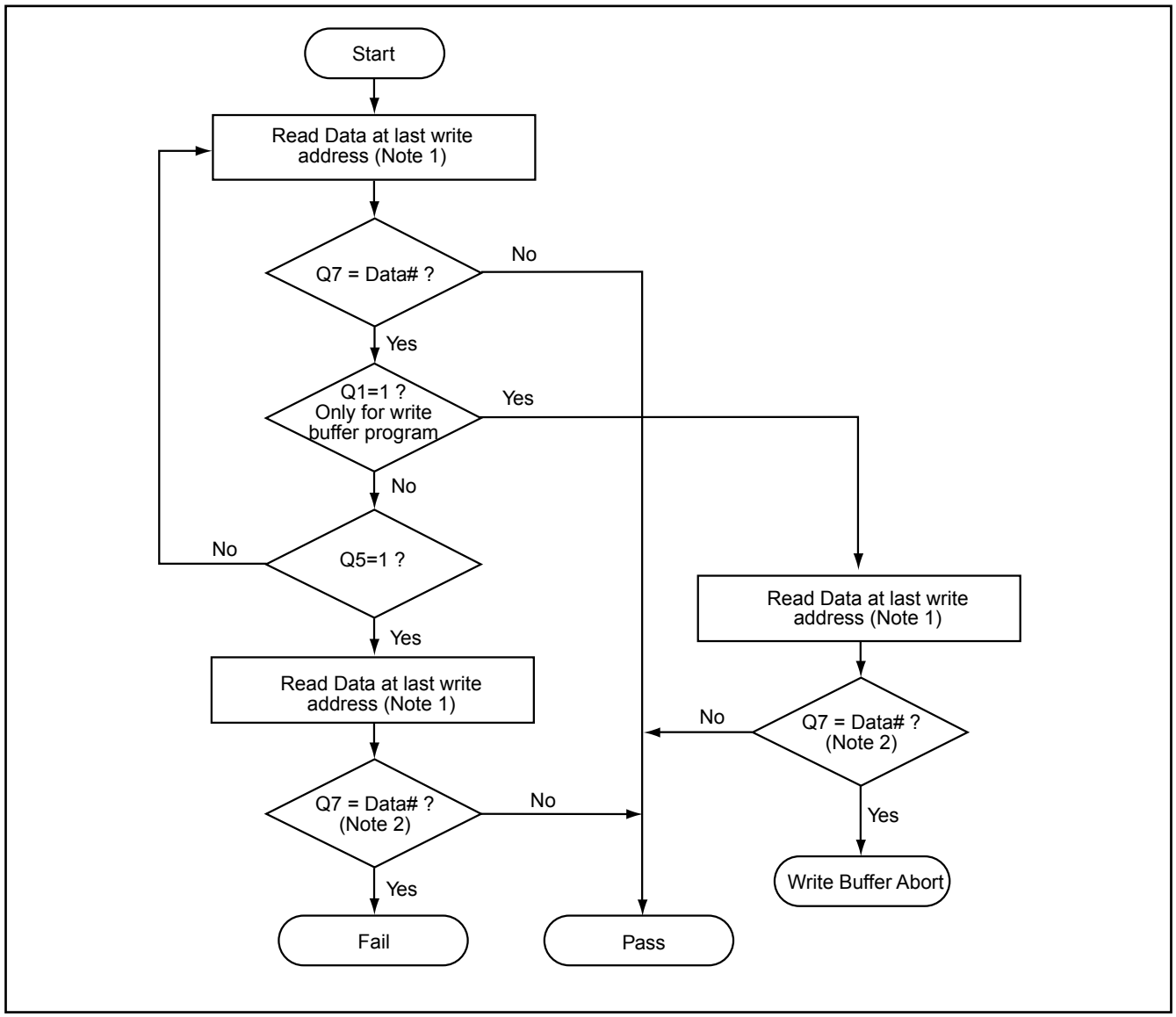


**Figure 18. STATUS POLLING FOR WORD PROGRAM/ERASE**




**Notes:**
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 may change simultaneously with Q5, so even Q5=1, Q7 should be reverify.

**Figure 19. STATUS POLLING FOR WRITE BUFFER PROGRAM**




**Notes:**

1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 may change simultaneously with Q5, so even Q5=1, Q7 should be reverify.

**Figure 20. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)**

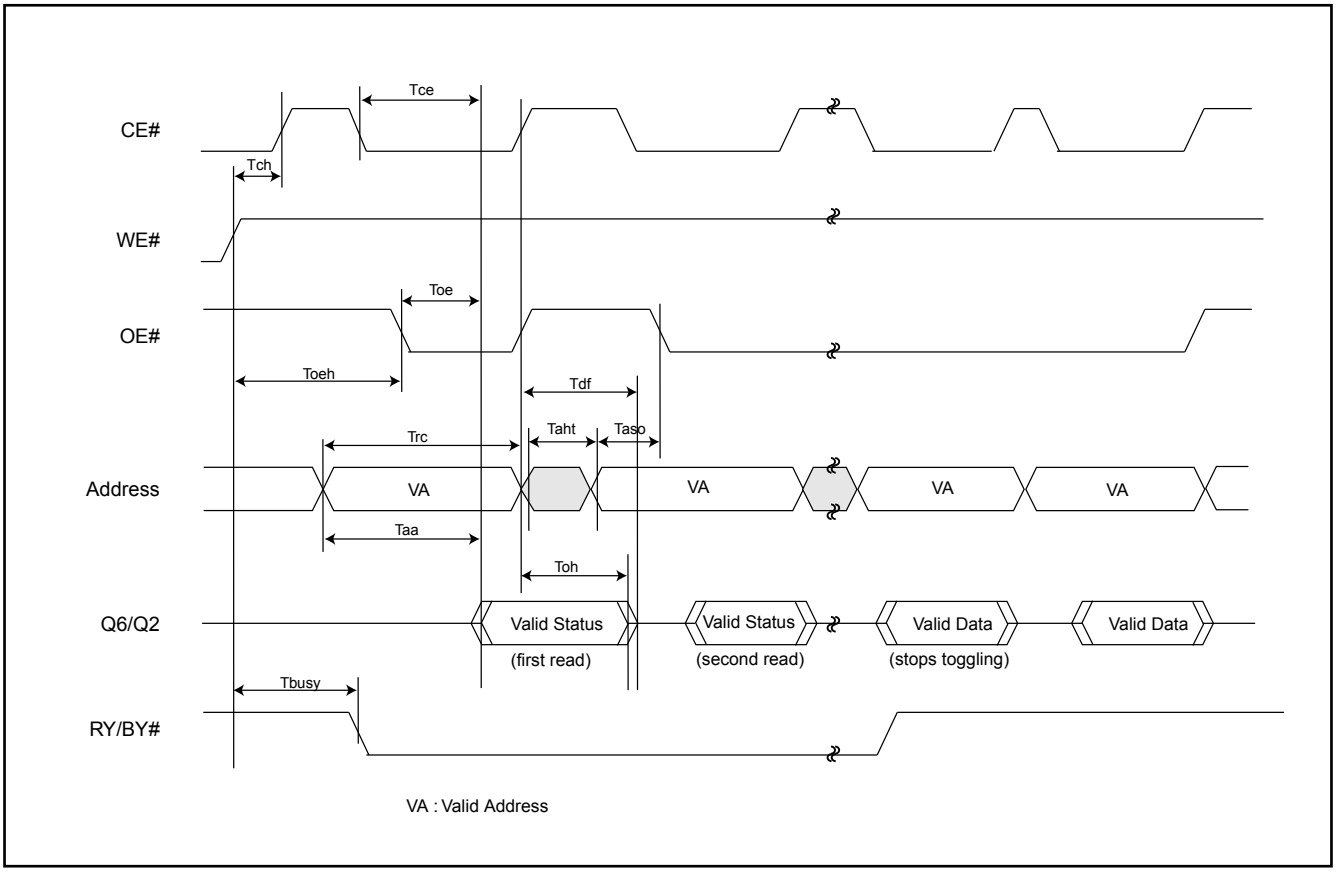
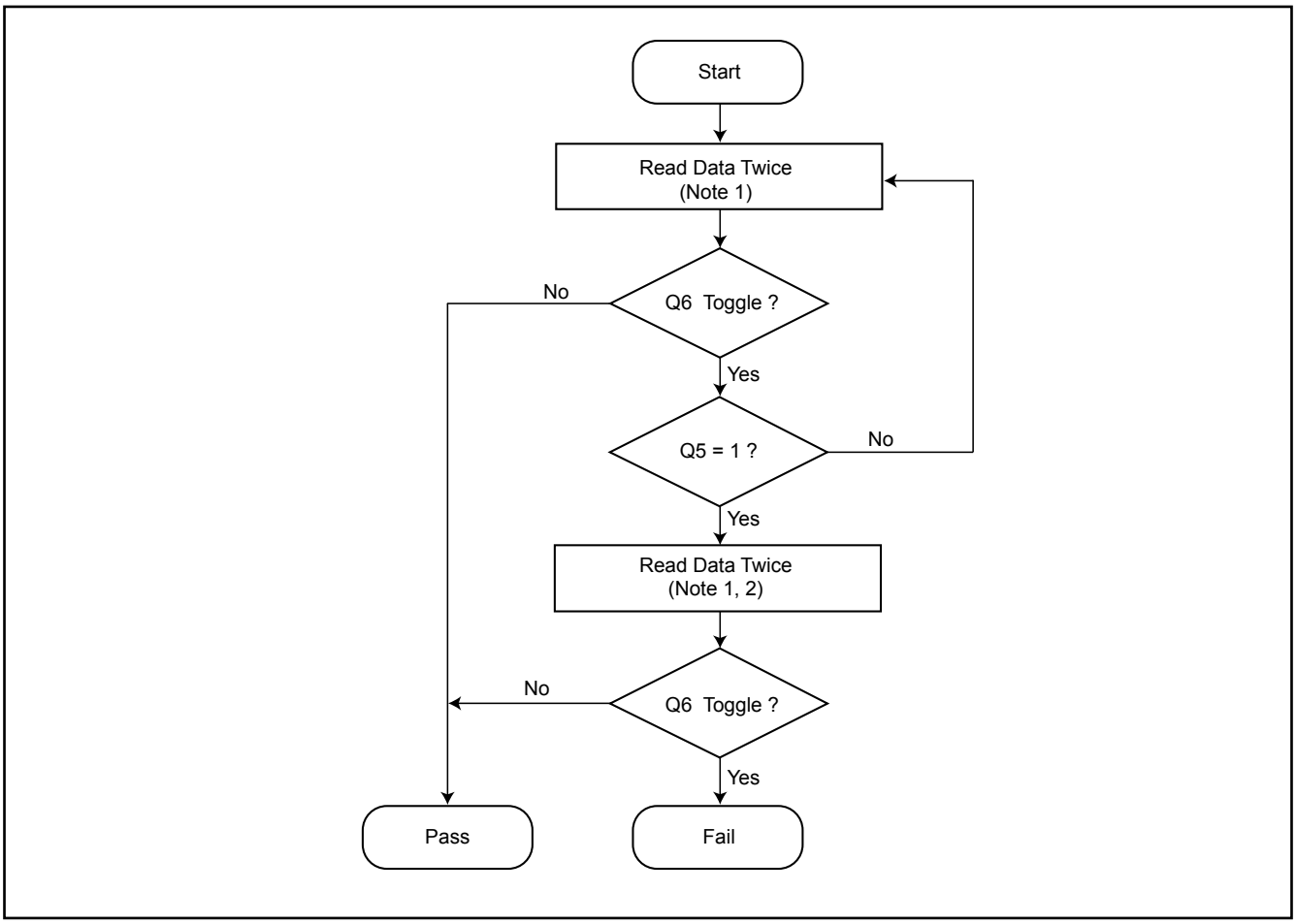


**Figure 21. TOGGLE BIT ALGORITHM**




**Notes:**
1. Toggle bit Q7-Q0 should be read twice to check if it is toggling.
2. While Q5=1, the toggle bit (Q6) may stop toggling. Therefore, the system should be read again.

## AC CHARACTERISTICS

### WORD/BYTE CONFIGURATION (BYTE#)

| Parameter | Description | Test Setup | All Speed Options | Unit |
|---|---|---|---|---|
| Telfl/Telfh | CE# to BYTE# from L/H | Max. | 5 | ns |
| Tflqz | BYTE# from L to Output Hiz | Max. | 30 | ns |
| Tfhqv | BYTE# from H to Output Active | Min. | 90 | ns |

**Figure 22. BYTE# TIMING WAVEFORM FOR READ OPERATIONS (BYTE# switching from byte mode to word mode)**

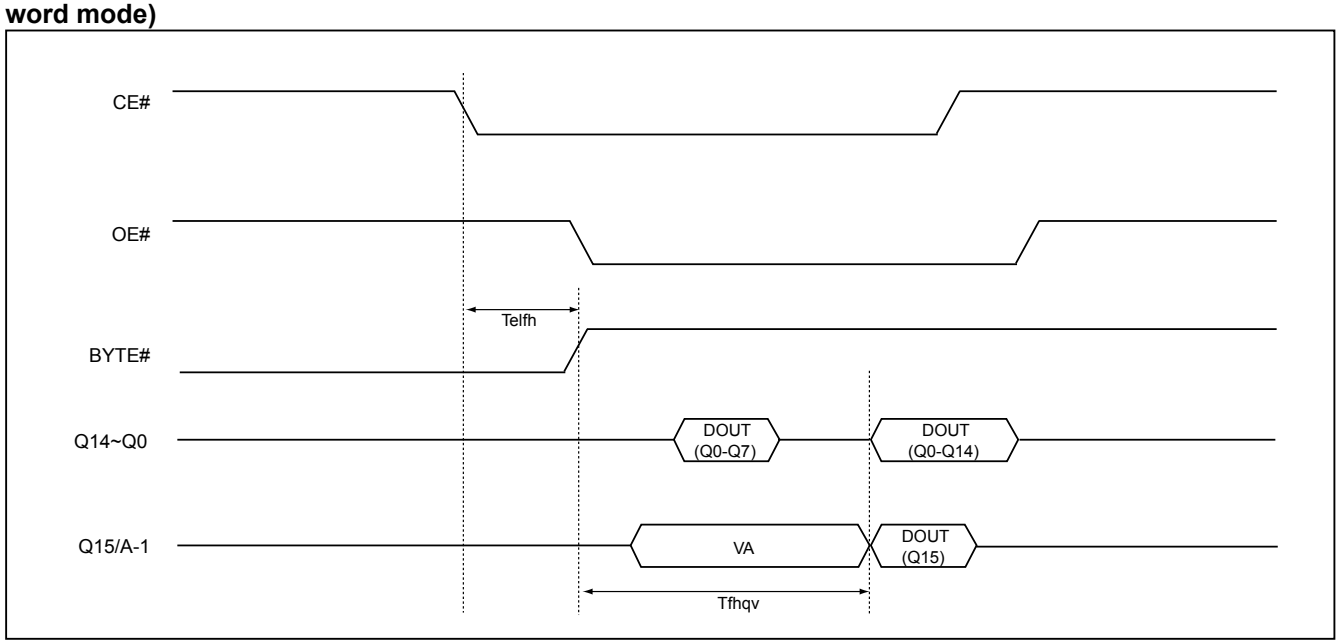
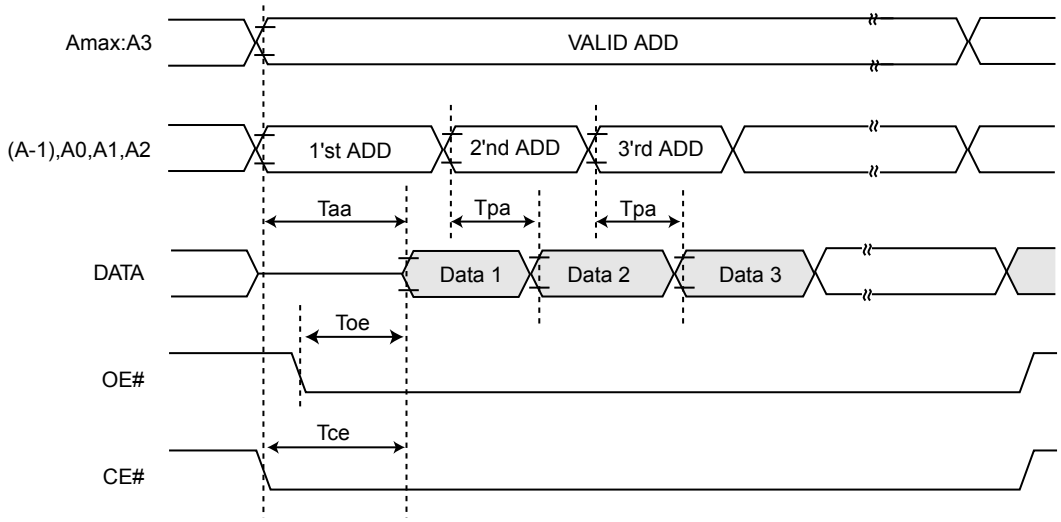


**Figure 23. PAGE READ TIMING WAVEFORM**




Note: CE#, OE# are enable.
Page size is 8 words in Word mode, 16 bytes in Byte mode.
Address are A2~A0 for Word mode, A2~A-1 for Byte mode.

## AC CHARACTERISTICS

| Item | | Typ. | Max. |
|---|---|---|---|
| WEB high to release from deep power down mode | tRDP | 100us | 200us |
| WEB high to deep power down mode | tDP | 10us | 20us |

**Figure 24. DEEP POWER DOWN MODE WAVEFORM**

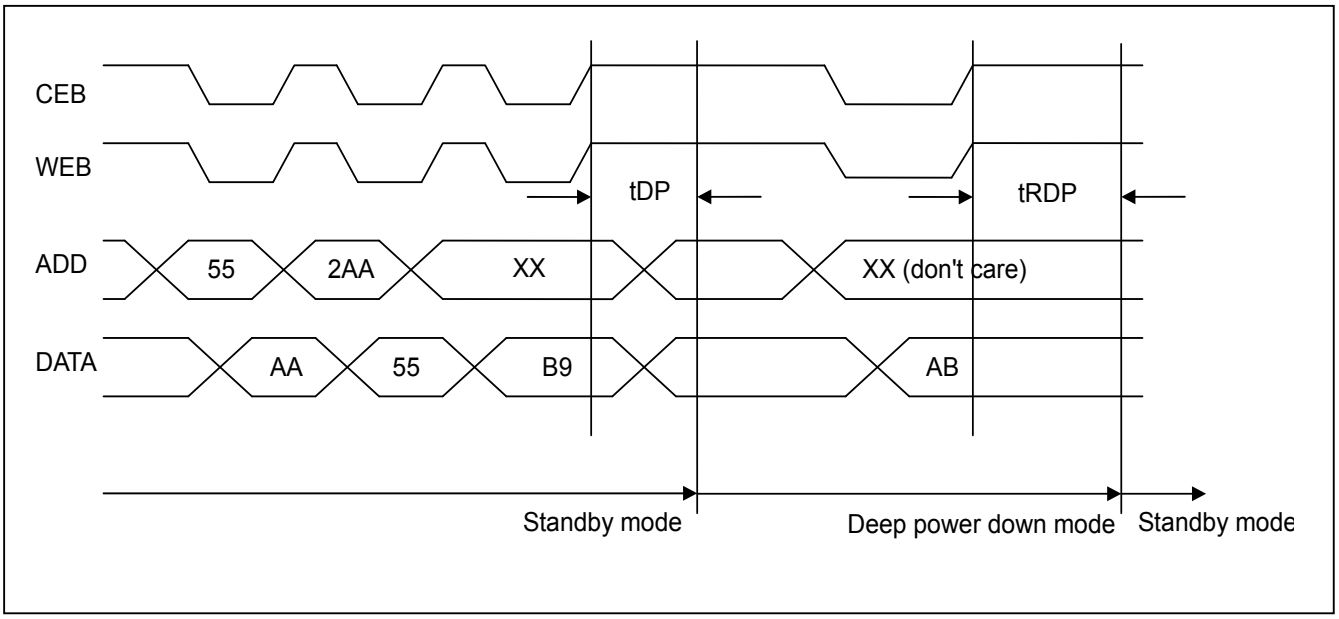
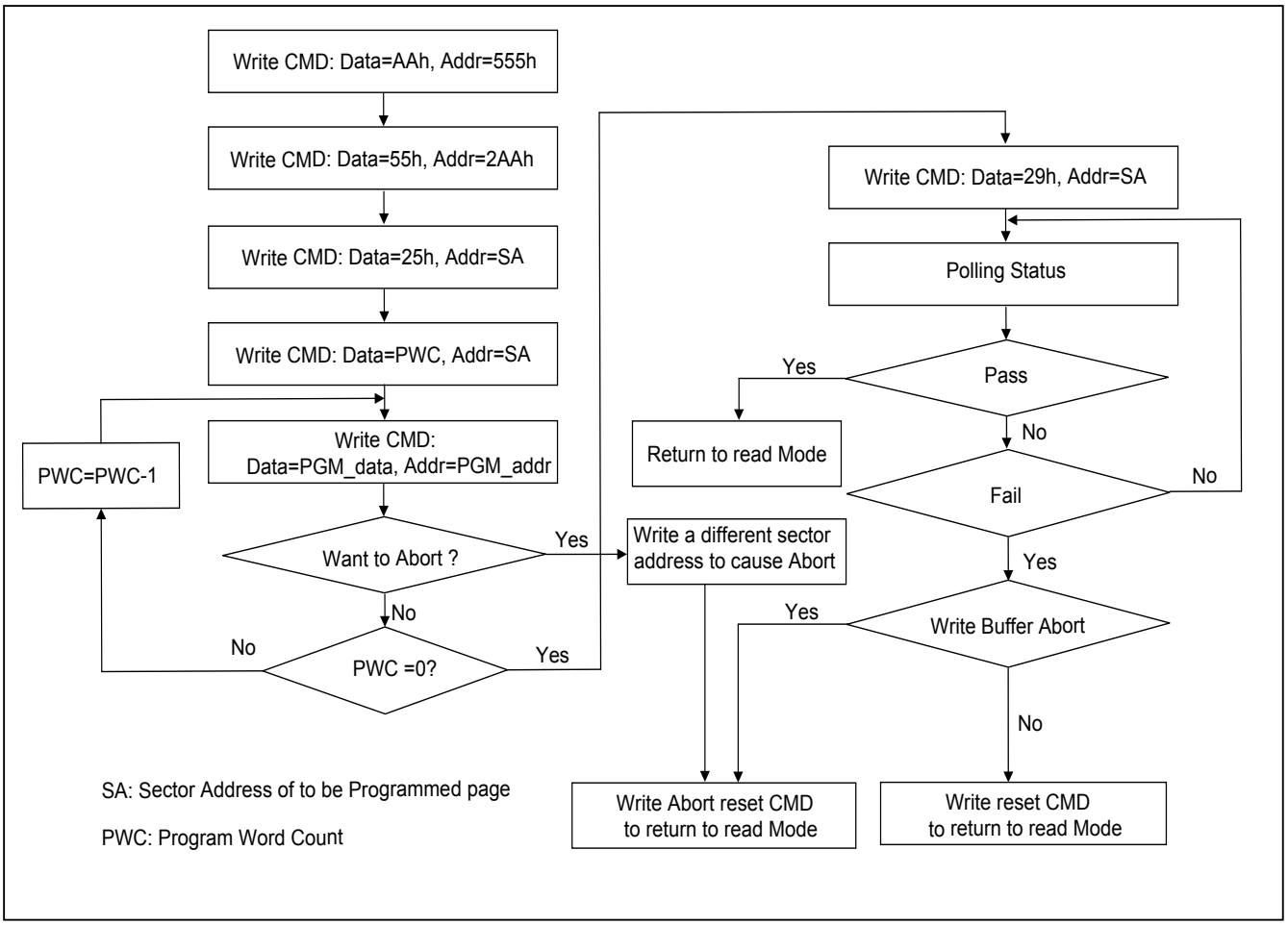


**Figure 25. WRITE BUFFER PROGRAM FLOWCHART**



## RECOMMENDED OPERATING CONDITIONS

### At Device Power-Up

AC timing illustrated in *Figure A* is recommended for the supply voltages and the control signals at device power-up (e.g. Vcc and CE# ramp up simultaneously). If the timing in the figure is ignored, the device may not operate correctly.

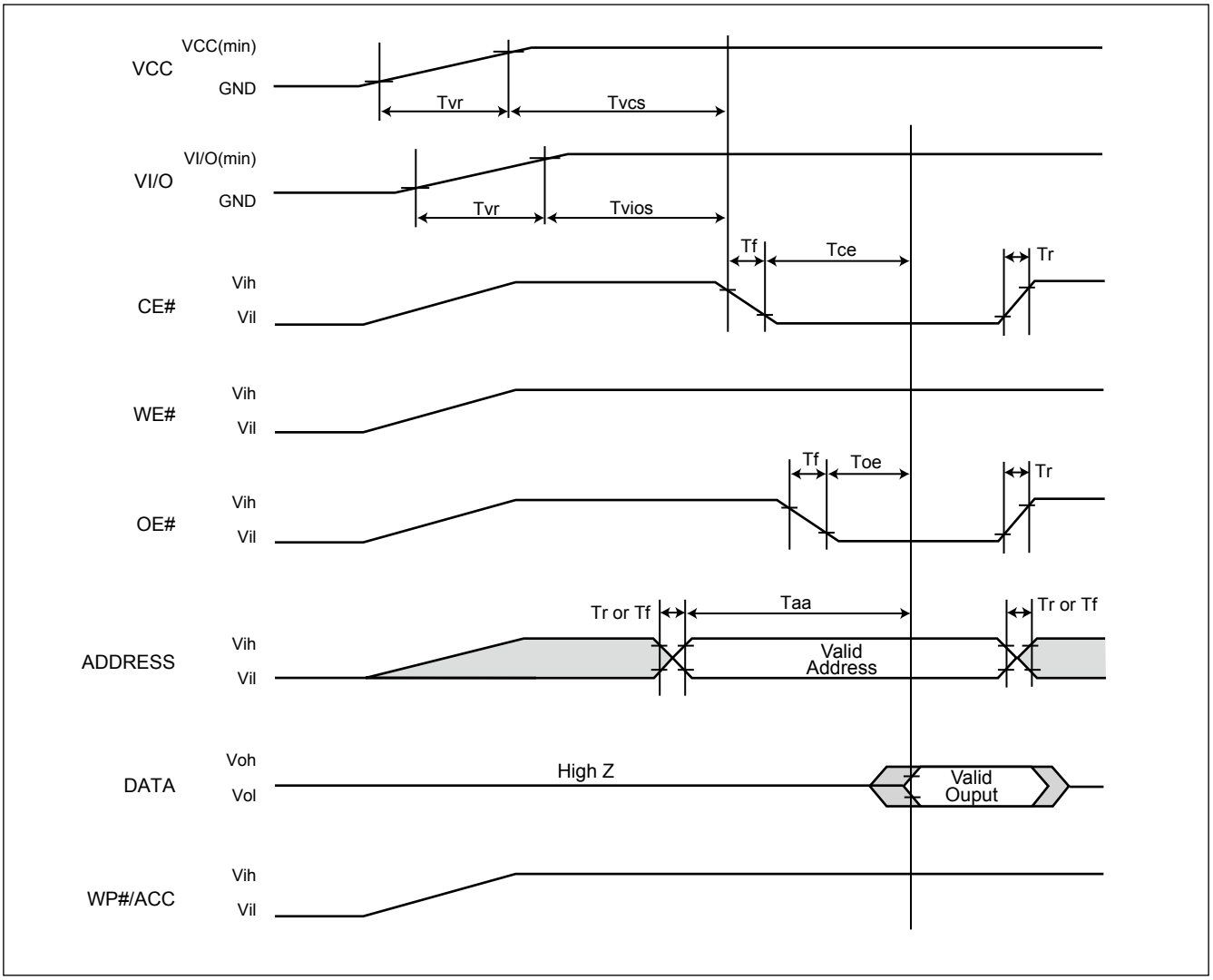



**Figure A. AC Timing at Device Power-Up**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| Tvr | VCC Rise Time | 20 | 500000 | us/V |
| Tr | Input Signal Rise Time | | 20 | us/V |
| Tf | Input Signal Fall Time | | 20 | us/V |
| Tvcs | VCC Setup Time | 500 | | us |
| Tvios | VI/O Setup Time | 500 | | us |

**Notes:**
1. VI/O<VCC+200mV.
2. Not test 100%

## ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Limits | | | Units |
|---|---|---|---|---|
| | Min. | Typ. (1) | Max. (2) | |
| Chip Erase Time | | 60 | 125 | sec |
| Sector Erase Time | | 0.5 | 3.5 | sec |
| Chip Programming Time | | 50 | 180 | sec |
| Word Program Time | | 10 | 180 | us |
| Total Write Buffer Time | | 120 | 240 | us |
| ACC Total Write Buffer Time | | 70 | | us |
| Erase/Program Cycles | 100,000 | | | Cycles |

**Notes:**
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC. Programming specifications assume checkboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Erase/Program cycles comply with JEDEC JESD-47 & 22-A117 standard.
4. Exclude 00h program before erase operation.

## DATA RETENTION

| Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|
| Data retention | 55˚C | 20 | | years |

## LATCH-UP CHARACTERISTICS

| | Min. | Max. |
|---|---|---|
| Input Voltage voltage difference with GND on WP#/ACC and A9 pins | -1.0V | 10.5V |
| Input Voltage voltage difference with GND on all normal pins input | -1.0V | 1.5Vcc |
| Vcc Current | -100mA | +100mA |
| All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing | | |

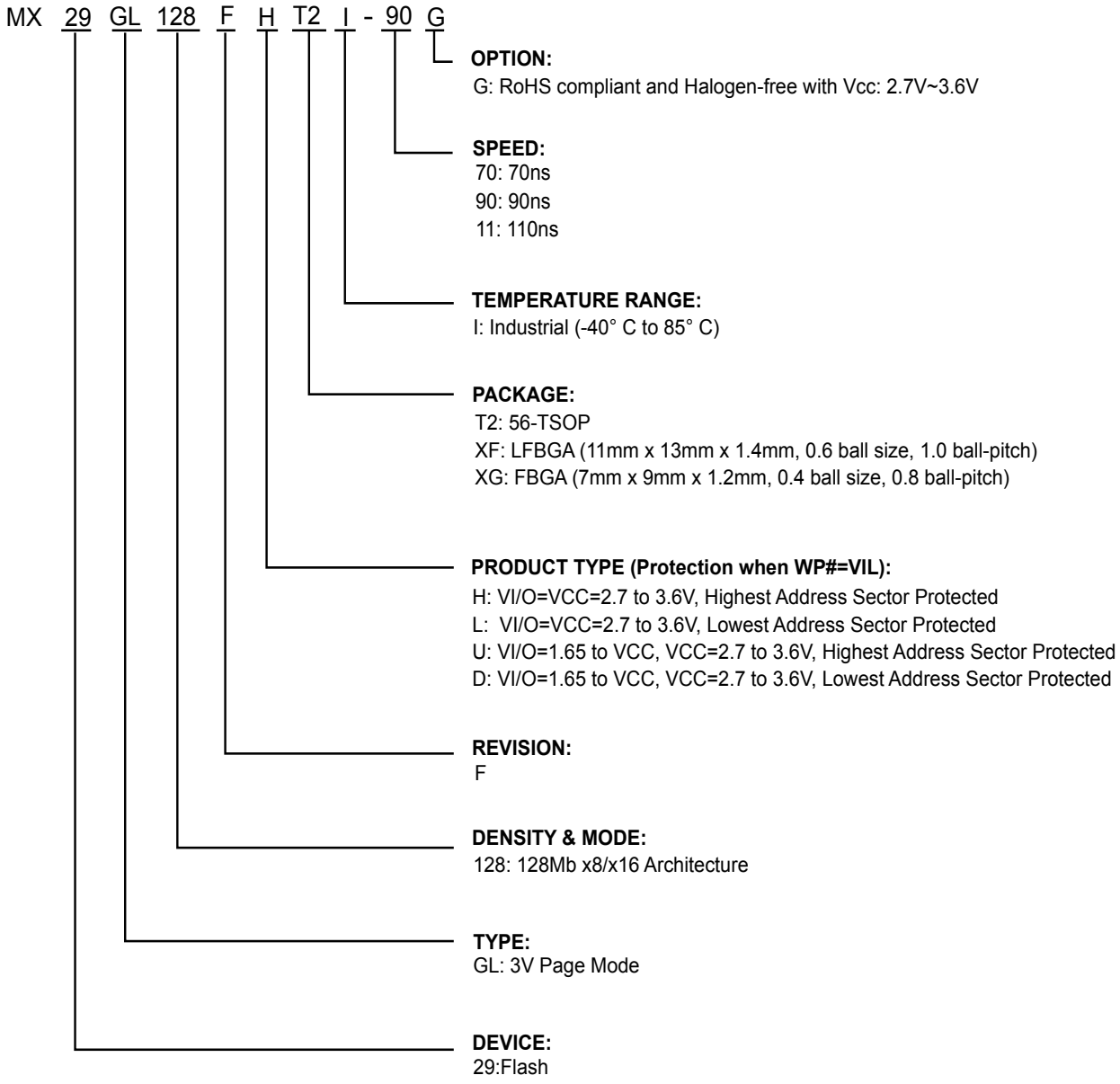
## PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Set | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| CIN2 | Control Pin Capacitance | VIN=0 | 7.5 | 15 | pF |
| COUT | Output Capacitance | VOUT=0 | 8.5 | 12 | pF |
| CIN | Input Capacitance | VIN=0 | 6 | 7.5 | pF |

## ORDERING INFORMATION

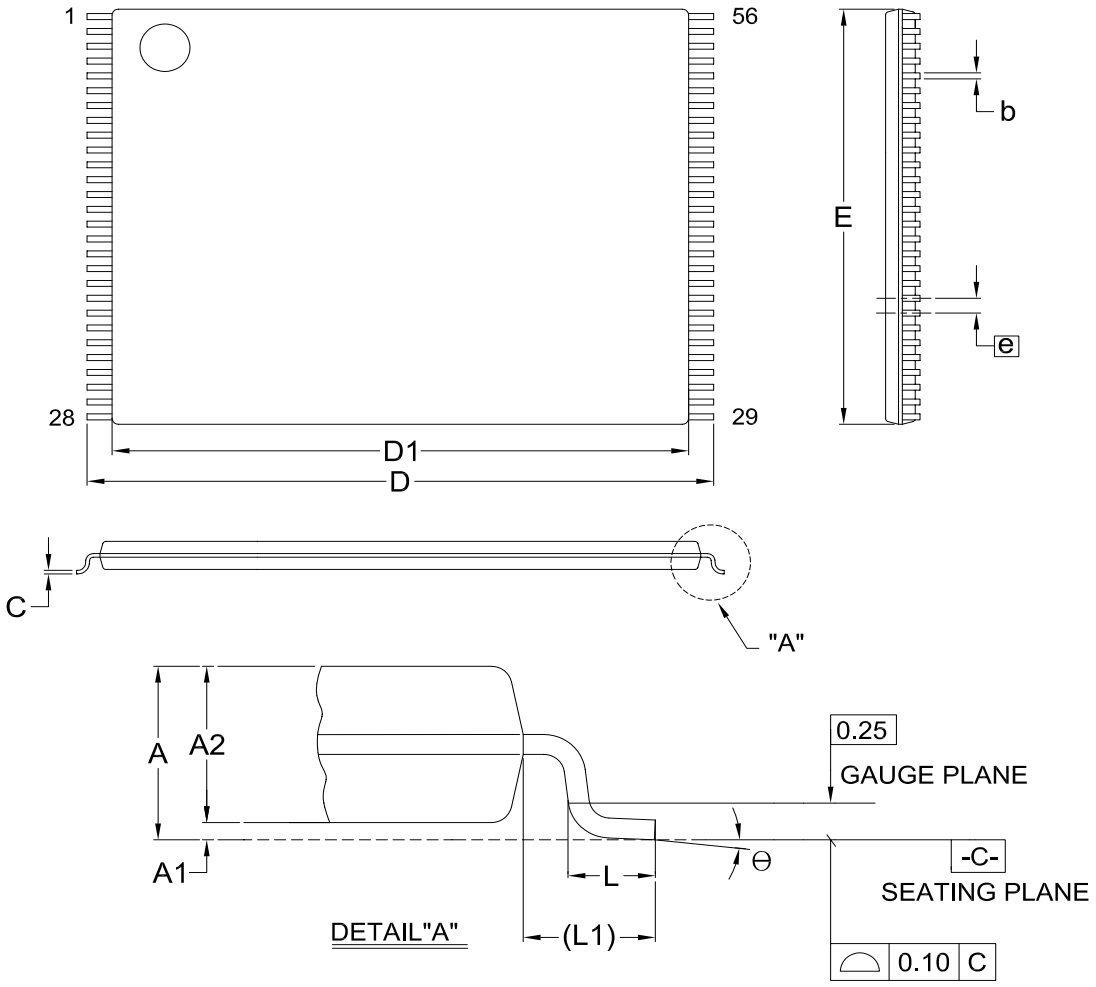
| PART NO. | ACCESS TIME (ns) | PACKAGE | Remark |
|---|---|---|---|
| MX29GL128FHT2I-70G | 70 | 56 Pin TSOP | |
| MX29GL128FLT2I-70G | 70 | 56 Pin TSOP | |
| MX29GL128FHXFI-70G | 70 | 64 LFBGA | |
| MX29GL128FLXFI-70G | 70 | 64 LFBGA | |
| MX29GL128FHXGI-70G | 70 | 56 FBGA | |
| MX29GL128FLXGI-70G | 70 | 56 FBGA | |
| MX29GL128FHT2I-90G | 90 | 56 Pin TSOP | |
| MX29GL128FLT2I-90G | 90 | 56 Pin TSOP | |
| MX29GL128FHXFI-90G | 90 | 64 LFBGA | |
| MX29GL128FLXFI-90G | 90 | 64 LFBGA | |
| MX29GL128FHXGI-90G | 90 | 56 FBGA | |
| MX29GL128FLXGI-90G | 90 | 56 FBGA | |
| MX29GL128FUT2I-90G | 90 | 56 Pin TSOP | |
| MX29GL128FDT2I-90G | 90 | 56 Pin TSOP | |
| MX29GL128FUT2I-11G | 110 | 56 Pin TSOP | |
| MX29GL128FDT2I-11G | 110 | 56 Pin TSOP | |
| MX29GL128FUXFI-11G | 110 | 64 LFBGA | |
| MX29GL128FDXFI-11G | 110 | 64 LFBGA | |

## PART NAME DESCRIPTION



## PACKAGE INFORMATION

Doc. Title: Package Outline for TSOP(I) 56L (14X20mm)

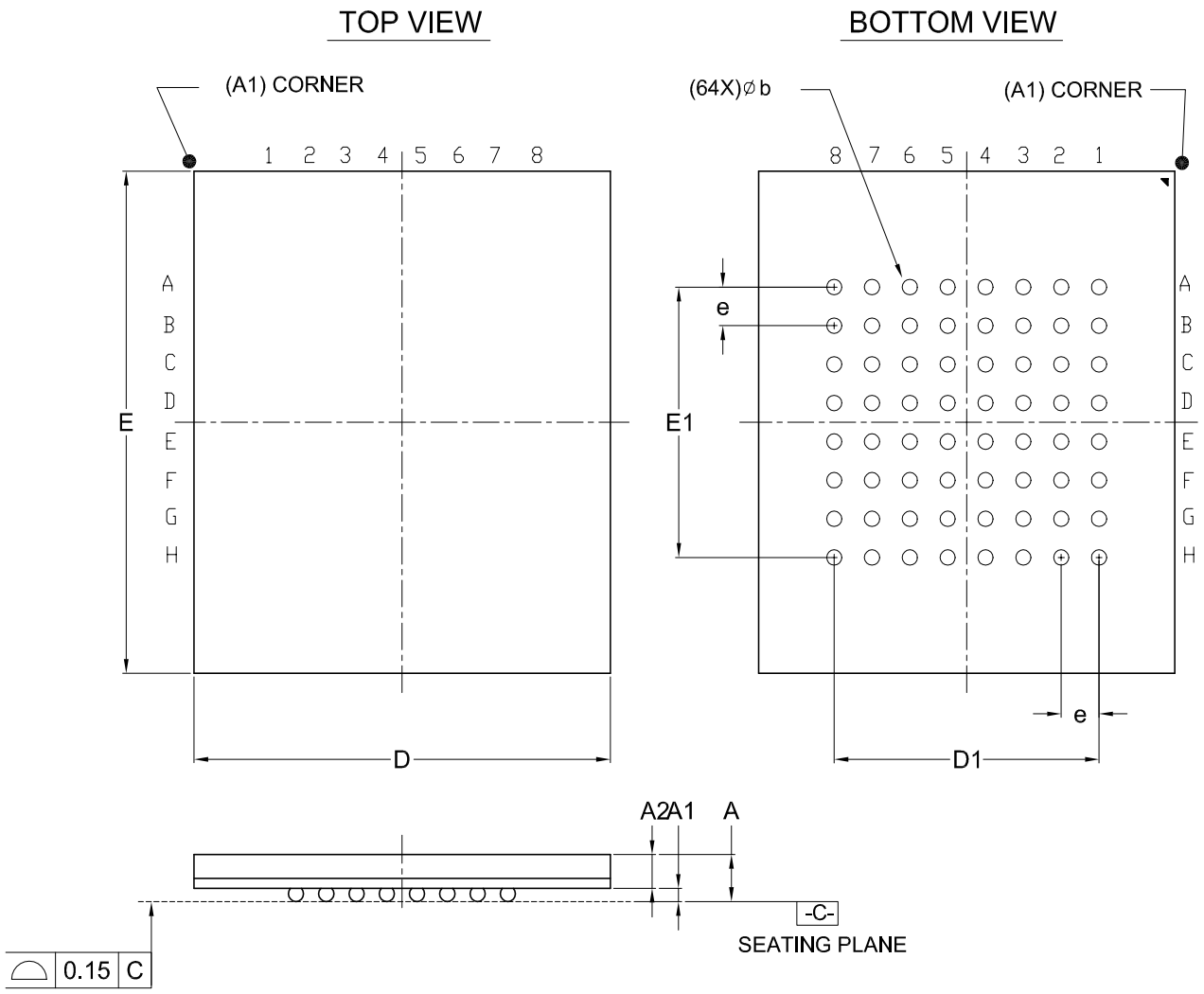



Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | D1 | E | e | L | L1 | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | — | 0.05 | 0.95 | 0.17 | 0.10 | 19.80 | 18.30 | 13.90 | — | 0.50 | 0.70 | 0° |
| | Nom. | — | 0.10 | 1.00 | 0.20 | 0.13 | 20.00 | 18.40 | 14.00 | 0.50 | 0.60 | 0.80 | 5° |
| | Max. | 1.20 | 0.15 | 1.05 | 0.27 | 0.21 | 20.20 | 18.50 | 14.10 | — | 0.70 | 0.90 | 8° |
| Inch | Min. | — | 0.002 | 0.037 | 0.007 | 0.004 | 0.780 | 0.720 | 0.547 | — | 0.020 | 0.028 | 0° |
| | Nom. | — | 0.004 | 0.039 | 0.008 | 0.005 | 0.787 | 0.724 | 0.551 | 0.020 | 0.024 | 0.031 | 5° |
| | Max. | 0.047 | 0.006 | 0.041 | 0.011 | 0.008 | 0.795 | 0.728 | 0.555 | — | 0.028 | 0.035 | 8° |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-1608 | 6 | MO-142 | | | |

Doc. Title: Package Outline for CSP 64BALL(11X13X1.4MM,BALL PITCH 1.00MM,BALL DIAMETER 0.6MM)

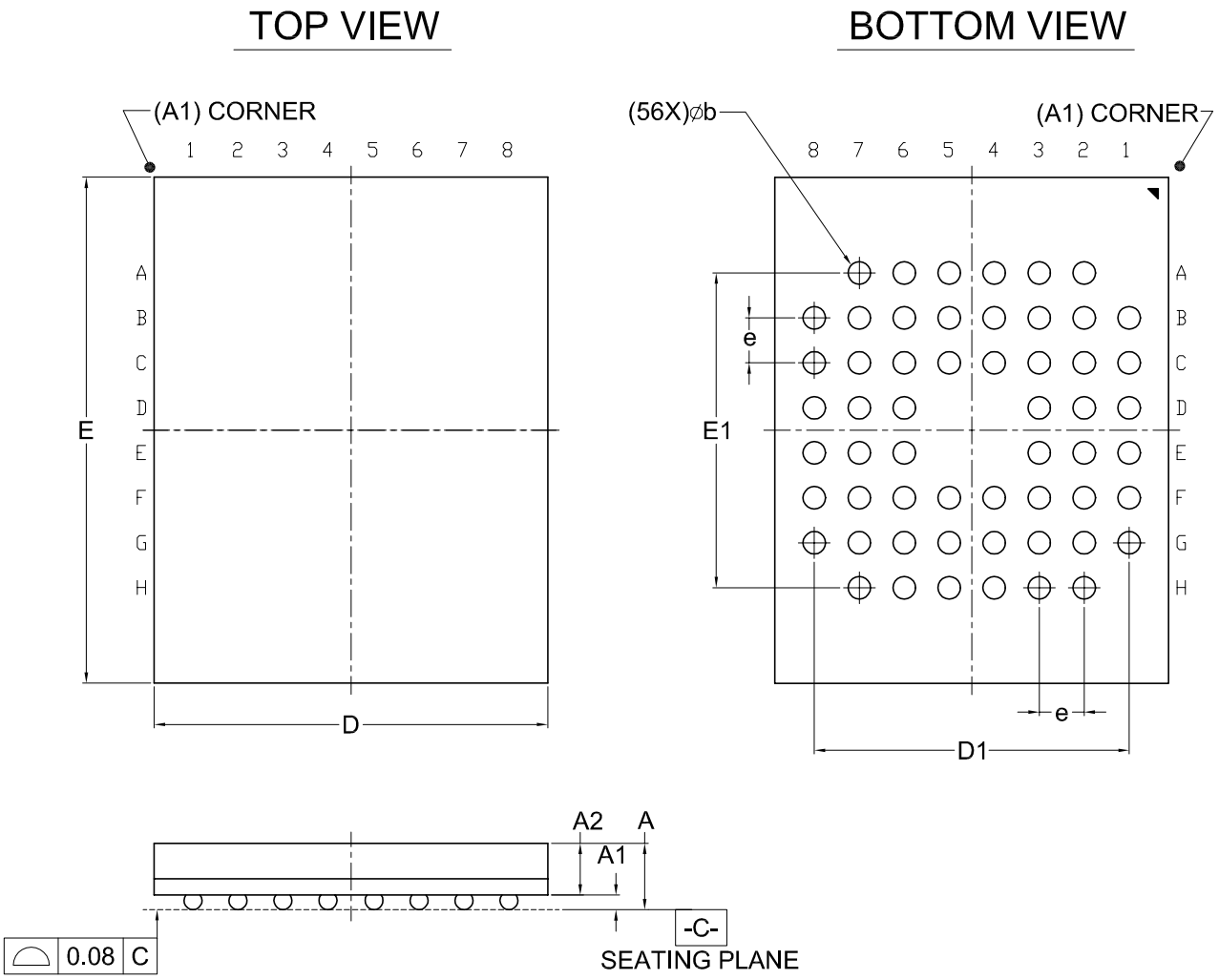



Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.40 | 0.65 | 0.50 | 10.90 | | 12.90 | | |
| | Nom. | --- | 0.50 | --- | 0.60 | 11.00 | 7.00 | 13.00 | 7.00 | 1.00 |
| | Max. | 1.40 | 0.60 | --- | 0.70 | 11.10 | | 13.10 | | |
| Inch | Min. | --- | 0.016 | 0.026 | 0.020 | 0.429 | | 0.508 | | |
| | Nom. | --- | 0.020 | --- | 0.024 | 0.433 | 0.276 | 0.512 | 0.276 | 0.039 |
| | Max. | 0.055 | 0.024 | --- | 0.028 | 0.437 | | 0.516 | | |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-4247 | 1 | MO-192 | | | |

Doc. Title: Package Outline for CSP 56BALL(7X9X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.25 | 0.65 | 0.35 | 6.90 | --- | 8.90 | — | — |
| | Nom. | --- | 0.30 | — | 0.40 | 7.00 | 5.60 | 9.00 | 5.60 | 0.80 |
| | Max. | 1.20 | 0.35 | — | 0.45 | 7.10 | --- | 9.10 | — | — |
| Inch | Min. | — | 0.010 | 0.026 | 0.014 | 0.272 | --- | 0.350 | — | — |
| | Nom. | — | 0.012 | — | 0.016 | 0.276 | 0.220 | 0.354 | 0.220 | 0.031 |
| | Max. | 0.047 | 0.014 | — | 0.018 | 0.280 | --- | 0.358 | — | — |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-4265 | 1 | | | | |

## REVISION HISTORY

| Revision No. | Description | Page | Date |
|---|---|---|---|
| 0.01 | 1. Changed title from "Advanced Information" to "Preliminary"<br>2. Modified Figure 19. Status Polling For Write Buffer Program for Abort function<br>3. Modified Total Write Buffer Time from 200us(typ.) to 120us(typ.); ACC Total Write Buffer Time from 100us(typ.) to 70us(typ.)<br>4. Modified standby current (typ.) from 50uA to 30uA | P5<br>P15,57<br>P64<br>P5,39 | JUN/28/2011 |
| 0.02 | 1. Added 56-Ball FBGA package information | P5,7,65,66,<br>P69 | JUL/14/2011 |
| 0.03 | 1. Modified Pin Configuration--56 FBGA<br>2. Modified Icr1 | P7<br>P39 | OCT/12/2011 |
| 1.0 | 1. Removed "Preliminary"<br>2. Added access time 70ns spec, Part Name Description and Ordering Information | P5<br>P5,41,65,66 | DEC/07/2011 |
| 1.1 | 1. Modified Figure 14. CE# Controlled Write Timing Waveform<br>2. Added VI/O Setup Time<br>3. Added access time 70ns spec 64-LFBGA Ordering Information<br>4. Removed access time 90ns spec with VI/O Ordering Information | P52<br>P63<br>P65<br>P65 | JUN/28/2012 |
| 1.2 | 1. Added access time 70ns spec for Trc, Twc and Tcwc<br>2. Modified Figure 23. PAGE READ TIMING WAVEFORM<br>3. Added "Note 1. Query data are always presented on the lowest data output Q7~Q0 only, Q8~Q15 are "0". | P41<br>P61<br>P35 | NOV/09/2012 |
| 1.3 | 1. Added 90ns spec for VI/O<br>2. Modified G5 pin for 56 FBGA<br>3. Added MAX. Total Write Buffer Time (480us)<br>4. Modified Sector Protection Status Table | P5,41,66<br>P7<br>P65<br>P30 | APR/26/2013 |
| 1.4 | 1. Updated parameters for DC Characteristics.<br>2. Updated Erase and Programming Performance.<br>3. Content correction | P5,39<br>P5,42,65<br>P25~30 | OCT/30/2013 |
| 1.5 | 1. Added 70ns Access Time 56 FBGA Pacakges for Ordering Information | P66 | AUG/24/2015 |

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