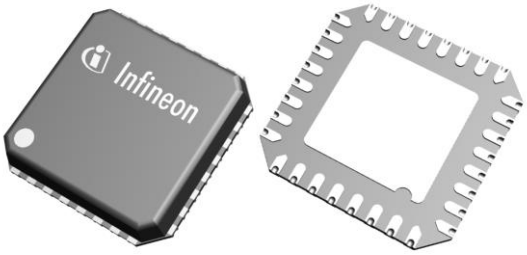
Target Data Sheet

BGMC1210 Power Amplifier Bias and Control IC

Features

- 2x 4 analog outputs with up to 50mA sourcing and 20mA sinking capability
  - 12 Bit DACs with programmable ranges:
    - 0...3.5V and 0...7V
    - bipolar range support: from -7…0V up to 0…7V
  - Programmable offset for range adaption
  - Internal voltage reference
  - Configurable tracking mode
  - Optional temperature compensation of analog outputs via Look-Up Table (LUT)
  - Configurable gate bias compensation
- 2x 2 bias switches for time-division-duplex (TDD) support with configurable clamp voltage:
  - Fixed to VREF
  - Neighbouring DAC (tracking opt.)
  - Tracking clamping DAC
- 2x Current Shunt ADC
  - 12 Bit SD ADC with internal reference
  - Programmable Full-Scales: 15mV, 30mV, 60mV, 120mV, 240mV
  - Offset compensated
  - Floating input stage up to 60V common mode
- Voltage ADC:
  - 11 Bit SAR ADC with internal reference
  - Available Inputs:
    - 2x 60V Full-Scale
    - 2x 3V Full-Scale
    - Supply pins



PG-VQFN-32 5x5mm^2

RoHS Halogen-Free Lead-Free

- Die Temperature Sensor
  - 9 bit resolution
  - Measurement Range: -40°C to 160°C
  - 2.5°C accuracy
  - Can be used for temperature compensation
- I3C Serial Interface with I^{2}C support
  - SDR (12.5MBit/s) and HDR-DDR (25MBit/s) transmission modes supported
  - Device ID selection via 3-state inputs
- Temperature Range (junction): -40°C to 150°C

Potential applications

Cellular Base Stations: bias-control circuit for power amplifiers

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The BGMC1210 is a bias and control IC for Power Amplifiers (PA) that operate with negative Gate-Source voltages (e.g. GaN) and/or positive Gate-Source voltages (e.g. LDMOS). The BGMC1210 supports up to 2 PAs with 4 DAC outputs per each side of the IC. DACs have a resolution of 12 Bit each, supplied by an internal reference voltage and buffered by an amplifier providing up to 50mA driving current. Block diagram of the BGMC1210 is shown in Figure 1 and simplified typical PA application circuit is shown in Figure 2. The ranges and output voltages can be programmed via an I3C interface, which is backward compatible with I^2C. The DACs are separated into two groups A and B, which can support independent output voltage ranges. Supported output voltage ranges are 0…7 V and 0…3.5 V, which can be offset into negative voltage domain depending on the selected DAC supply voltage for corresponding group at pins VREF_A/VREF_B and VDDA_A/VDDA_B. Thus, four DACs can support positive voltage range of 0…+7V or 0…+3.5V, whereas the other group of four DACs can support negative voltage range of -7…0V or -3.5…0V (or any range in between defined by lower DAC supply voltage at pins VREF_A/VREF_B, such as e.g. -6…+1). On top of that there is an OFFSET parameter, which allows to shift the voltage within the supply range.

Biasing switches for Time-Division-Duplex (TDD) support are present on 2 outputs per side (OUT_xy), directly controlled via dedicated pins EN_OUT_x (x = [A, B]; y = [0, 2]). The grouping of switched outputs by EN_OUT_x inputs can be defined. Clamping voltages for switched outputs can be set to a fixed VREF_x potential, DAC_x1/DAC_x3 output or a dedicated 6-bit clamping DAC voltage.

The output values of the DAC can be configured to compensate the power amplifier temperature drift via a Look-Up Table (LUT) and an integrated temperature sensor.

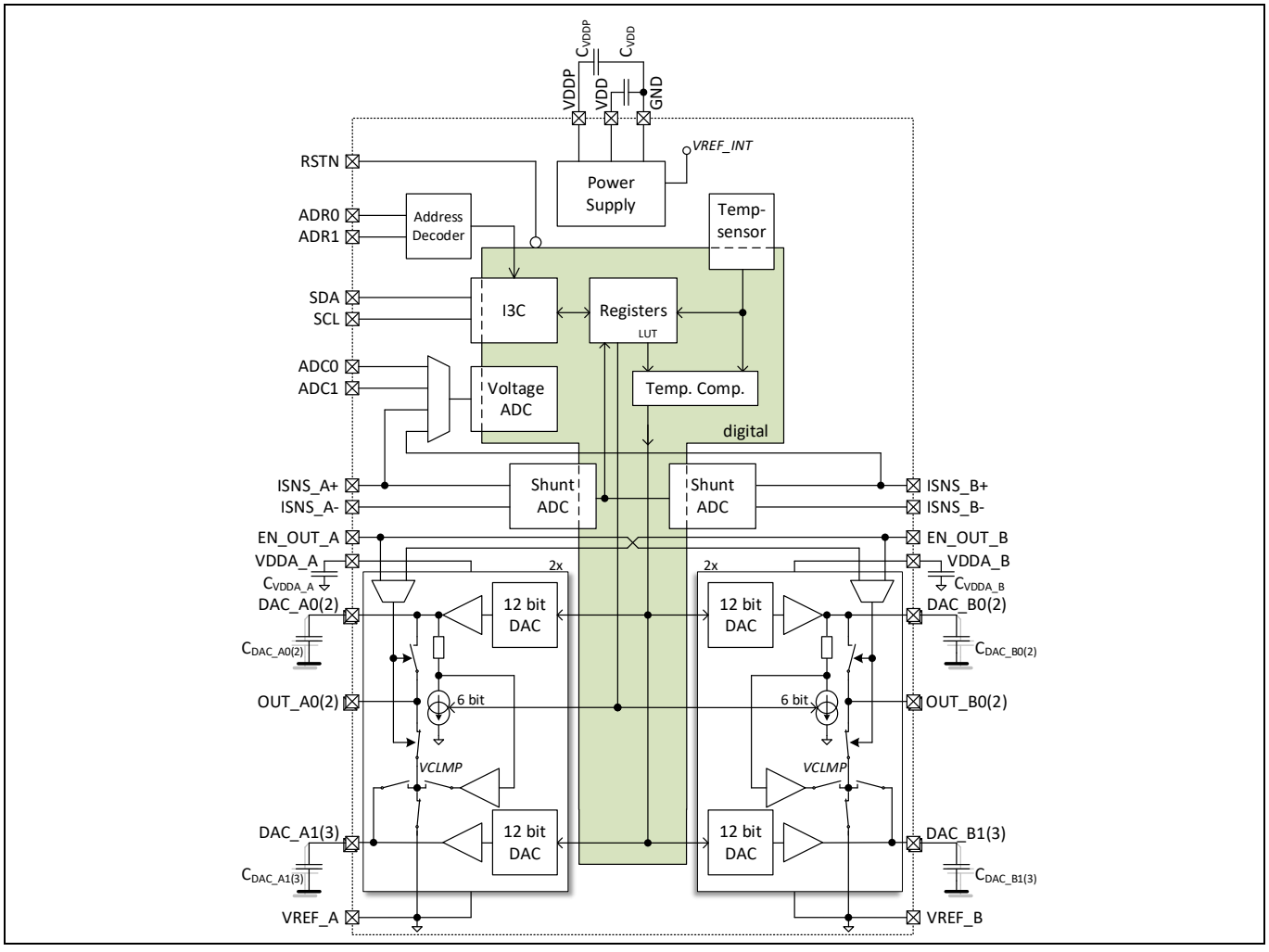


Figure 1 Functional Block Diagram

Pin Configuration

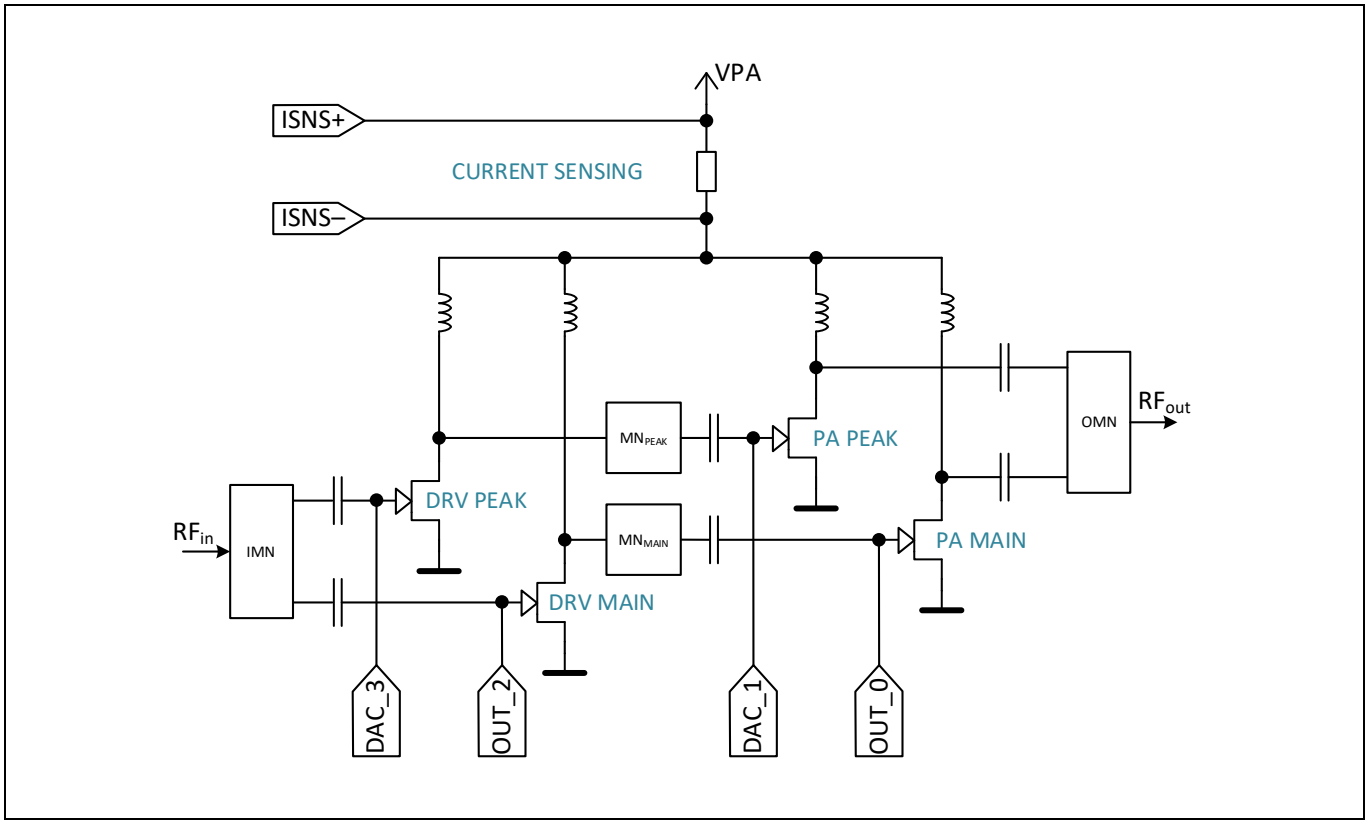


Figure 2 Typical Power Amplifier application circuit

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1 Pin Configuration

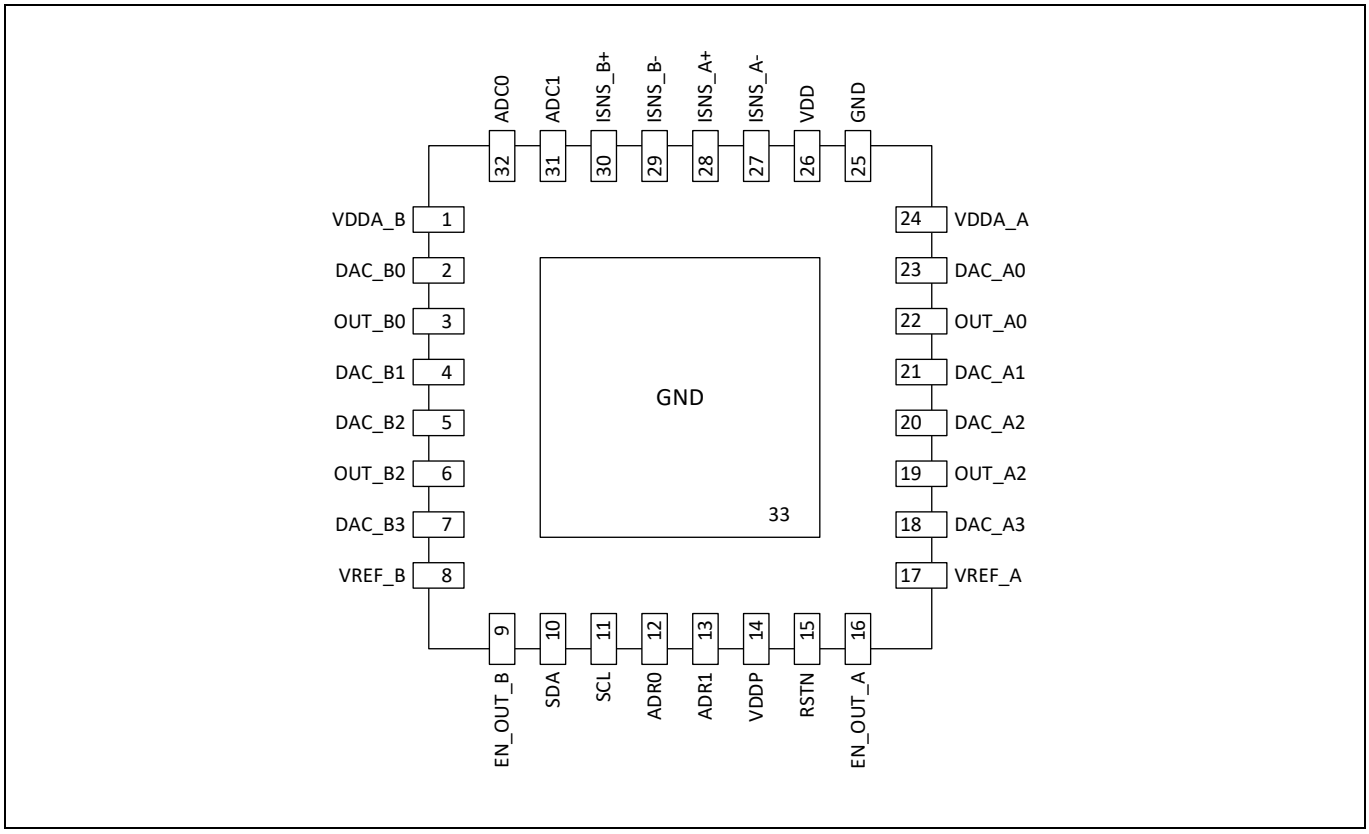

Figure 3 Pin number assignment of BGMC1210

Table 1 Pin definition and function

Pin #	Symbol	Function	Description
1	VDDA_B	SUP	Upper DAC supply voltage; depending on selected DAC output range, connects either to positive supply (positive gate voltages) or GND (negative gate voltages); side B
2	DAC_B0	DAC OUT	DAC out; side B
3	OUT_B0	OUT	Switched bias output; connects to DAC_B0 or VCLMP potential based on the level at configured EN_OUT_x, (x = [A, B]); VCLMP can be defined by VREF_B, DAC_B1 or CLMP DAC based on register configuration; side B
4	DAC_B1	DAC OUT	DAC out; no switching; side B
5	DAC_B2	DAC OUT	DAC out; side B
6	OUT_B2	OUT	Switched bias output; connects to DAC_B2 or VCLMP potential based on the level at configured EN_OUT_x, (x = [A, B]); VCLMP can be defined by VREF_B, DAC_B3 or CLMP DAC based on register configuration; side B
7	DAC_B3	DAC OUT	DAC out; no switching; side B
8	VREF_B	SUP	Lower DAC supply / reference voltage; depending on selected DAC output range, connects either to GND (positive gate voltages) or negative supply (negative gate voltages); side B
9	EN_OUT_B	IN	Switch the configured OUT_xy outputs between DAC_xy and corresponding VCLMP potential (x = [A, B]; y = [0, 2]); side B
10	SDA	IN/OUT	I3C/I²C data
11	SCL	IN	I3C/I²C clock

Pin Configuration

12	ADR0	IN	I3C/I²C Device ID, bit 0
13	ADR1	IN	I3C/I²C Device ID, bit 1
14	VDDP	SUP	Digital I/O pins supply rail
15	RSTN	IN	Asynchronous reset
16	EN_OUT_A	IN	Switch the configured OUT_xy outputs between DAC_xy and corresponding VCLMP potential (x = [A, B]; y = [0, 2]); side A
17	VREF_A	SUP	Lower DAC supply / reference voltage; depending on selected DAC output range, connects either to GND (positive gate voltages) or negative supply (negative gate voltages); side A
18	DAC_A3	DAC OUT	DAC out; no switching; side A
19	OUT_A2	OUT	Switched bias output; connects to DAC_A2 or VCLMP potential based on the level at configured EN_OUT_x, (x = [A, B]); VCLMP can be defined by VREF_A, DAC_A3 or CLMP DAC based on register configuration; side A
20	DAC_A2	DAC OUT	DAC out; side A
21	DAC_A1	DAC OUT	DAC out; no switching; side A
22	OUT_A0	OUT	Switched bias output; connects to DAC_A0 or VCLMP potential based on the level at configured EN_OUT_x, (x = [A, B]); VCLMP can be defined by VREF_A, DAC_A1 or CLMP DAC based on register configuration; side A
23	DAC_A0	DAC OUT	DAC out; side A
24	VDDA_A	SUP	Upper DAC supply voltage; depending on selected DAC output range, connects either to positive supply (positive gate voltages) or GND (negative gate voltages); side A
25	GND	SUP	Ground connection
26	VDD	SUP	Main supply voltage
27	ISNS_A-	ADC IN	Differential current sensing ADC negative input; side A
28	ISNS_A+	ADC IN	Differential current sensing ADC positive input / Voltage ADC input; side A
29	ISNS_B-	ADC IN	Differential current sensing ADC negative input; side B
30	ISNS_B+	ADC IN	Differential current sensing ADC positive input / Voltage ADC input; side B
31	ADC1	ADC IN	Voltage ADC input 1
32	ADC0	ADC IN	Voltage ADC input 0
33	GND	SUP	Ground connection

2 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1,2]

Parameter	Symbol / Function	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
Main supply	VDD	-0.3		5.5	V	
Pad supply	VDDP	-0.3		3.6	V	
Positive DAC supply [3]	VDDA_x	-0.3		8.0	V	
Negative DAC supply/reference [3]	VREF_x	-8.0		0.3	V	
DAC supply [3]	VDDA_x – VREF_x	-0.3		8.0	V	
Digital I/Os	IN/OUT	-0.3		VDDP+0.3	V	
DAC outputs [3]	DAC_xy	VREF_x-0.3		VDDA_x+0.3	V	
Switched outputs [3]	OUT_xy	VREF_x-0.3		VDDA_x+0.3	V	
Voltage ADC inputs	ADC0/1	-0.3		3.3	V	
Current sense inputs [3]	ISNS_x+/-	-0.3		60	V	
Differential current sense input voltage [3]	ISNS_x+ – ISNS_x-	-1		1	V	
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{STG}	-65		150	°C	

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltages are with respect to GND=0V unless otherwise noted. Currents are positive into and negative out of the specified terminal.

[3] x = [A, B]; y = [0, 1, 2, 3].

3 Specifications

3.1 Operational Ratings

Table 3 Operational Ratings[2]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
Main supply	VDD	3.1	3.3	5.5	V	
Pad supply	VDDP	1.65	1.80	3.60	V	
Positive DAC supply [1]	VDDA_x	0		8	V	
Negative DAC supply/reference [1]	VREF_x	-8		0	V	
DAC supply [1]	VDDA_x – VREF_x	3.1		8.0	V	
ISNS inputs	ISNS_x+/-	0		60	V	
Junction temperature	T_J	-40		150	°C	

[1] x = [A, B].

[2] All voltages are with respect to GND=0V unless otherwise noted.

3.2 ESD Ratings

Table 4 ESD Ratings[1]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
ESD robustness on all pins, Human Body Model (HBM)	V_{HBM}	-2		+2	kV	
ESD robustness on all pins, Charged Device Model (CDM)	V_{CDM}	-0.5		+0.5	kV	

[1] All voltages are with respect to GND=0V unless otherwise noted.

3.3 External components

Table 5 External components

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
DAC load capacitance [1]	C_{DAC_xy}	30 [2] / 100	1000	1200 [3]	nF	
VDD buffer capacitor	C_{VDD}		100		nF	
VDDP buffer capacitor	C_{VDDP}		100		nF	
VDDA_x-VREF_x buffer capacitance [1]	C_{VDDA_x}		1000		nF	Connected between VDDA_x and VREF_x
OUT load capacitance for VCLMP buffer usage [1]				5	nF	Maximum load capacitance for VCLMP buffer; VCLMP_x.SET_xy = 10_b or 11_b
VADC input buffer capacitance	$C_{ADC0/1}$		10		nF	Noise filter

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] Lower capacitance value is only valid if the load (DACCNF2.LD_xy) is configured to “low capacitance”.

[3] Maximum capacitance value can be exceeded (up to 15 µF), but a sequential turn-on or a slow DACCNF1.SLP setting of the DACs is recommended in this case to avoid overheating.

3.4 Thermal information

Table 6 Thermal resistance

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
Thermal resistance between junction and bottom pad	Rth_B		2.64		K/W	
Thermal resistance between junction and package top	Rth_T		35.4		K/W	

3.5 Electrical characteristics

3.5.1 Gate biasing

Table 7 Electrical characteristics of gate biasing [2,3]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
GATE BIASING DAC						
DAC resolution	RES_{DAC}		12		bits	
DAC full-scale range “low”	FSR_{low}		3.5		V	Referred to VREF_x, RNG=’0’ [1]
DAC full-scale range “high”	FSR_{high}		7		V	Referred to VREF_x, RNG=’1’ [1]
DAC gain error	Eg_{DAC}	-3		+3	%FSR	
DAC differential non-linearity	DNL_{DAC}	-1.0		1.5	LSB	Monotonic
DAC temperature stability	dV_{DAC}/dT			0.3	mV/K	
DAC source current	I_{src}	10			mA	Current flowing out of pins, DAC_xy < VDDA_x – 0.2V [1]
DAC source current “high”	$I_{src,hi}$	50			mA	Current flowing out of pins, high current mode enabled, DAC_xy < VDDA_x – 1.0V [1]
DAC sink current	I_{snk}	8			mA	Current flowing into pins, DAC_xy > VREF_x + 0.7V [1]
DAC sink current “high”	$I_{snk,hi}$	20			mA	Current flowing into pins, high current mode enabled, DAC_xy > VREF_x + 1.0V [1]
DAC source current limitation	$I_{src,lim}$		20		mA	Current flowing out of pins, DAC_xy < VDDA_x – 0.2V [1]
DAC source current limitation, “high”	$I_{src,lim,hi}$		70		mA	Current flowing out of pins, high current mode enabled, DAC_xy < VDDA_x – 1.0V [1]
DAC sink current limitation	$I_{snk,lim}$		13		mA	Current flowing into pins, DAC_xy > VREF_x + 0.7V [1]
DAC sink current limitation, “high”	$I_{snk,lim,hi}$		30		mA	Current flowing into pins, high current mode enabled, DAC_xy > VREF_x + 1.0V [1]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
DAC static load regulation	dV_{DAC}/dI_{DAC}	0.0	0.7	1.9	mV/ mA	VREF_x + 1V < V_{DAC} < VDDA_x - 1V [1]
BIAS SWITCHES						
OUT transmission resistance	R_{trans}		3.5	5	Ω	OUT_xy is connected to DAC_xy, DAC_xy > VREF_x + 1.5V, I_{DC} = 10mA [1]
OUT transmission resistance variation over Temperature	dR_{trans} /dT			12	mΩ/ K	OUT_xy is connected to DAC_xy, DAC_xy > VREF_x + 1.5V, I_{DC} = 10mA [1]
OUT clamping resistance	R_{clamp}			15	Ω	OUT_xy is connected to VREF_x, I_{DC} = 10mA [1]
OUT transient peak current	$I_{OUT,peak}$	-200		200	mA	for pulses shorter than 100 ns
CLAMP DAC						
CLMP DAC resolution	RES_{CLMP}		6		bit	
CLMP DAC full scale range	FSR_{CLMP}		1.4175		V	referred to DAC_x0(2) [1]
CLMP DAC LSB size	LSB_{CLMP}		22.5		mV	
CLMP DAC gain error	Eg_{CLMP}	-5		5	%FSR	I_{OUT_xy} = 0mA [1]
CLMP DAC sink current	$I_{CLMPsnk}$			30	mA	OUT_xy > VREF_x + 1.5V [1]
CLMP DAC current limitation	$I_{CLMPsnk,lim}$		50		mA	
CLMP DAC static load regulation	dV_{CLMP}/ dI_{CLMP}			15	mV/ mA	EN_OUT_x = 0, $I_{OUT,snk}$=0…20mA, OUT_xy > VREF_x + 1.5V [1]

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] All voltages are with respect to GND=0V unless otherwise noted.

[3] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.2 Supply monitoring

Table 8 Electrical characteristics of supply monitoring [2,3]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
VDD UVLO release	$UVLO_{VDD,rel}$	2.6	2.8	3	V	
VDD UVLO lock	$UVLO_{VDD,lck}$	2.5	2.7	2.9	V	
VDD UVLO hysteresis	$UVLO_{VDD,hys}$		100		mV	
VDDA_x-VREF_x UVLO release [1]	$UVLO_{VDDA-VREF,rel}$	2.6	2.8	3	V	
VDDA_x-VREF_x UVLO lock [1]	$UVLO_{VDDA-VREF,lck}$	2.5	2.7	2.9	V	
VDDA_x-VREF_x UVLO hysteresis [1]	$UVLO_{VDDA-VREF,hys}$		100		mV	
VDDP UVLO release	$UVLO_{VDDP,rel}$	1.50	1.55	1.60	V	

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
VDDP UVLO lock	$UVLO_{VDDP,lck}$	1.45	1.50	1.55	V	
VDDP UVLO hysteresis	$UVLO_{VDDP,hys}$	30	50	70	mV	

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] All voltages are with respect to GND=0V unless otherwise noted.

[3] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.3 Temperature sensor

Table 9 Electrical characteristics of temperature sensor [1]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
DTS resolution	RES_{DTS}		9		bits	
DTS measurement range	RNG_{DTS}	-40		160	°C	
DTS absolute error	E_{DTS}	-2.5		2.5	°C	

[1] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.4 Voltage ADC

Table 10 Electrical characteristics of VADC [2,3]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
VADC resolution	RES_{VADC}		11		bit	
VADC full-scale range ADC0/1	$FSR_{VADC,ADC}$		3		V	
VADC full-scale range ISNS_x+[1]	$FSR_{VADC,ISNS}$		60		V	
VADC differential non-linearity	DNL_{VADC}	-1		2	LSB11	
VADC gain error ADC0/1	$Eg_{VADC,ADC}$			2	%	
VADC gain error ISNS_x+[1]	$Eg_{VADC,ISNS}$			2.5	%	
VADC offset error	Eo_{VADC}	-3		3	LSB11	

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] All voltages are with respect to GND=0V unless otherwise noted.

[3] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.5 Current shunt ADC

Table 11 Electrical characteristics of CSA [2,3]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
CSA resolution	RES_{CSA}		12		bit	
CSA input range 0	$RNG_{CSA,rng0}$		15		mV	ADCEN.ISNS_x_RNG=000_b [1]
CSA LSB size range 0	$LSB_{CSA,rng0}$		9.4		µV	ADCEN.ISNS_x_RNG=000_b [1]
CSA input range 1	$RNG_{CSA,rng1}$		30		mV	ADCEN.ISNS_x_RNG=001_b [1]
CSA LSB size range 1	$LSB_{CSA,rng1}$		18.8		µV	ADCEN.ISNS_x_RNG=001_b [1]
CSA input range 2	$RNG_{CSA,rng2}$		60		mV	ADCEN.ISNS_x_RNG=010_b [1]
CSA LSB size range 2	$LSB_{CSA,rng2}$		37.6		µV	ADCEN.ISNS_x_RNG=010_b [1]
CSA input range 3	$RNG_{CSA,rng3}$		120		mV	ADCEN.ISNS_x_RNG=011_b [1]
CSA LSB size range 3	$LSB_{CSA,rng3}$		75.2		µV	ADCEN.ISNS_x_RNG=011_b [1]
CSA input range 4	$RNG_{CSA,rng4}$		240		mV	ADCEN.ISNS_x_RNG≥100_b [1]
CSA LSB size range 4	$LSB_{CSA,rng4}$		150.4		µV	ADCEN.ISNS_x_RNG≥100_b [1]
CSA sample rate	SR_{CSA}		20		kS/s	
SNDR input ranges 0 and 1	$SNDR_{0/1}$	50			dB	ADCEN.ISNS_x_RNG=000_b / ADCEN.ISNS_x_RNG=001_b [1]
SNDR input ranges 2 and 3	$SNDR_{2/3}$	56			dB	ADCEN.ISNS_x_RNG=010_b / ADCEN.ISNS_x_RNG=011_b [1]
SNDR input range 4	$SNDR_4$	62			dB	ADCEN.ISNS_x_RNG=100_b [1]

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] All voltages are with respect to GND=0V unless otherwise noted.

[3] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.6 Timing parameters

Table 12 Timing parameters [2]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
Rampup time				180	µs	RSTN is tied to VDDP, VDD and VDDP are above UVLO threshold. Time until interface is ready to accept commands
Startup time	t_{start}			10	µs	RSTN transision from 0 to 1 until interface is ready to accept commands
BIAS SWITCHES						

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
OUT propagation delay clamping	t_{clamp}			300	ns	C_{OUT}=0nF, time measured from OUT_EN_x change until 10% of final value [1]
OUT propagation delay enable	$t_{prop,en}$			300	ns	C_{OUT}=0nF, time measured from OUT_EN_x change until 10% of final value [1]
ADC						
VADC startup time	$t_{VADC,start}$	35	47	59	µs	from VADC_EN=1 until first result (I_ISNS_A) is available
VADC round robin time	$t_{VADC,round}$	17	23	29	µs	Full conversion cycle of all 10 channels
CSA						
CSA startup time	$t_{CSA,start}$	43	57	71	µs	
CSA conversion time	$t_{CSA,conv}$	38.4	51.2	64.0	µs	
DTS						
DTS Startup Time	$t_{DTS,start}$	3.15	4.2	5.25	ms	
DTS Conversion Time	$t_{DTS,conv}$	3	4	5	ms	

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.7 Current consumption

Table 13 Current consumption [1]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
VDD current consumption, in RESET	$I_{VDD,reset}$		200		µA	RSTN pin = ‘0’
VDD current consumption, in ACTIVE	$I_{VDD,active}$		4	7	mA	RSTN pin = ‘1’, VADC and CSA enabled, all DACs enabled, no DC loads at DAC outputs
VDDA / VREF current consumption, in RESET	$I_{VDDA,reset}$		300		µA	RSTN pin = ‘0’; per one side
VDDA / VREF current consumption, in RESET	$I_{VDDA,active}$		4		mA	RSTN pin = ‘1’, VADC and CSA enabled, all DACs enabled, no DC loads at DAC outputs; per one side
VDDP current consumption	I_{VDDP}		1		mA	Depending on communication traffic

[1] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.8 Digital logic

Table 14 Logic levels [1,2]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
High-level input voltage	V_{IH}		2.5		V	VDDP = 3.3 V
Low-level input voltage	V_{IL}		1		V	VDDP = 3.3 V
High-level input voltage	V_{IH}		1.85		V	VDDP = 2.5 V
Low-level input voltage	V_{IL}		0.8		V	VDDP = 2.5 V
High-level input voltage	V_{IH}		1.15		V	VDDP = 1.8 V
Low-level input voltage	V_{IL}		0.65		V	VDDP = 1.8 V

[1] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

[2] All voltages are with respect to GND=0V unless otherwise noted.

4 Reset behavior and power-on/off sequences

4.1 State: RESET

At power-up, in the event of RSTN input “low”, or in the event of any supply getting out of range, the BGMC1210 state machine is placed in a RESET state:

- All registers are reset to their initial values (asynchronous)
- Analog infrastructure for DAC is powered up to ensure safe output voltages and fast startup (controlled by UV-comparators)
- DAC_xy outputs are set to VREF_x by default register settings and are pulled down to VREF_x with internal resistors
- OUT_xy outputs are switched to VREF_x
- All ADCs are disabled
- No communication possible
- OUT_xy Pins switched to VREF_x (clamped)

4.2 State: ACTIVE

After RSTN input “high” and if main supplies (VDD, VDDP and internal supplies) are ready and within range, the BGMC1210 state machine finds itself in an ACTIVE state:

- I3C device ID is read and latched
- All registers are transparent towards the analog part: a changed register contents will have immediate effect on the output
- The ADCs are operating (if enabled) and results can be fetched from registers

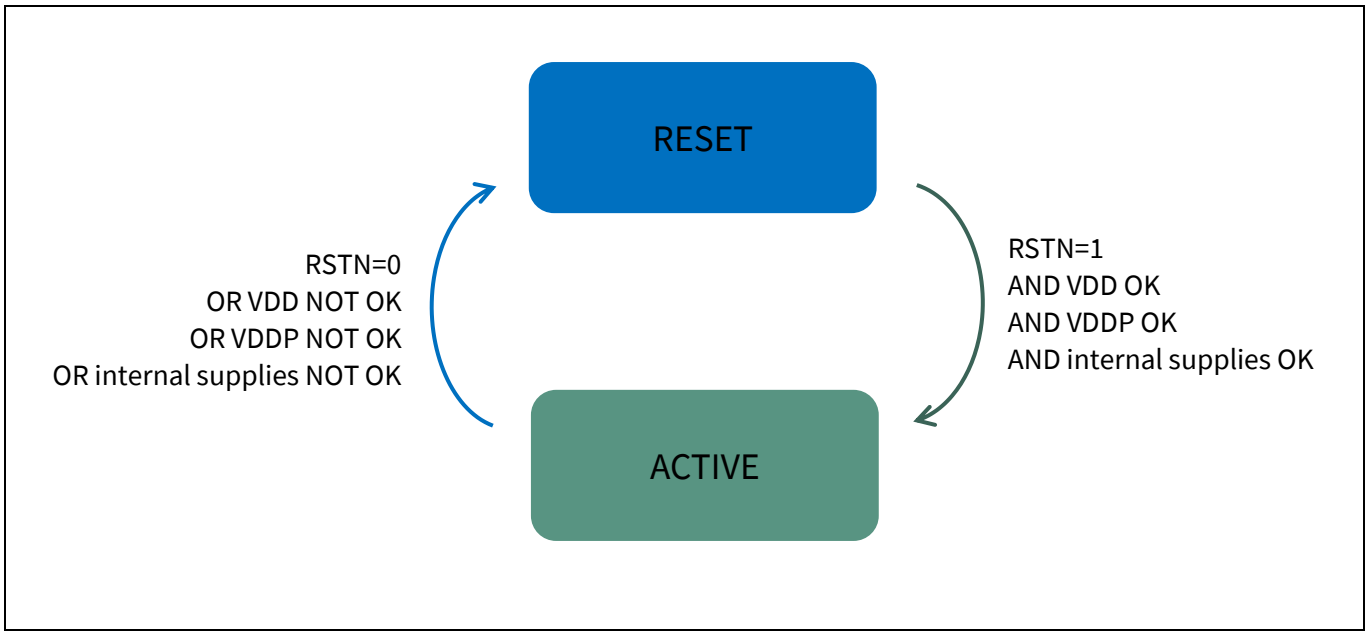

Figure 4 BGMC1210 state diagram

4.3 Power-on sequence

Recommended power-on sequence:

1. Keep RSTN low (RSTN =0);
2. Turn-on VREF_A, VREF_B, VDD, VDDP, VDDA_A, VDDA_B (no specific sequence required);
3. Set RSTN high (RSTN=1);
4. Program registers:
   - programmed registers will have immediate effect on analog periphery;
   - ADCs can be fetched (if enabled);
5. PA transistor gate voltages at OUT_A0(2), OUT_B0(2), DAC_A1(3), DAC_B1(3) can be enabled;
6. PA transistors Vdd supply can be enabled.

4.4 Power-off sequence

Recommended power-off sequence:

1. If necessary, set gate voltages at DAC_A1(3), DAC_B1(3) to pinchoff or lower;
2. Set transistor gate voltages at OUT_A0(2), OUT_B0(2) to clamping or lower;
3. Disable PA transistors Vdd supply;
4. Set RSTN low (RSTN =0);
5. Turn-off VREF_A, VREF_B, VDD, VDDP, VDDA_A, VDDA_B (no specific sequence required).

5 DAC and Bias Switches

5.1 DAC configuration

The BGMC1210 IC offers 2 independent groups of outputs A and B, each consisting of 4 DACs with separate supply domain per group. Block diagram of one such DAC group is shown on Figure 5 (half is shown for clarity reasons). 2 of the DACs (DAC_x0(2)) are connected to OUT_x0(2) outputs via gate biasing switches for TDD support. Every DAC has a 12 bit resolution, internal reference voltage and can be adjusted in range and offset. Supply range per DAC group is defined by reference potential VREF_x and supply input VDDA_x: (VDDA_x - VREF_x). Supply can be selected in voltage range from -8…0V up to 0…8V, so that enhancement type LDMOS transistors as well as depletion type GaN transistors are supported.
To reduce traffic on the digital control interface it is possible to enable temperature compensation via a look-up table and/or enable tracking of the DAC used for peak device to the DAC used for main device.
Additional features include DAC clamping compensation, a dedicated internal clamping buffer and a possibility to use neighboring DAC as a clamping potential.

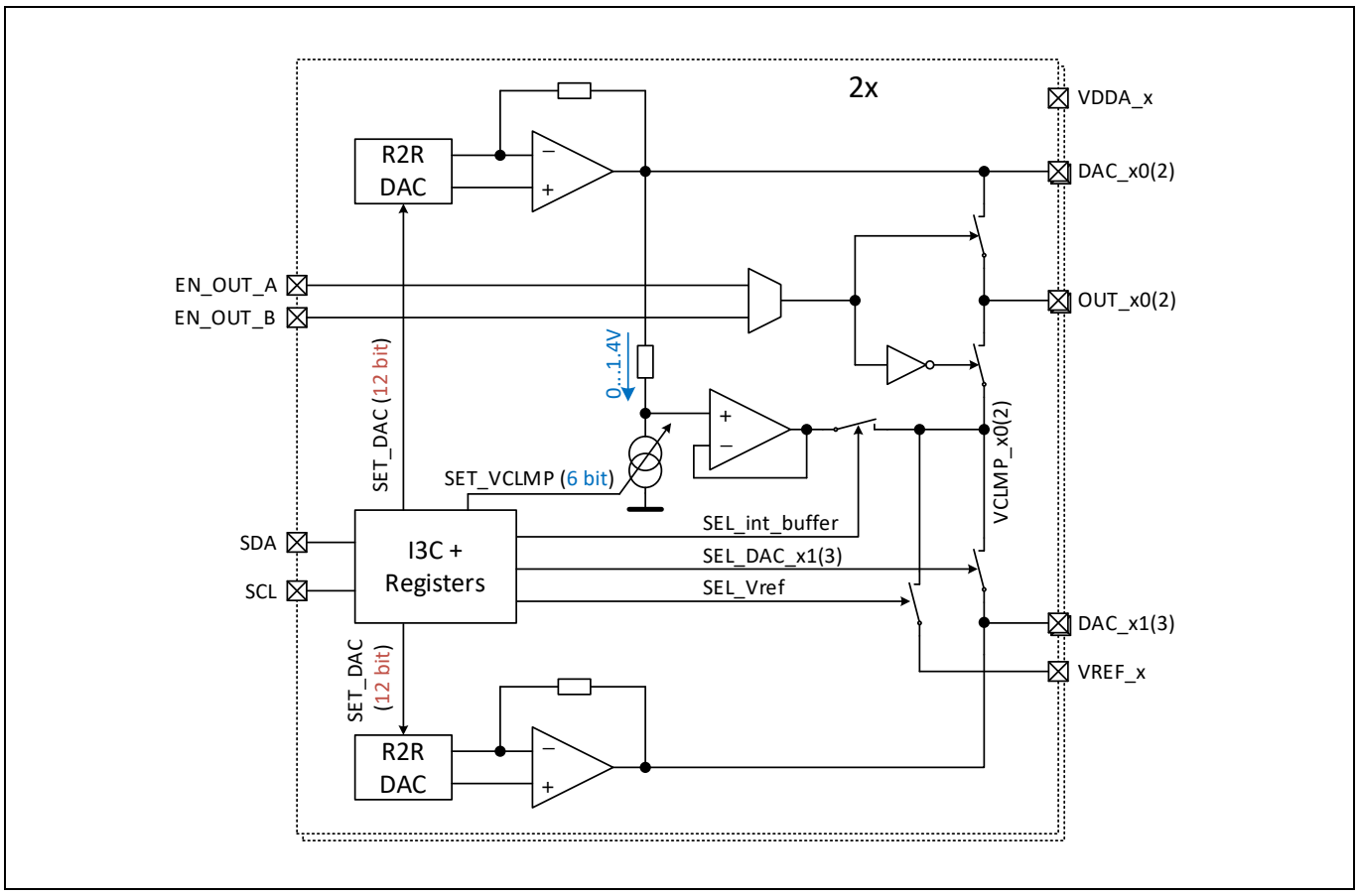

Figure 5 DAC and Bias Switches

Clamping potential VCLMP

During reset and after startup the clamping potential of the biasing switches (VCLMP_x0(2)) is connected to VREF_x input. Alternative clamping voltages can be selected with the configuration register VCLMP_x.SEL_xy:

- SEL_xy = 00_b: VCLMP_xy = Vref
- SEL_xy = 01_b: VCLMP_xy = DAC_x1(3)
- SEL_xy = 10_b or 11_b: VCLMP_xy = Buffer

DAC used as VCLMP

The neighboring DAC can be used as VCLMP: in case of DAC_x0, DAC_x1 would define clamping potential; in case of DAC_x2 it would be DAC_x3. The voltage at these DACs (DAC_x1(3)) can either be set to a fixed value or configured as a relative offset to the main DAC (tracking: DACCNF1.TRK_* = 1_b).
As VCLMP must not become higher than the DAC voltages, all range and offset settings for DAC_x1(3) will be ignored in such case and the settings from DAC_x0(2) will be used (see 5.3).

Internal Buffer used as VCLMP

Another alternative for lower current loads is an internal buffer with a 6-bit DAC, which is tracking the main DAC_x0(2). The voltage difference towards the main DAC can be set via the register VCLMP_x.DVAL_xy - a low value relates to a small delta-voltage, a large value to a large delta-voltage below DAC_x0(2). This option offers independent internal clamping potentials without sacrificing neighboring DAC.

In order to set the necessary clamping voltage below DAC_x0(2) voltage:

$$V_{CLMP_xy} = V_{DAC_xy} - V_{delta},$$

The following value needs to be written to VCLMP_x.DVAL_xy register entry:

$$DVAL_xy = V_{delta} / LSB_{CLMP}, \quad (1)$$

where:
V_{delta} = [0…1.4175 V]– the necessary difference in bias voltage below DAC_xy nominal voltage for clamping mode;
LSB_{CLMP} = 22.5mV – clamping DAC LSB.

5.2 DAC value computation

Depending on the configured offset voltage and range, the DAC value to be written in DAC_xy.VALUE is defined as follows:

$$VALUE = \frac{V_{OUT} - V_{OFFSET}}{\frac{RANGE}{2^{12}}}, \quad (2)$$

where:

V_{OUT} is desired output voltage referred to Vref_x;
$RANGE$ is configurable DAC output range defined by DAC_xy.RNG bits: $RANGE$ = [3.5V; 7V];
V_{OFFSET} is configurable offset voltage defined by DAC_xy.OFFS bits: V_{OFFSET} = [0V; 0.5V; 1.5V; 3V] for 3.5V DAC output range, V_{OFFSET} = [0V; 1V] for 7V DAC output range;
x = [A; B], y = [0; 1; 2; 3].

The even DAC_x0(2) values are directly controlled by the DAC_x0.VALUE and DAC_x2.VALUE register entries and can be optionally modified by several adjustment blocks before being applied to the DAC input (as shown on Figure 6): Temperature Compensation, Slope and Limitation, and Clamp Compensation that can temporarily change the output as well.

The odd DAC_x1(3) values can be configured to track the even DAC_x0(2) with DACCNF1.TRK_x1(3)tox0(2) = 1 (Range and Offset are adjusted to the even DAC). This arrangement is possible for the pairs of DAC_x0 & DAC_x1 and DAC_x2 & DAC_x3. The odd DAC values can also be modified by the Temperature Compensation and the Slope and Limitation blocks.

A special function of the odd DACs (DAC_x1 and DAC_x3) is the possibility to work as Clamping Voltage (VCLMP) for the bias switches (VCLMP_x.SEL_x0(2)='01'). In this mode all range and offset values of the even DAC

(DAC_x0(2)) is set to equal (see 5.3) and the maximum value is limited to the even DAC value. Please refer to section 11.3 for more details.

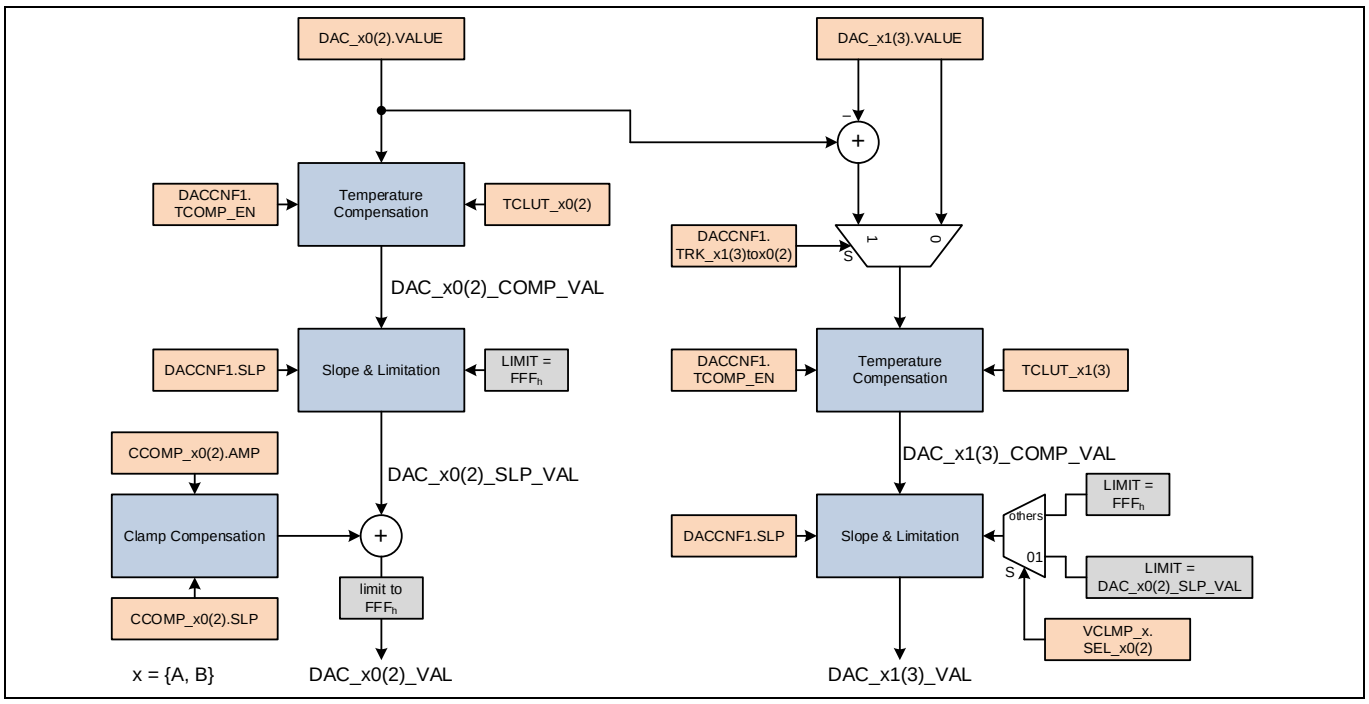

Figure 6 DAC value computation

5.3 DAC settings in tracking and clamping modes

If the odd DAC is configured to track the even DAC (DACCNF1.TRK_x1(3)tox0(2)) or it's selected as clamping voltage for the even DAC (VCLMP_x.SEL_x = "01") the range and offset settings will be taken from the even registers (DAC_x0(2).RNG, DAC_x0(2).OFFS). This is needed for linear tracking and proper limitation.

In case the odd DAC is acting as clamping voltage, the signal to enable the odd DAC (dac_x1(3)_en_o) is forced to '1' (the even enable signals dac_x0(2)_en are not affected) - the register field DAC_x1(3).EN is not affected.

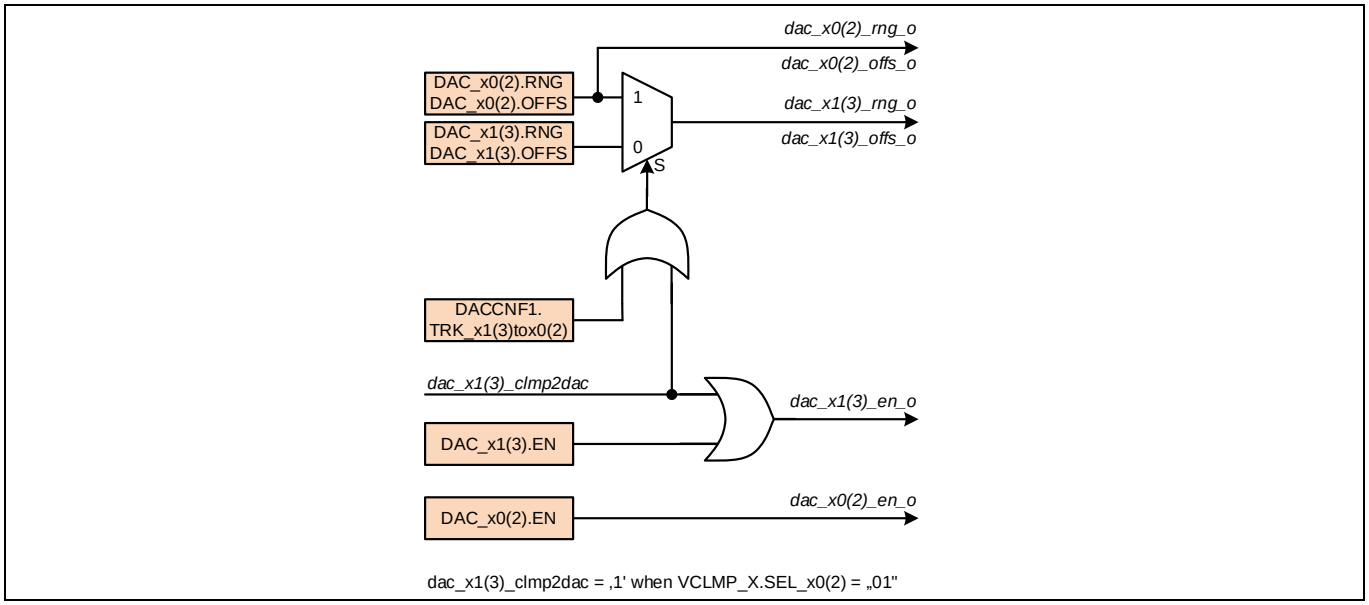

Figure 7 Odd DAC_x1(3) settings in tracking/clamping modes

5.4 DAC temperature compensation

The BGMC1210 IC is offering a Look-Up Table (LUT), in which a temperature coefficient for the Gate Voltage can be configured. Depending on the temperature measured by the DTS a delta (ΔV_g) to the reference value (at room temperature) is calculated and provided to the DAC. In total 8 interpolation points ($\Delta V_{ref,0...7}$ in Figure 8) are available, the gradients ($grad_{0...7}$) from one point to the next one are defined by the LUT.

To enable the built-in Gate Voltage temperature compensation the TCOMP_EN bit of DACCNF register needs to be set to 1. The LUTs in the register map hold a series of gradients between predefined points on the compensated gate-voltage/temperature curve for each DAC. These gradients are used to approximate the curve using piecewise linear interpolation and are stored in TCLUT_xy_L/H registers (x=[A, B]; y=[0,1,2,3]). The module's single datapath computes one linear interpolation segment at a time, according to following equations.

DAC_xy.RNG = 0_b:

$$\Delta V = \frac{\Delta V_{ref} + (-1)^{negate_gradient} \cdot grad \cdot \Delta T}{4} \quad (3)$$

DAC_xy.RNG = 1_b:

$$\Delta V = \frac{\Delta V_{ref} + (-1)^{negate_gradient} \cdot grad \cdot \Delta T}{8} \quad (4)$$

Please refer to section 11.4 for more details.

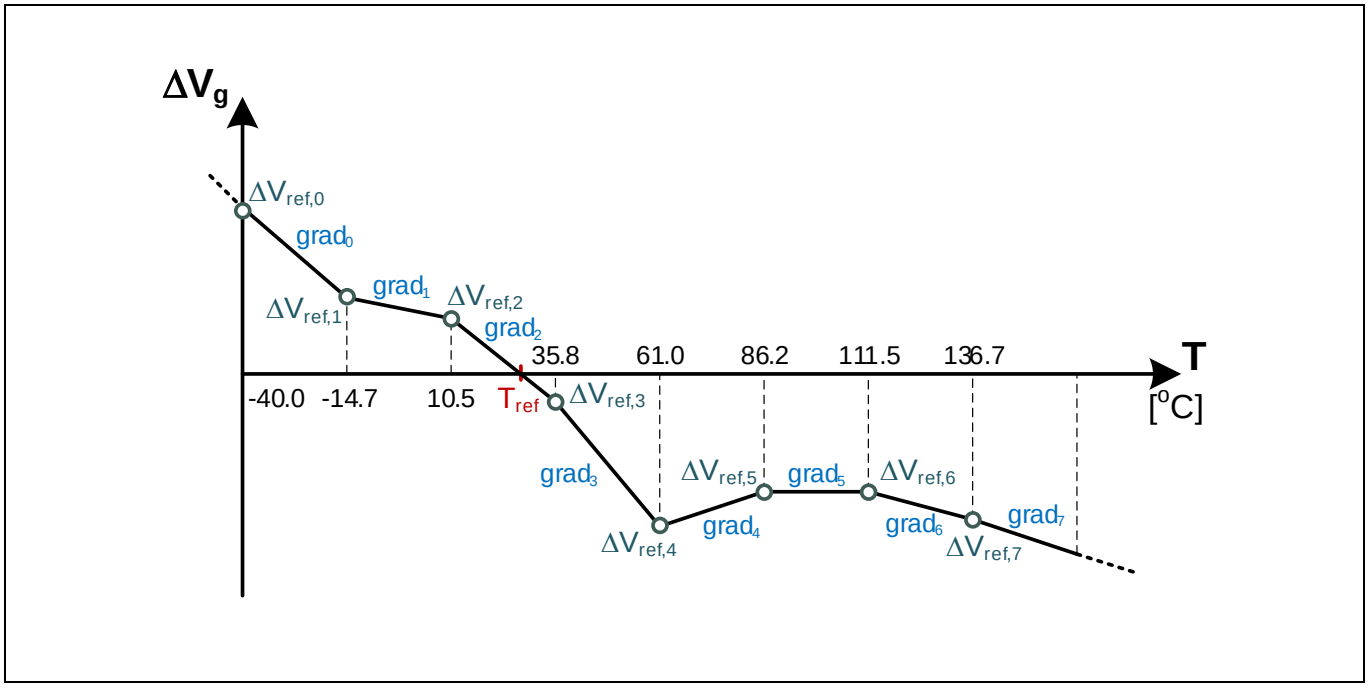

Figure 8 Coefficients in LUT for temperature compensation

5.5 DAC slope and limitation

The DAC values coming from the registers and Temperature Compensation are reduced to the limitation defined by a LIMIT before they are increased/decreased bit by bit with an update rate configured in DACCNF1.SLP.
For a smooth turn-on at the first power-up the ramp starts at lowest output voltage, the default value of DAC_x_VAL is 000_h.
The testmode bit TMDAC.DAC_A0_4ALL propagates the DAC_A0_VAL to all other DACs - also to side B.

DAC and Bias Switches

Configuration for update rate (1 code per time step defined in DACCNF1.SLP):
- 000_b: 50 ns
- 001_b: 1 µs
- 010_b: 5 µs
- 011_b: 10 µs
- 100_b: 100 µs
- 101_b: 250 µs
- 110_b: 1 ms
- 111_b: 4 ms (DTS update rate)

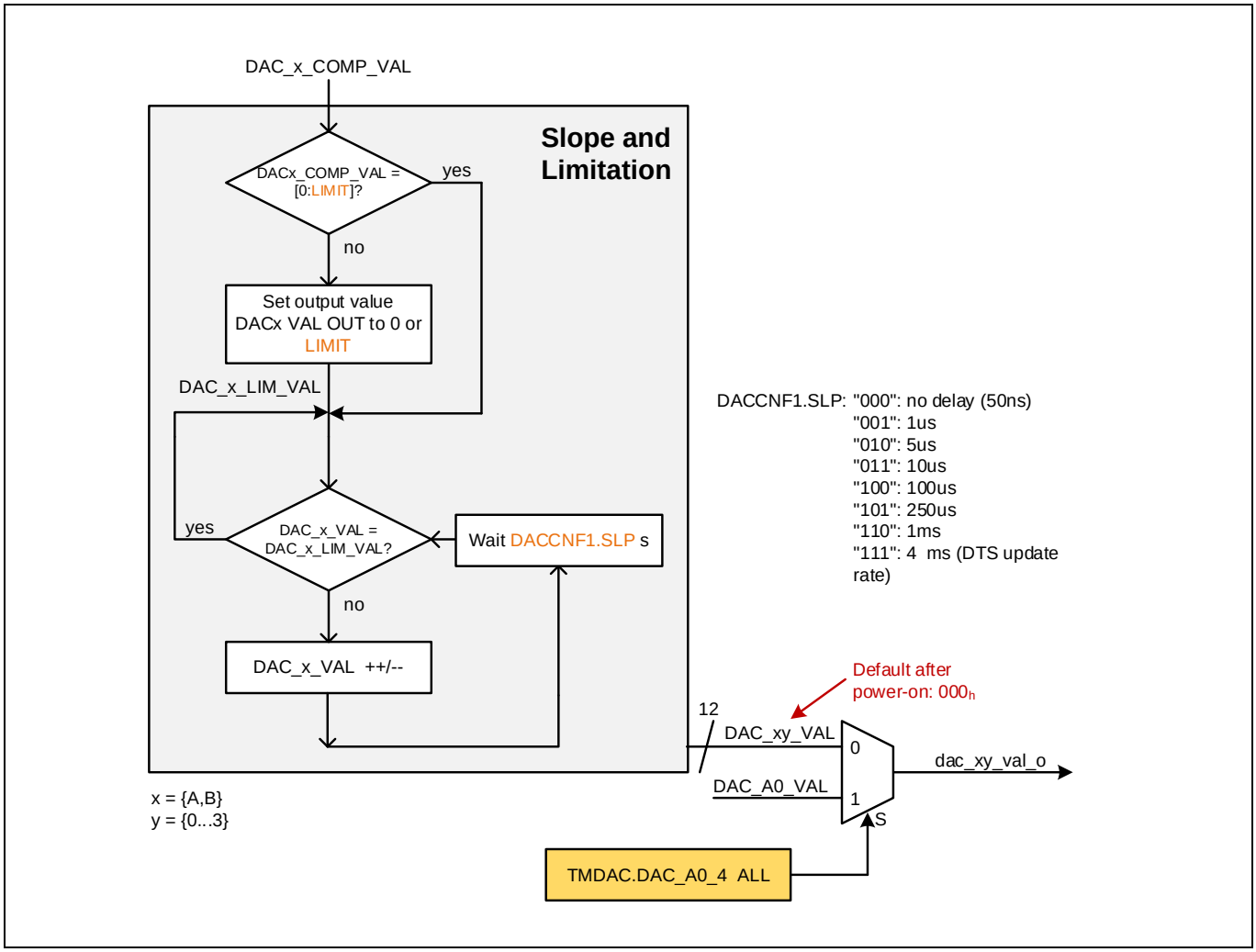

Figure 9 DAC slope and limitation

5.6 DAC clamping compensation

The DAC outputs to which the bias switches are connected (DAC_x0 and DAC_x2) can be configured to compensate for effects coming from a re-turn on of the external transistors. Possible effects are:
- Too small capacitor at DAC_xy
- Too high load at OUT_xy
- Thermal settling effects
- Trapping effects in GaN devices
- etc.

DAC and Bias Switches

As countermeasure the device can temporarily increase the output voltage at the DAC_xy pins, depending on the state of EN_OUT_x (to enable this feature CCOMP_xy.EN =1, where x=[A;B], y=[0;2]):

• While EN_OUT_x is low, the output voltage at DAC_xy is incremented with a fast transition (1 step per 50ns) up to an amplitude defined in CCOMP.AMP (delta value to DAC_xy.VALUE).
• After detecting a rising edge at EN_OUT_x, the output DAC_xy is decremented again down to its initial value (delta value = 0) with a transition defined in CCOMP.SLP (1 step per CCOMP.SLP * 1us).
- In case CCOMP.SLP = 00h, there will be just a minimum delay (50ns) between the steps counting down.
• In case the decrement is interrupted by another falling event at EN_OUT_x, the DAC_xy output is immediately incremented to the desired AMP.

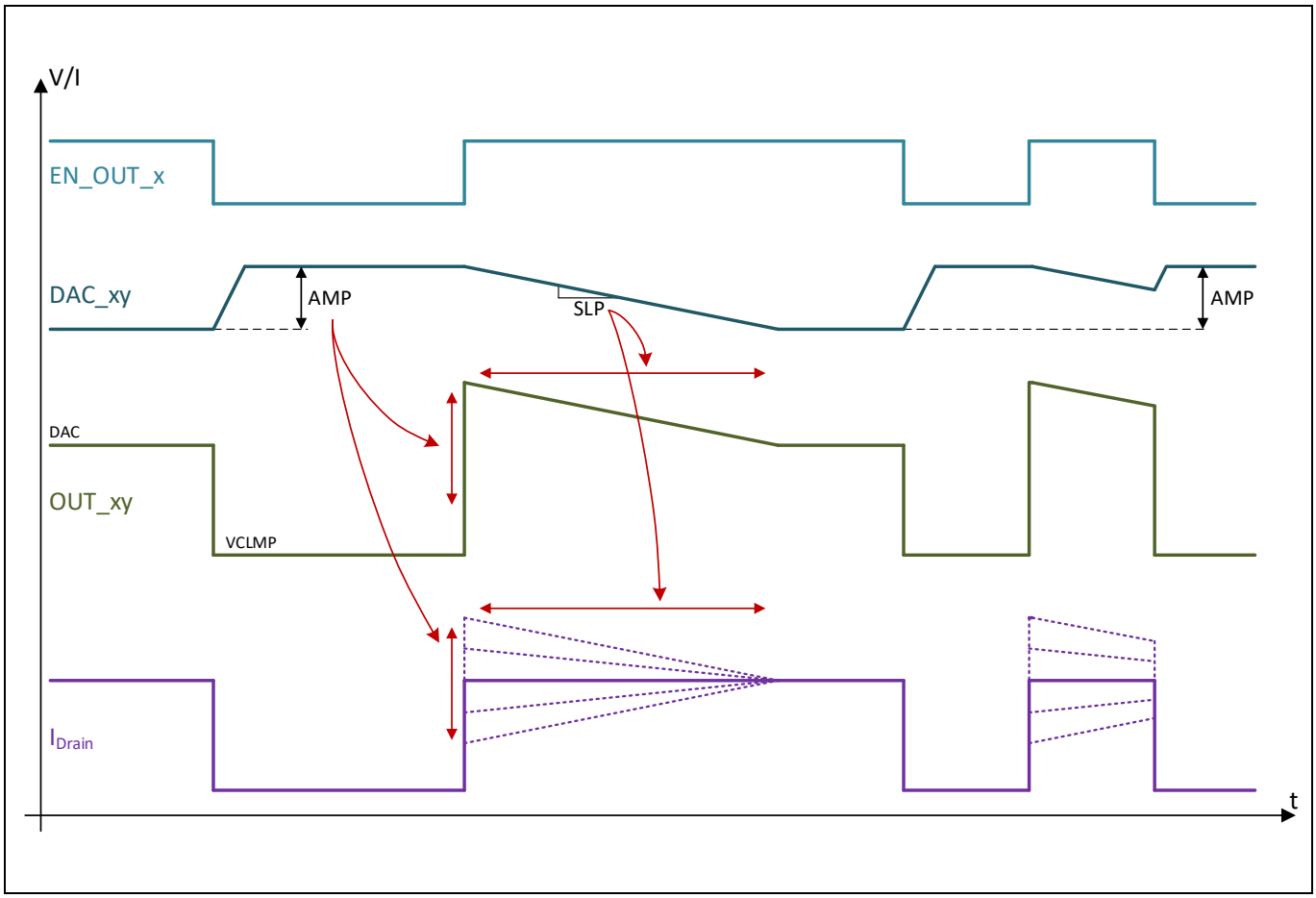

Figure 10 DAC clamping compensation

5.7 DAC feedback

The IC is offering a digital feedback of the calculated DAC value, which can be read out via the digital interface. This is done with the register DAC_FB.

Address: **$0F_h$**

Name: **DAC_FB**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES	DAC SIDE	DAC_CH		VALUE (read only)											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

With a write command the DAC_SIDE (0 for side A, 1 for side B) and the DAC_CH (channel) will be set. The data provided for VALUE will be ignored for the write command.

A consecutive read command will return the actual calculated DAC-value (DAC_xy_VAL) as well as the selected DAC side + channel.

This value will be updated at the time, the I3C read command is issued. If this is happening during a slope, the value read back will be the intermediate one (at the time, the I3C read arrives) and not the final one.

5.8 DAC output range

Figure 11 illustrates the operating range of the DAC output.

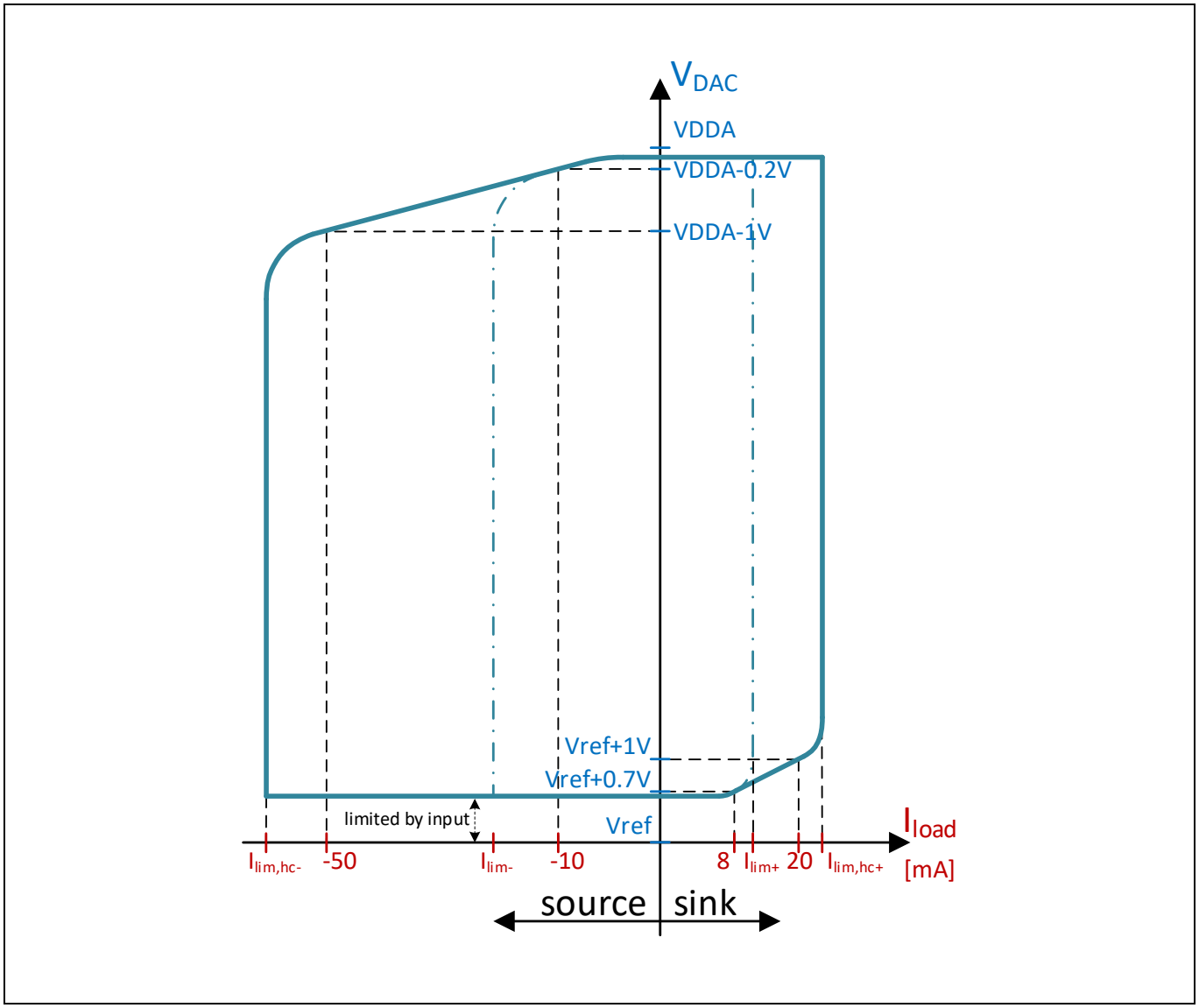

Figure 11 DAC output range

6 Voltage ADC

The Voltage ADC is an 11-bit SAR ADC with several multiplexed inputs:

- ADC0 / ADC1
- ISNS_A+ / ISNS_B+
- Supply inputs VDD / VDDP / VDDA_A / VDDA_B / VREF_A / VREF_B

ADC is operated in round-robin scheme: once it's enabled, inputs are sampled and converted sequentially. The results are stored in corresponding separate registers.

VADC is using internal reference voltage, inputs are referred to GND.

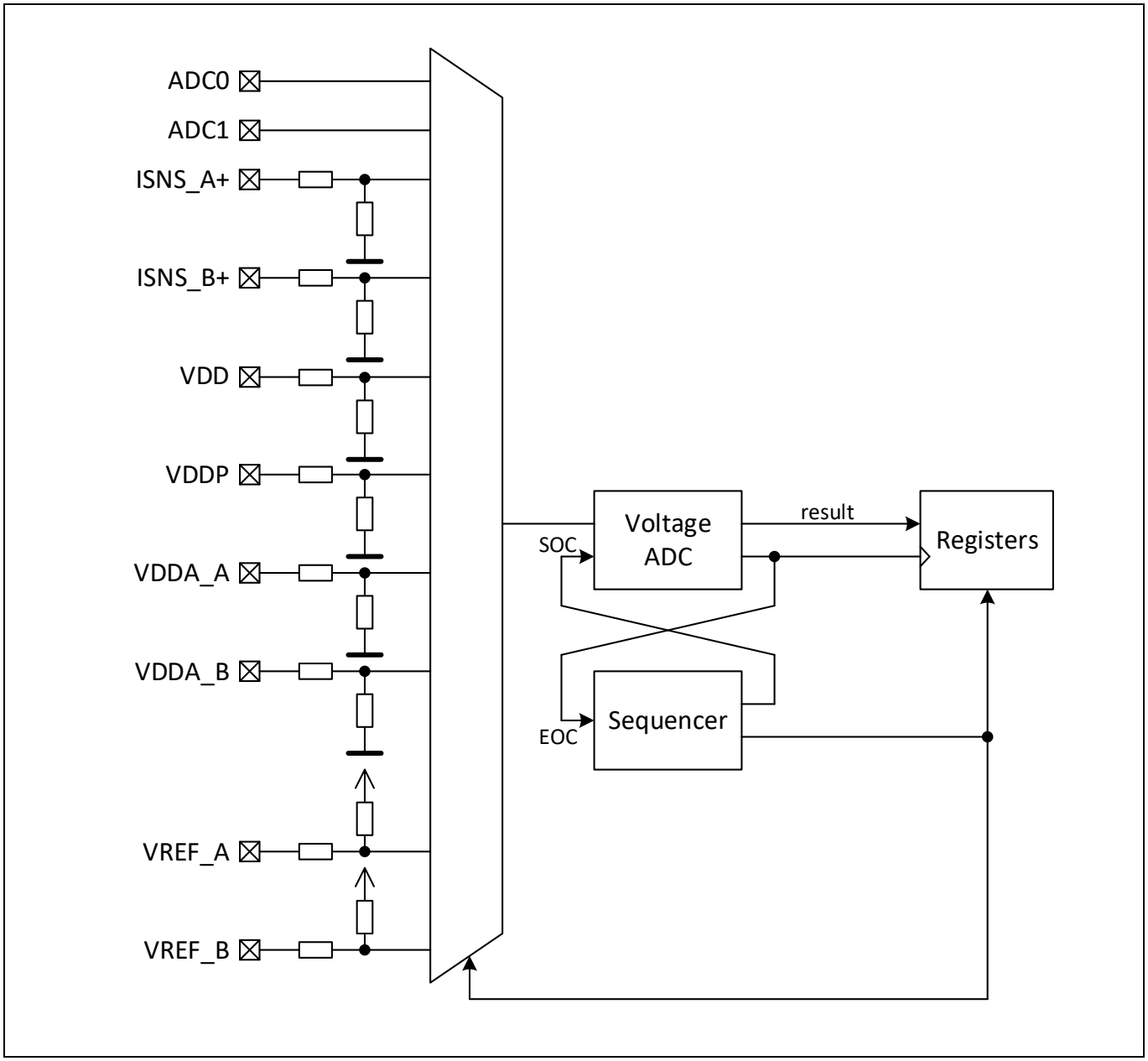

Figure 12 Voltage ADC

Voltage ADC

Table 15 VADC channels

Pin	ADC Channel	Full-Scale	LSB size
ISNS_A+	Ch 0	60.89 V	29.73 mV
ISNS_B+	Ch 1	60.89 V	29.73 mV
ADC0	Ch 2	3.04 V	1.487 mV
ADC1	Ch 3	3.04 V	1.487 mV
VDD	Ch 4	5.69 V	2.78 mV
VDDP	Ch 5	3.69 V	1.805 mV
VDDA_A	Ch 6	8.48 V	4.141 mV
VDDA_B	Ch 7	8.48 V	4.141 mV
VREF_A	Ch 8	-8.4 V	4.1 mV
VREF_B	Ch 9	-8.4 V	4.1 mV

6.1 VADC transfer functions

ISNS:

$$V_{ISNS} = VALUE \cdot 20 \cdot \frac{512}{204} \cdot \frac{V_{ref}}{2^{11}}, \quad (6)$$

ADC0/1:

$$V_{ADC0/1} = VALUE \cdot \frac{512}{204} \cdot \frac{V_{ref}}{2^{11}}, \quad (7)$$

VDD:

$$V_{VDD} = VALUE \cdot \frac{430}{230} \cdot \frac{512}{204} \cdot \frac{V_{ref}}{2^{11}}, \quad (8)$$

VDDP:

$$V_{VDDP} = VALUE \cdot \frac{340}{280} \cdot \frac{512}{204} \cdot \frac{V_{ref}}{2^{11}}, \quad (9)$$

VDDA:

$$V_{VDDA} = VALUE \cdot \frac{390}{140} \cdot \frac{512}{204} \cdot \frac{V_{ref}}{2^{11}}, \quad (10)$$

VREF:

$$V_{VREF} = \left(VALUE \cdot \frac{V_{ref}}{2^{11}} - 1.2\right) \cdot 7, \quad (11)$$

where:

VALUE is contents of one of the corresponding registers (e.g. ADC0.VALUE);

$V_{ref} = 1.213$ V.

7 Current Shunt ADC

The Current Shunt ADC (CSA) is capable of sampling the voltage across an external shunt directly, without the need of a shunt amplifier. The floating input stage enables a fully-differential measurement across the entire common mode input range from 0 V up to 60 V.

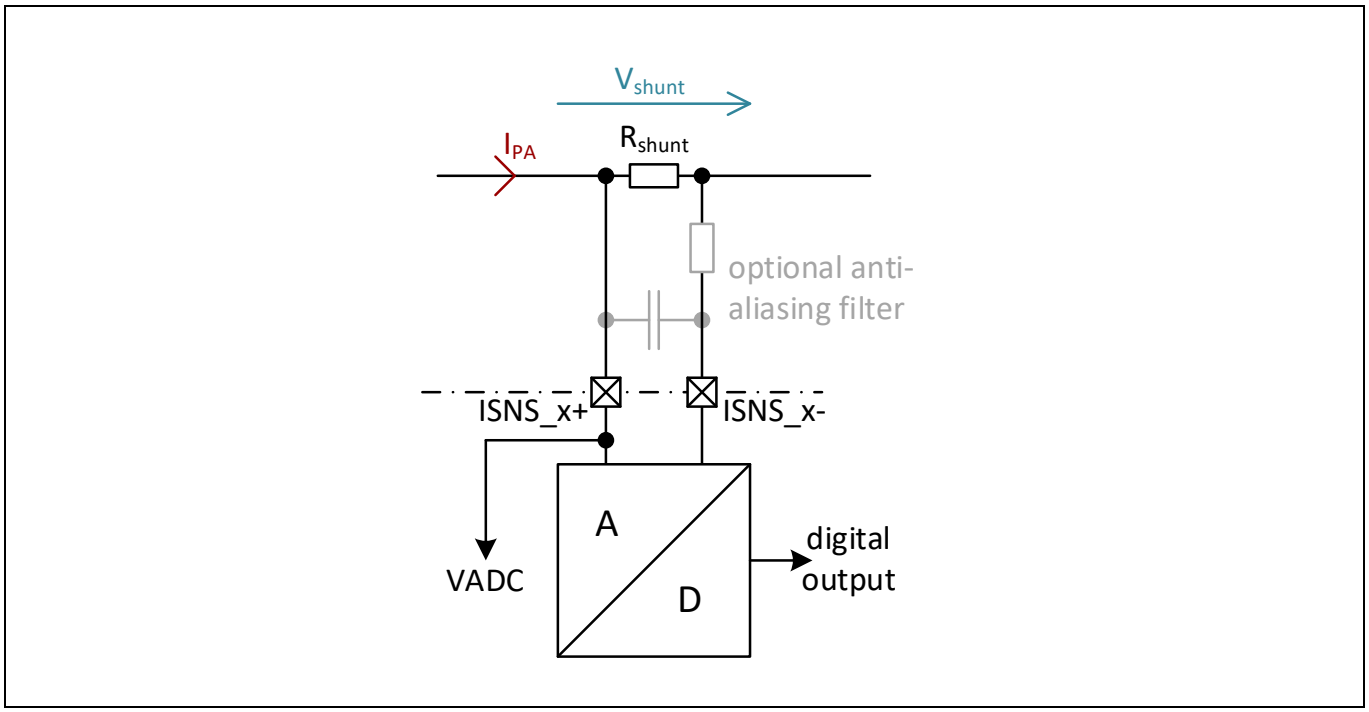

Figure 13 Shunt ADC

For optimal matching to the external shunt different full scales can be programmed - please be aware that due to the architecture of the ADC the theoretical full-scale cannot be used without non-linear distortion.

Table 16 CSA ranges and LSB

Range	-3dB full scale	Theoretical full scale	LSB_{range}
15 mV	±13.6 mV	±19.25 mV	9.4 µV
30 mV	±27.2 mV	±38.5 mV	18.8 µV
60 mV	±54.4 mV	±77 mV	37.6 µV
120 mV	±108.8 mV	±154 mV	75.2 µV
240 mV	±217.6 mV	±308 mV	150.4 µV

7.1 CSA transfer function

$$V_{SNS} = VALUE \cdot LSB_{range}, \quad (5)$$

where:

VALUE is contents of one of the corresponding registers I_ISNS_A.VALUE or I_ISNS_B.VALUE;

LSB_{range} is defined by Table 16.

It's important to note that V_{SNS} result is fully differential and depending on the voltage presented to ISNS pins will return a positive or negative result. Result in the VALUE field in I_ISNS_A and I_ISNS_B registers is provided as signed integer in two's complement format as shown in Table 17 below.

Table 17 I_ISNS_A.VALUE/ I_ISNS_B.VALUE result mapping

	11	10	9	8	7	6	5	4	3	2	1	0
	VALUE											
+FS	0	1	1	1	1	1	1	1	1	1	1	1
…	…	…	…	…	…	…	…	…	…	…	…	…
0	0	0	0	0	0	0	0	0	0	0	0	0
…	…	…	…	…	…	…	…	…	…	…	…	…
-FS	1	0	0	0	0	0	0	0	0	0	0	0

8 Die Temperature Sensor

The IC is equipped with a Die Temperature Sensor (DTS) which is sensing the junction temperature of the IC. In order to reach a high uncalibrated accuracy the sensing concept is based on V_{BG} / V_{diode} and the conversion is done based on a sigma-delta ADC.

8.1 DTS transfer function

Die Temperature can be calculated according to the following transfer function:

$$T = 0.7648 \cdot \mathrm{TEMPERATURE} - 80.497, \quad [°C] \tag{1}$$

where:
TEMPERATURE is the content of corresponding field in TEMP register.

9 I2C/I3C Serial Digital Interface

This device supports I3C communication and therefore is backwards compatible to I2C. The pads of the digital interface use VDDP and connect to the digital core logic. This logic runs on a voltage derived from VDD using a voltage regulator (VREG). Therefore an undervoltage of any of the two voltages makes the interface unavailable.

VDDP is typically chosen to be 1.8V but it can also handle 3.3V. All digital I/Os (ADR0, ADR1, SCL, SDA, RSTn, EN_OUT_A, EN_OUT_B) need to use the same voltage as VDDP.

The I3C-interface of the Bias and Control IC is configured as slave device supporting all modes up to HDR-DDR, ternary symbol modes (HDR-TSL or HDR-TSP) are not supported. This leads to specified data rates up to 25MBit/s. The implementation was done according to MIPI Standard v1.0. Details on the protocol can be found on the MIPI webpage: https://www.mipi.org/specifications/i3c-sensor-specification. In all available modes, the slave interprets the first two bytes of data written to it by the master as the register address. This feature is called 'sub-addressing', and it is not explicitly defined by the MIPI I3C specification. The interface provides backward compatibility with the I2C protocol.

After RSTN release the digital interface will be in I2C mode until the first I3C message is recognized (Dynamic Address assignment). Once the digital interface has switched to I3C mode it will remain in this until it gets reset.

9.1 I2C Address Selection

Each I2C-device requires a unique address at which it can be reached. Each communication to a slave with an invalid address will remain unacknowledged.

This device offers address selection pins ADR0 and ADR1 to choose between addresses ranging from 0x40 to 0x47. The three logic levels are defined as follows:

- low: short to GND
- high: short to VDDP
- open: floating (VDDP/2)

To avoid external components for VDDP/2 internal pull-resistors are connected to the ADR[0:1] pins. They will be active during power-on conditions + 8µs after such a condition. After that time the slave address is fix during normal operation (no power-on reset or reset). Therefore the pull-resistors are disconnected to avoid extra current between VDDP and GND.

The three input states for each pin allow the following addresses to be selected:

Table 18 I2C Device Address truth table

ADR1	ADR0	I2C address ($+40_h$)
low	low	0
low	open	0
low	high	1
open	low	2
open	open	3
open	high	4
high	low	5
high	open	6
high	high	7

In Figure 14 the functional building blocks for the address selection are shown:

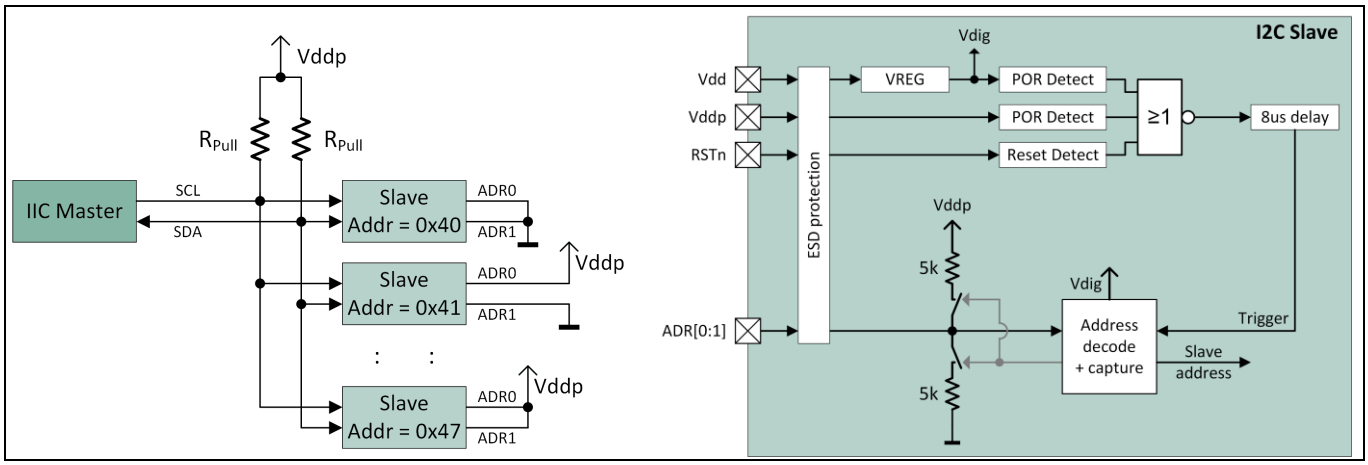

Figure 14 I2C Address Selection

9.2 I2C Design Considerations

For a proper communication it is important that Master and Slave can both drive data reliably. The SCL will only be driven by the Master as this Slave does not support clock stretching etc. Therefore it is possible that the Master drives SCL by a push-pull digital pin (GPO). In case an Open-Drain pin is used a pull-up is required. In the latter case pull-up and the capacity connected to it will be the only design factor to consider. This is described for the SDA pin in greater details.

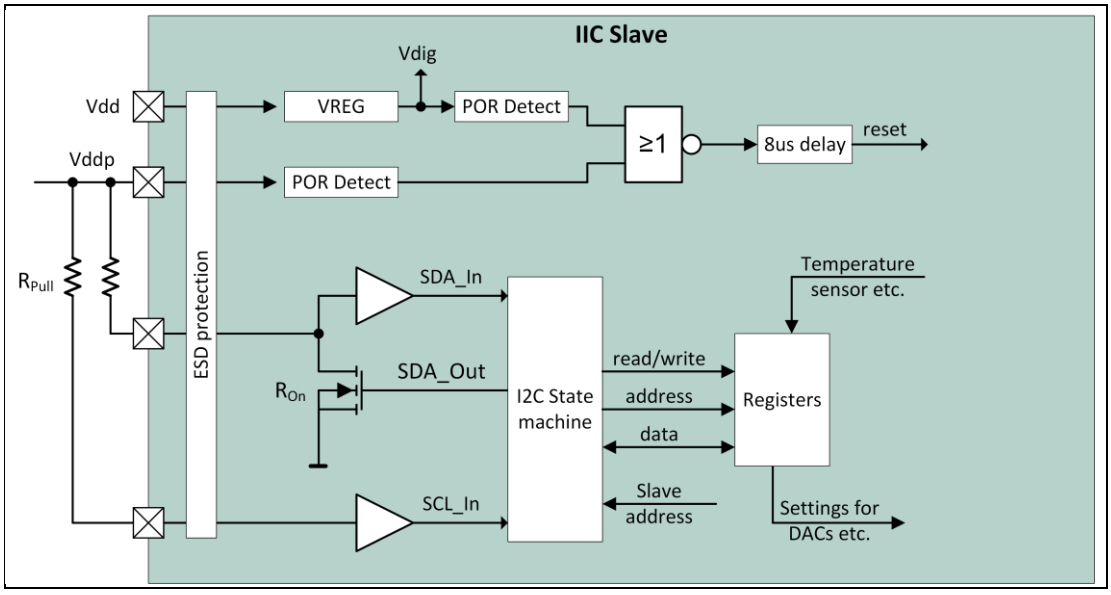

Figure 15 I2C Structure

The SDA pin is bi-directional which means it can be driven either by the Master or by the Slave. When handing over the driving authority from one to the other spikes and dips may occur on the SDA line. Such a handover happens when e.g. a Slave needs to acknowledge a byte sent by the Master. The SDA line is expected to change during the SCL low phase and remain stable during SCL high phase (see **Figure 16** green area). Additionally there is a spike filter that anyway will swallow pulses smaller than 60ns. Still care should be taken to avoid excessive crosstalk between SCL and SDA.

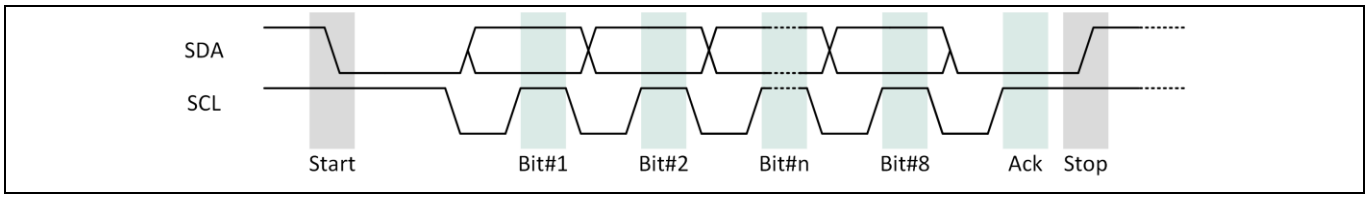

Figure 16 I2C Sample Phase

When data is sent on the SDA line the driver must be strong enough to drive a valid low as well as releasing the line in time to allow the external pull-up resistor to pull high. All capacitance connected to the line, the inner driver strength as well as the pull-up resistor need to be considered:

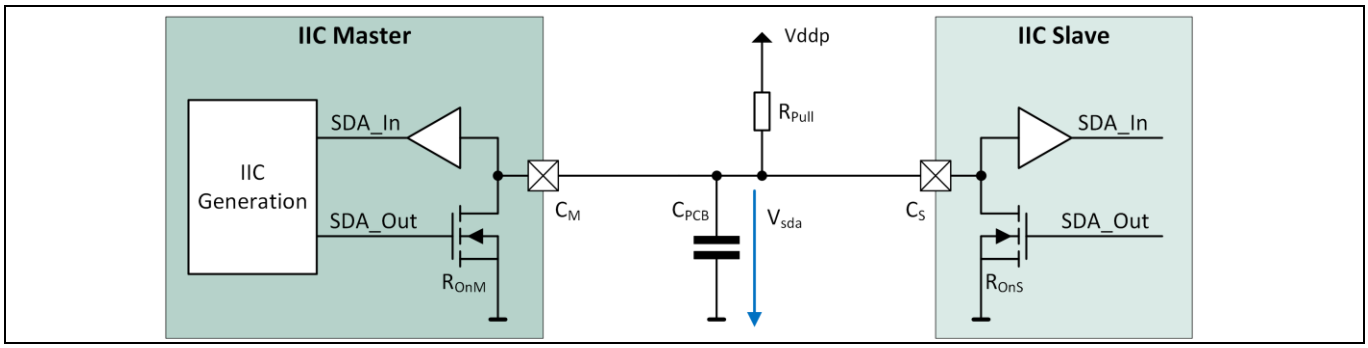

Figure 17 I2C SDA Driver Considerations

The required equations to calculate pull-up resistors, voltage levels and ramp times are given in the following overview:

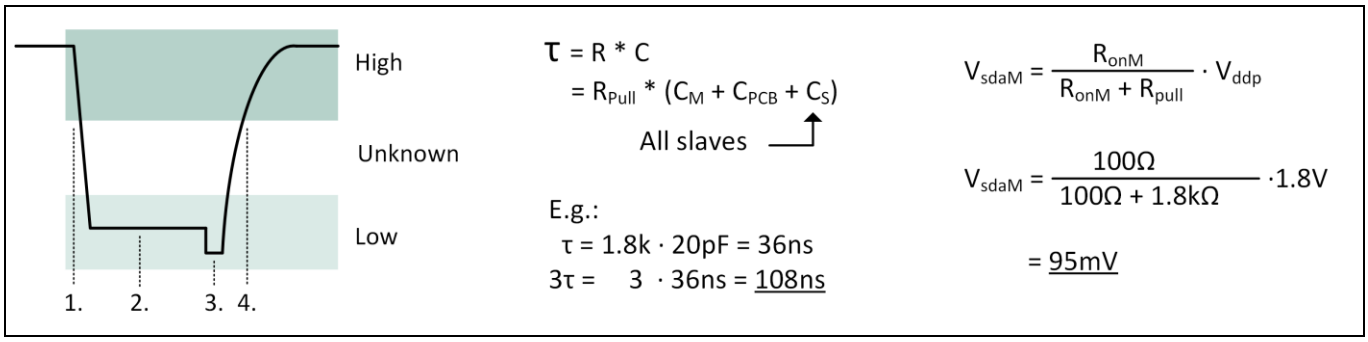

Figure 18 I2C Timing Equations

In this example the pull-up resistor is 1.8kOhm and the transistor which pulls low has 100Ohm on-resistance (R_{onM} and R_{onS}).

When e.g. the Master drives low (phase #2 in Figure 18 on the left) it competes with the pull-up resistor. This creates a voltage divider as described by the equations shown in Figure 18 on the right. The actual voltage on the SDA line for the Low level is approximately 95mV. Even for lower pull-up resistor values this is typically no problem. The fall-times usually lie in the <=50ns range.

When e.g. the Master drives a High after a Low it shuts off the transistor that pulls low. Now the pull-up resistor takes over and will charge the line and all the capacity attached to it. The total capacity consists of the pin capacities of the Master, the Slave(s) and the PCB trace. The charging looks like an RC-charging curve (phase #4 in Figure 18 on the left). The time constant is given by the equation in Figure 18 in the middle. One time constant τ reflects 63% Vdd, 2τ 86% and 3τ 95%. While 1τ may still be marginal 2τ or even 3τ are sufficient to be

detected as a solid High. In this example τ = 36ns and therefore 2τ = 72ns and 3τ = 108ns. The charge times may appear slow but they are still far away from becoming an issue. Even for communication speeds of 1MHz there is enough time to ensure a proper High. At 1MHz one SCL clock cycle lasts 1us and therefore half a clock cycle lasts 500ns. This is the time during which the data on SDA needs to settle. When planning for a decent guard band of e.g. 100ns there are still 400ns left for the High to settle.

When one driver hands over the SDA line to the other, e.g. Master hands over to Slave while waiting for the Slave to acknowledge, it is possible to see spikes and glitches during this time (phase #4 in Figure 18 on the left). Whether these will be spikes or dips and also their duration very much depends on the timing and driving capability between Master and Slave(s) as well as on the SDA data itself.

9.3 I2C Communication

9.3.1 I2C Dummy access

During and after a power-on of VDD or VDDP the I2C interface remains in a state which blocks all I2C communication and therefore no data can be acknowledged. Depending on the I2C implementation in the Master such a non-acknowledge may cause the Master to get stuck while waiting for the slave to acknowledge.

To leave this blocked state at least the following options exist:

- Send two or more clock pulses with SDA = '1'
- Send bus clear command where the master sends 9 clock pulses with SDA = '1'
- Make I2C read/write to a slave address that does not require such a dummy access
- Ping slave with one byte

After the blocked state was left the I2C operates according to the NXP I2C specification. The following figure shows an example for 'bus clear' and 'ping':

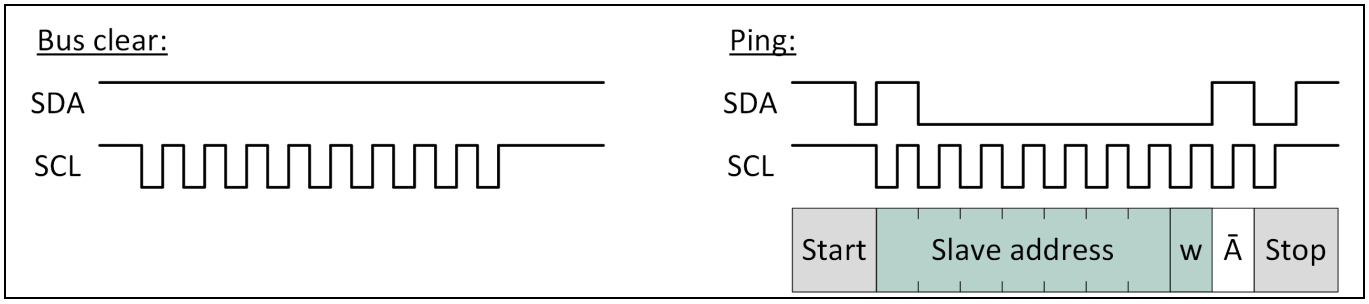

Figure 19 I2C Bus Clear & Ping

9.3.2 I2C Write access

There is the possibility of a single write access and block write access. A single write-access will allow writing to one 16-bit address while a block access allows multiple 16-bit accesses in a sequence:

Single Write Access:

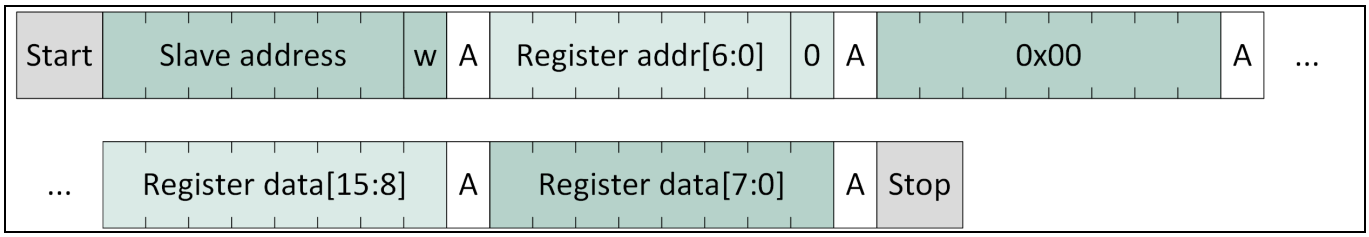

Figure 20 I2C Single Write Access

An example write access to register address 0x02 for I2C Slave address 0x40 with data 0x83A1 is shown in the figure below:

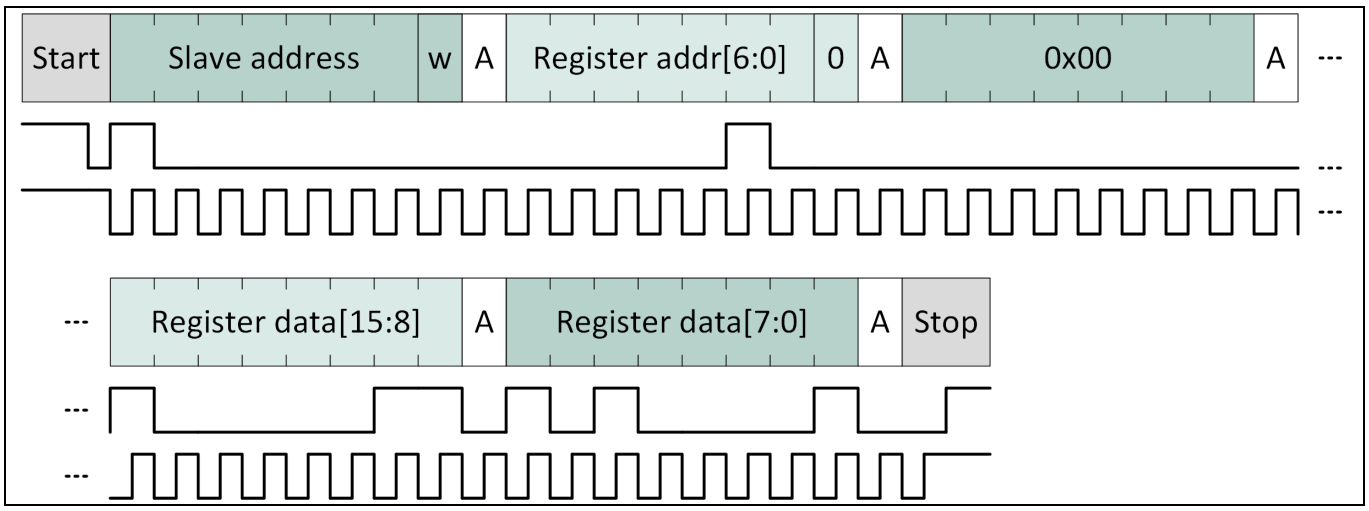

Figure 21 Single Write Access Example

A block write access is simply a single write access with additional bytes before the Stop condition:

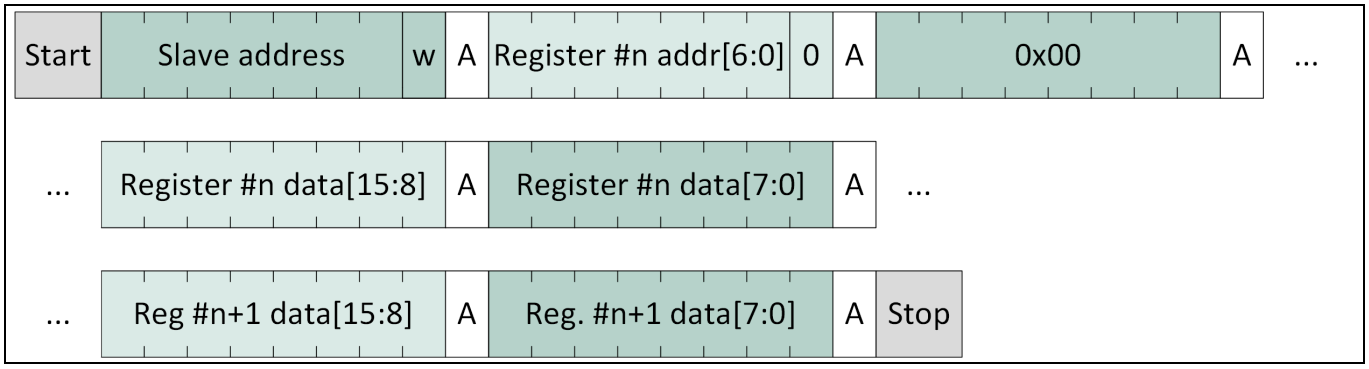

Figure 22 Block Write Access Example

9.3.3 I2C Read access

There is the possibility of a single read access and block read access. A single read-access will allow reading of one 16-bit address while a block access allows multiple 16-bit reads in a row:

Single Read Access:



Figure 23 I2C Single Read Access

An example read access from register address 0x02 for I2C Slave address 0x40 with read data 0x83A1 is shown in the figure below:

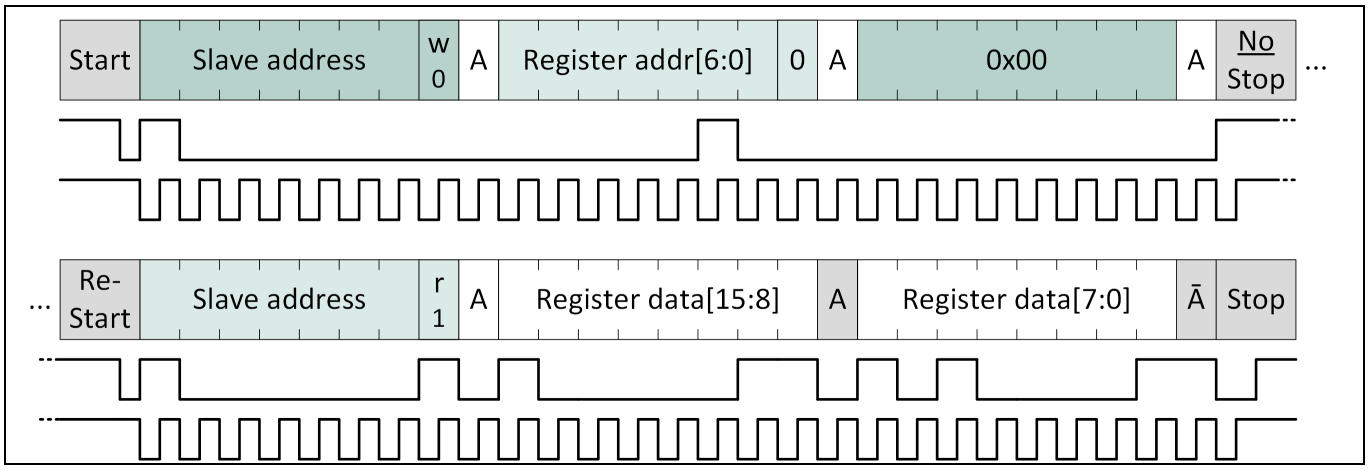

Figure 24 Single Read Access Example

A block read access is simply a single read access with additional read bytes before the NACK and Stop condition:

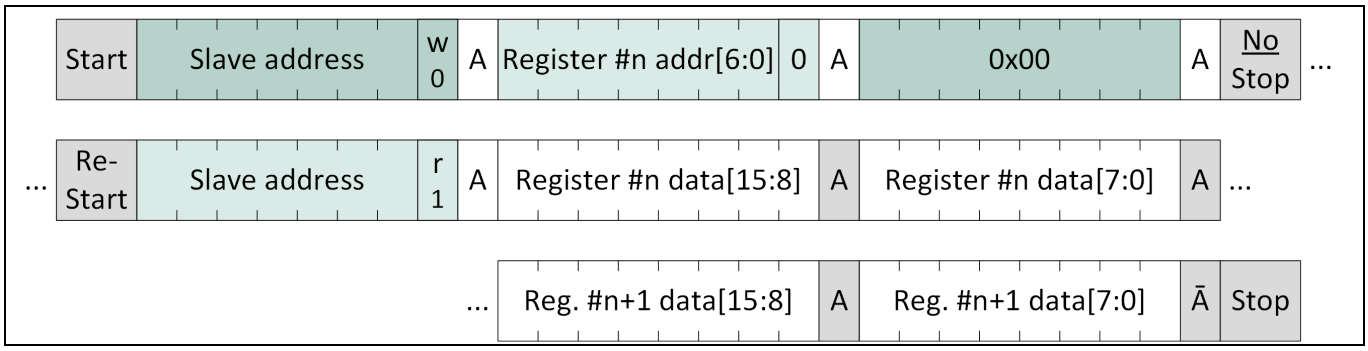

Figure 25 I2C Block Read Access

9.4 I3C Communication

This device is an I3C capable target and acts as an I2C device (with all the I2C limitations) before it gets its I3C Dynamic Address assigned. It fulfills the I3C Basic[SM] Specification version 1.1.1 from 09/Jun/2021. The following Dynamic Addressing modes are supported:

- ENTDAA
- SETDASA (assign target dynamic address) with limitations
- SETAASA

To communicate with the target using I3C the Primary Controller (Master) needs to execute the following steps:

- Set Dynamic Address for each target
- Read and/or write registers

These steps are described in the following chapters.

9.4.1 I3C Target Information

Some I3C commands require/deliver additional information about the target and its capabilities. At least the following commands do so:

- PID: Provisioned ID (used e.g. for ENTDAA or GETPID)
- BCR: Bus Characteristics Register (used e.g. for GETBCR)
- DCR: Device Characteristics Register (used e.g. for GETDCR)

The Provisioned ID (PID) looks like this:

- Bits[47:33]: 15-bit MIPI Manufacturer ID = 0x011A (Infineon)
- Bit [32] : Provisioned ID Type Selector = Vendor Fixed Value = 0x0
- Bits[31:16]: 16-bit Part ID = 0x0000
- Bits[15:12]: Instance ID = I2C address – 0x40 according to the ADR0 and ADR1 pins = 0x0 .. 0x7
- Bits[11:0]: 12-bit = 0x000

For an Instance ID = 0x**1** the PID is 0x0234_0000_**1**000 and for an Instance ID = 0x**5** the PID is 0x0234_0000_**5**000.

The 8-bit BCR register has the value 0x22 and looks like this:

- 7:6 = 0x0 = device is an I3C target
- 5 = 0x1 = device supports Advanced Capabilities
- 4 = 0x0 = device is not a virtual target
- 3 = 0x0 = device does not have low-power modes
- 2..1 =0x1 = device supports in-band interrupts (currently no interrupts available)
- 0 = 0x0 = no data speed limitation

The 8-bit DCR register has the value 0x00.

9.4.2 I3C Dynamic Address assertion using ENTDAA

One way to assign Dynamic Addresses to all targets can be done by using the ENTDAA command. The targets will answer one after the other. An answer includes PID, BCR and DCR. After those the Controller will provide the Target Dynamic Address with the next byte:

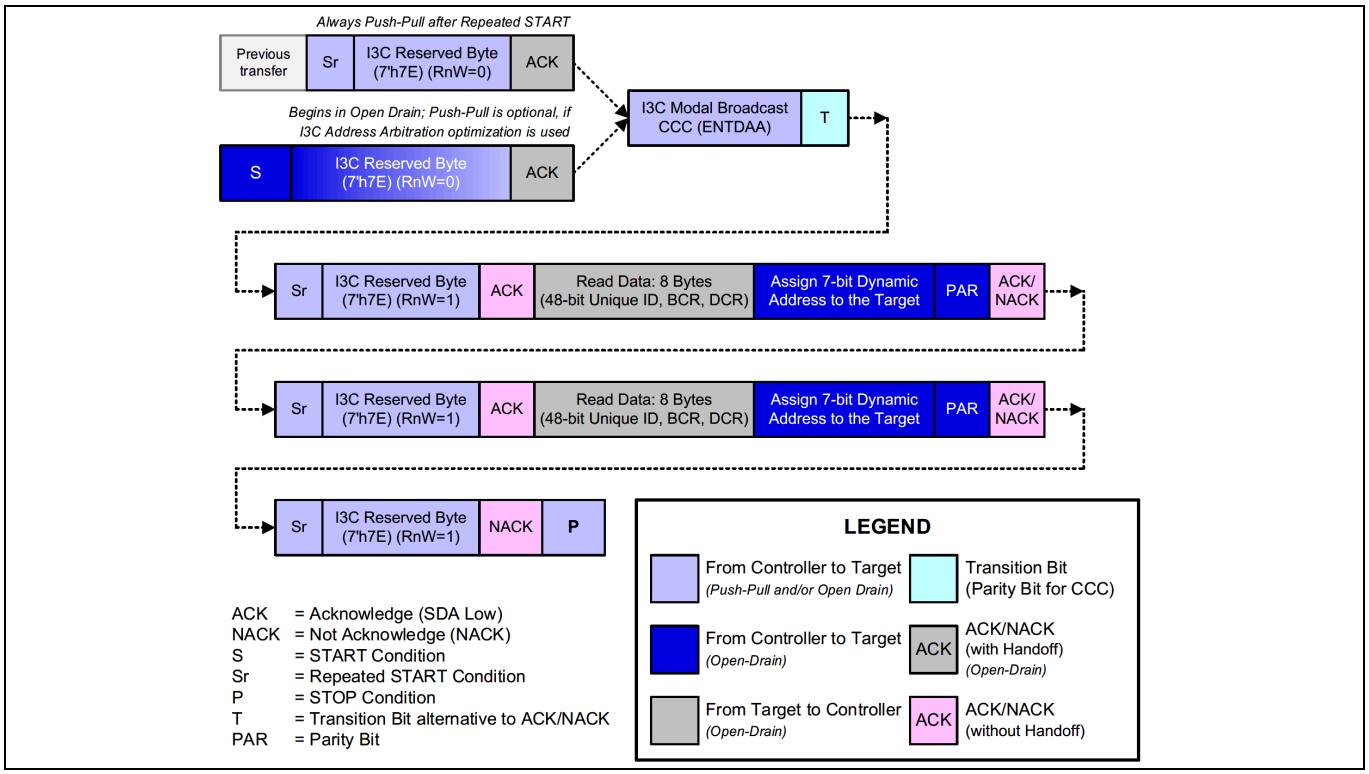

Figure 26 ENTDAA Command Structure

For a configuration with two targets (e.g. one target has I2C address 0x1 and one 0x5) the answer will be:

- Target 0x1: PID = 0x0234_0000_**1**000, BCR = 0x22, DCR = 0x00, Dynamic Address = 0x08
- Target 0x5: PID = 0x0234_0000_**5**000, BCR = 0x22, DCR = 0x00, Dynamic Address = 0x09

Please note that the Dynamic Address depends on the I3C Controller implementation.

9.4.3 I3C Dynamic Address assertion using SETDASA

With this command the Dynamic Address in a target can be set by addressing the Targets via their static I2C address:

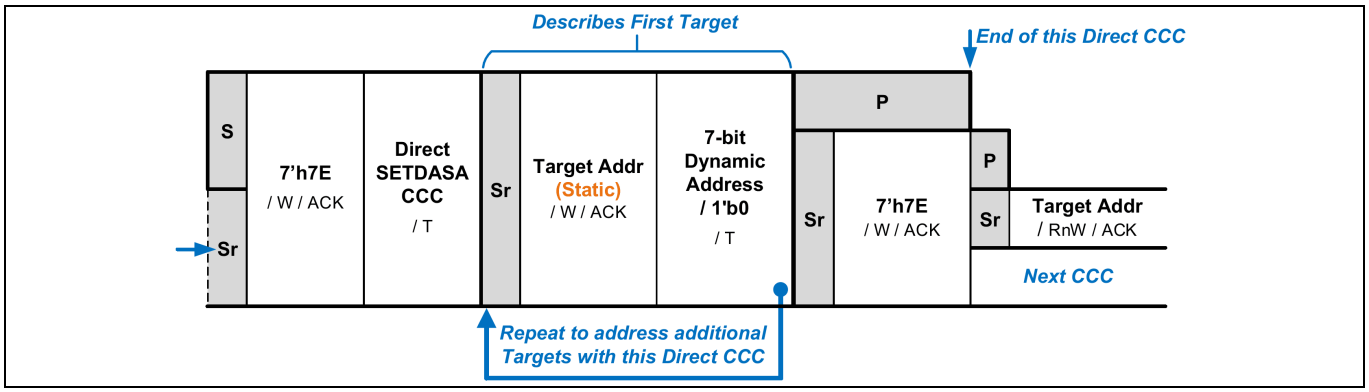

Figure 27 SETDASA Command Structure

Please note that the Static Address is the address set by the ADR0 and ADR1 pins. For this device it can range from 0x40 until 0x47.

Note: For this device version it is not possible to repeat the command part 'Target Addr' and 'Dynamic Address' as stated in Figure 27. Instead the SETDASA direct command must end after this part. In other words: for each Target an individual SETDASA command has to be used.

9.4.4 I3C Dynamic Address assertion using SETAASA

This command is the fastest way to set the Dynamic Address for all Targets.

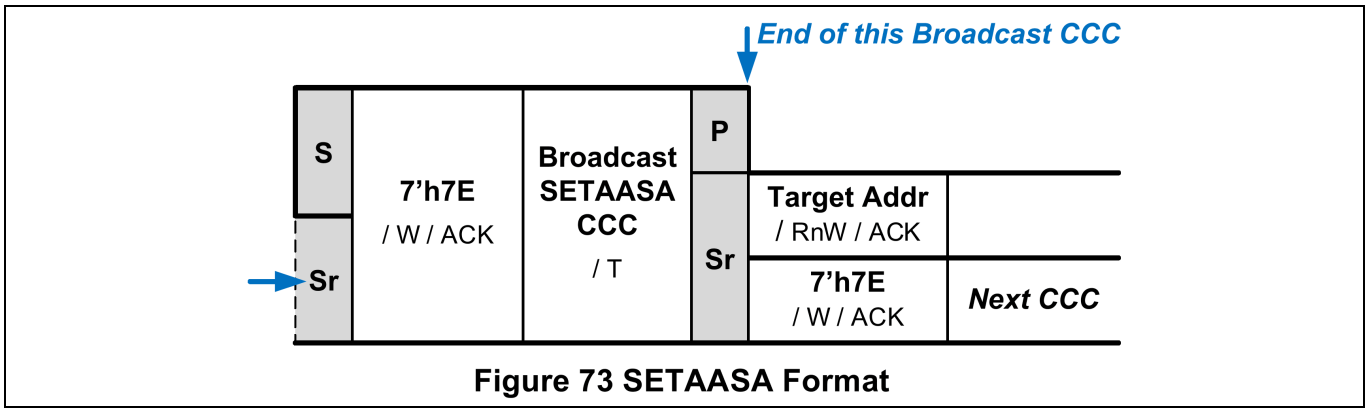

Figure 28 SETAASA Command Structure

9.4.5 I3C SDR read access

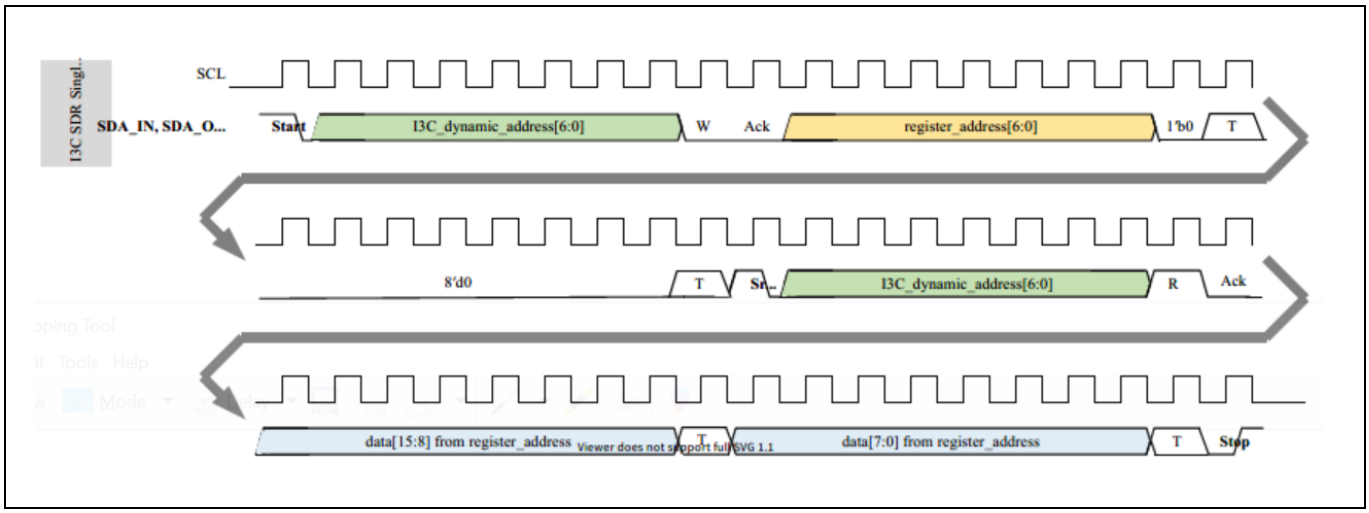

Figure 29 I3C SDR single read

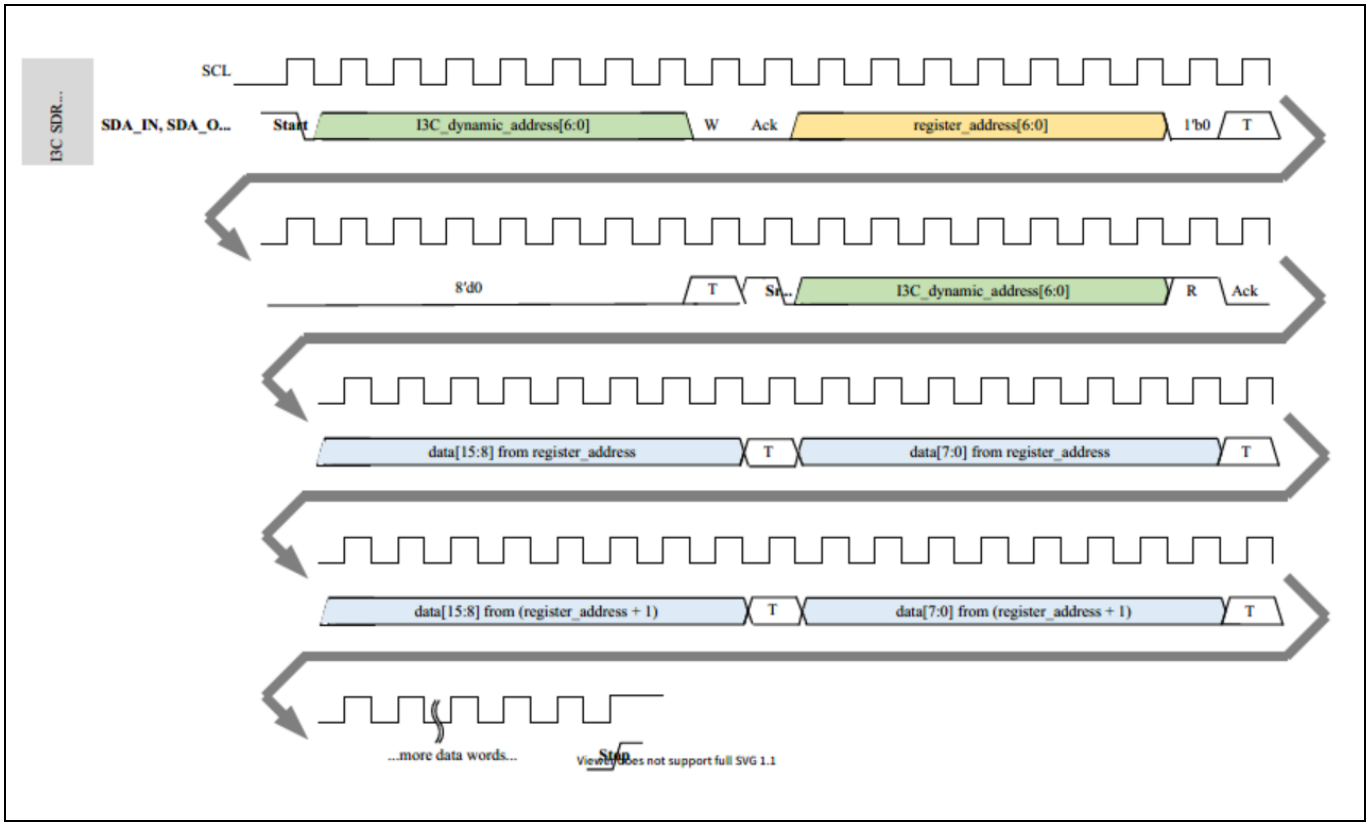

Figure 30 I3C SDR block read

9.4.6 I3C SDR write access

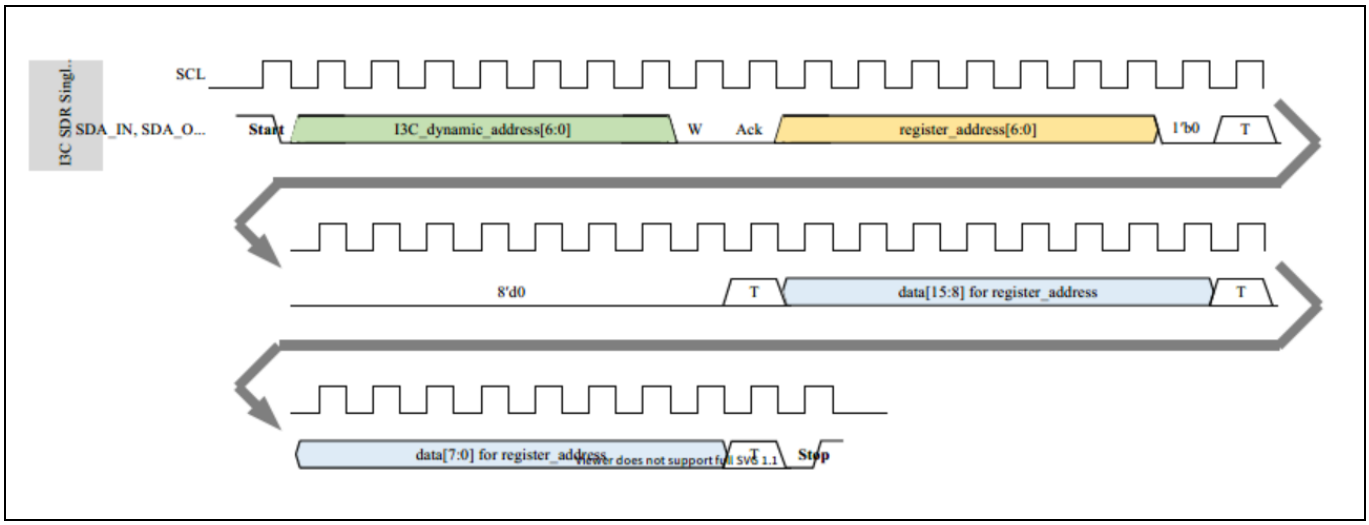

Figure 31 I3C SDR single write

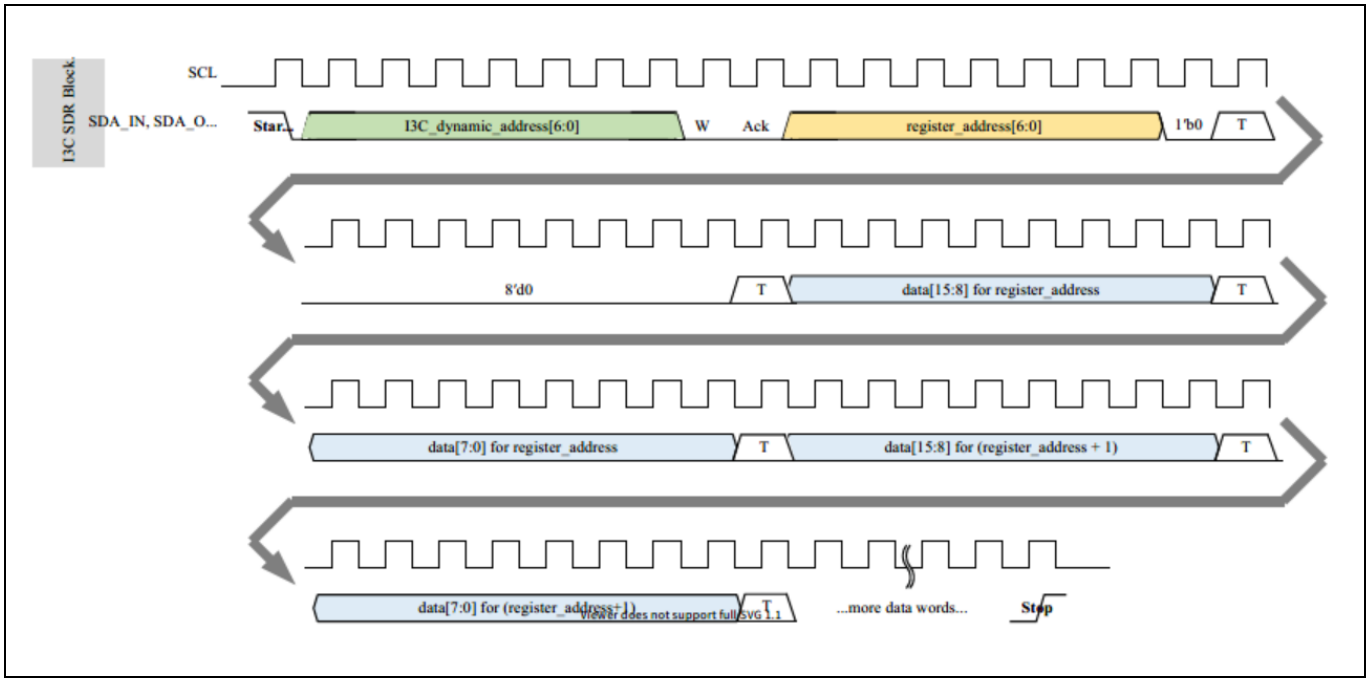

Figure 32 I3C SDR block write

9.4.7 I3C HDR DDR

Both single and block transfers are supported for HDR-DDR mode in the read and write directions. HDR-DDR transfers are terminated by a CRC word, transmitted by the device which sent the data (in the write direction this is the master, and in the read direction this is the slave). In the write direction, the master simply transmits the CRC word after it has finished transmitting data to the bus. In the read direction, the master must send the requested length of the transfer in advance, as part of its command word (see HDR-DDR read transfers). There are some important considerations for HDR-DDR communications:

- The HDR-DDR command codes 'Reserved for I3C Definition' in the MIPI I3C specification should not be used. This is achieved by starting all HDR-DDR command codes with 11_b.

- In a HDR-DDR read transaction, the command code in the write command word is taken as the number of words expected. The command code in the read command word is ignored.
- HDR-DDR bus turnaround occurs in a write transaction during preamble of first data word returned by slave, and during setup bits of CRC word returned by slave. Please see the MIPI I3C specification for detail on HDR-DDR bus turnaround, as it is not shown in detail here.

The following figures show the timing diagrams of both single and block read and write processes.

9.4.8 I3C HDR DDR read access

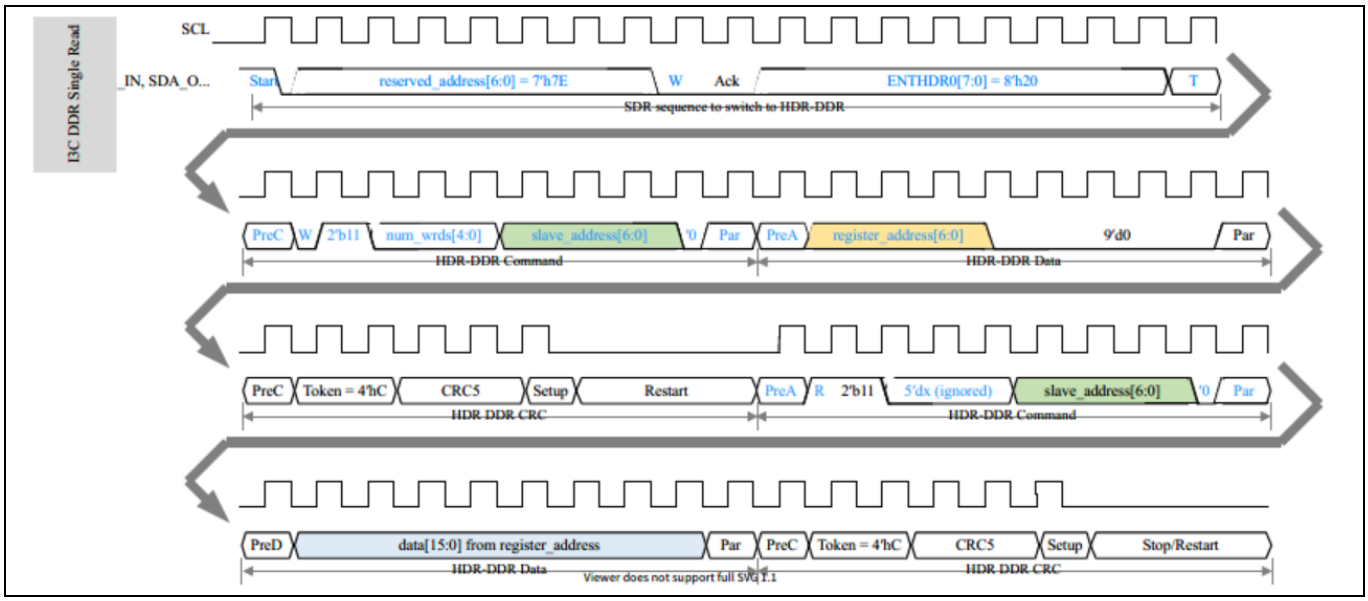

Figure 33 I3C HDR-DDR single read

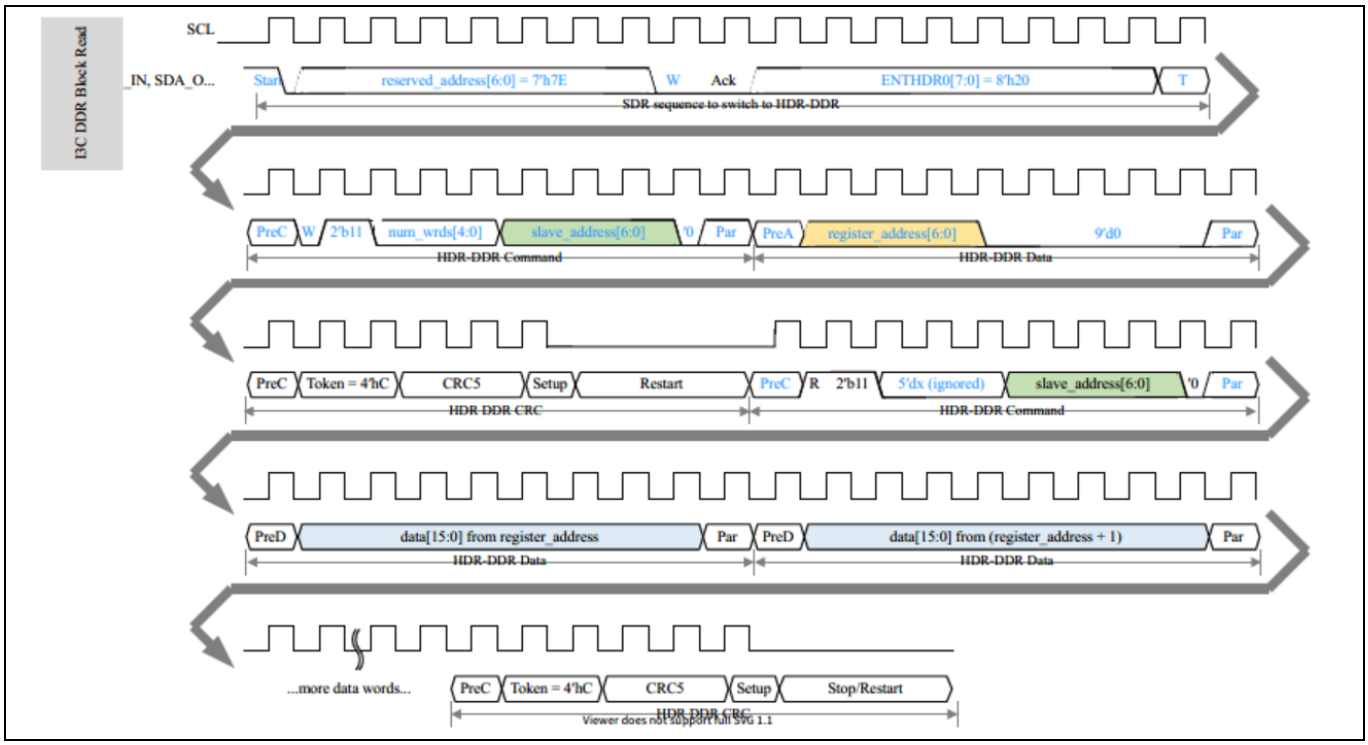

Figure 34 I3C HDR-DDR block read

9.4.9 I3C HDR DDR write access

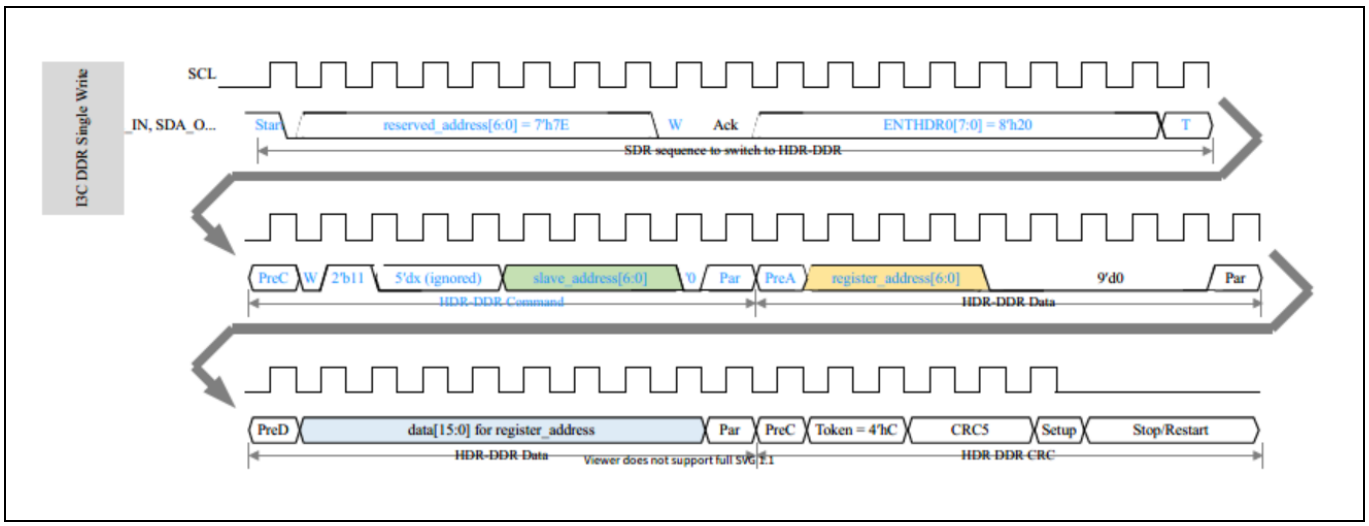

Figure 35 I3C HDR-DDR single write

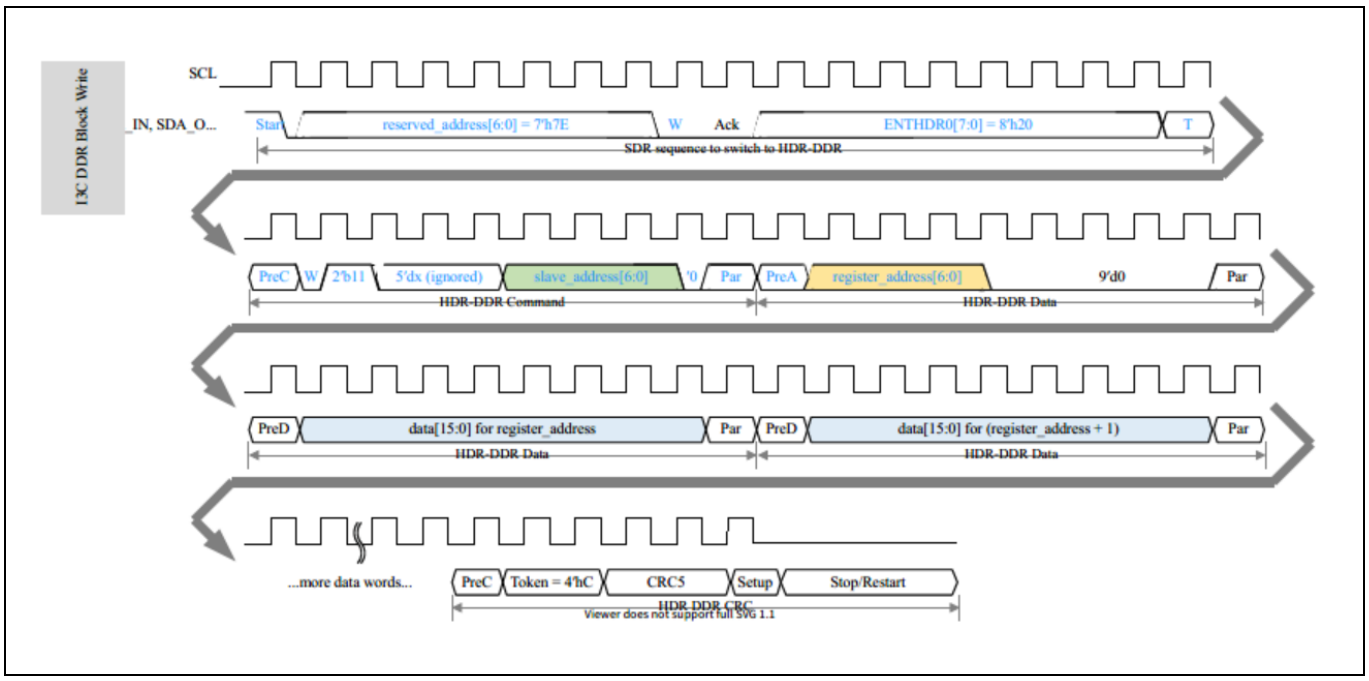

Figure 36 I3C HDR-DDR block write

10 Functional behavior description

The main function of this device is to have DACs generate voltages used as gate voltages for RF transistors to set their bias point e.g. in power amplifier applications:

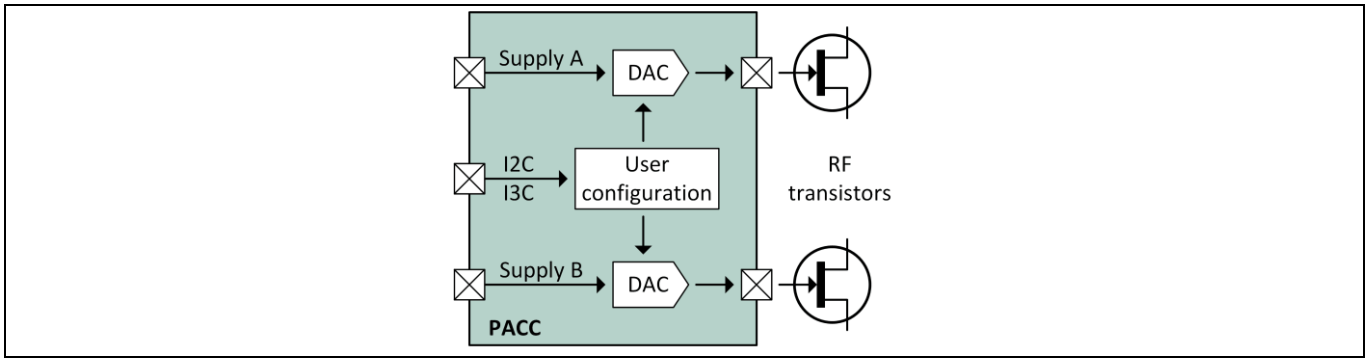

Figure 37 Simplified Device Block Diagram

10.1 Device Interface Signals

A more detailed diagram focusing on the main functions is shown in the figure below. It also lists all device pins/signals:

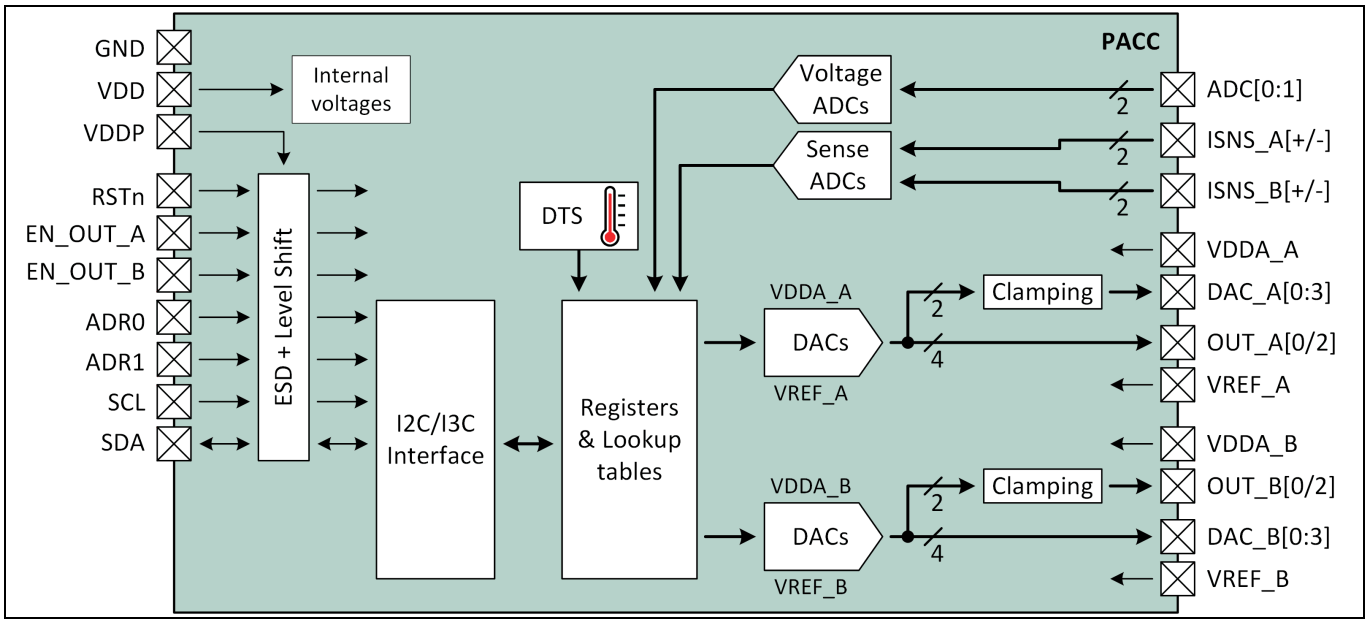

Figure 38 Detailed Device Block Diagram

10.2 Power-Up and Digital Interface Availability

Power supplies can be ramped-up in any sequence. To make the digital interface available VDD and VDDP need to cross their undervoltage release threshold $UVLO_{VDD,rel}$ and $UVLO_{VDDP,rel}$. This is necessary as the device-internal logic is supplied by internal voltages derived from VDD (see Figure 39 time point #1):

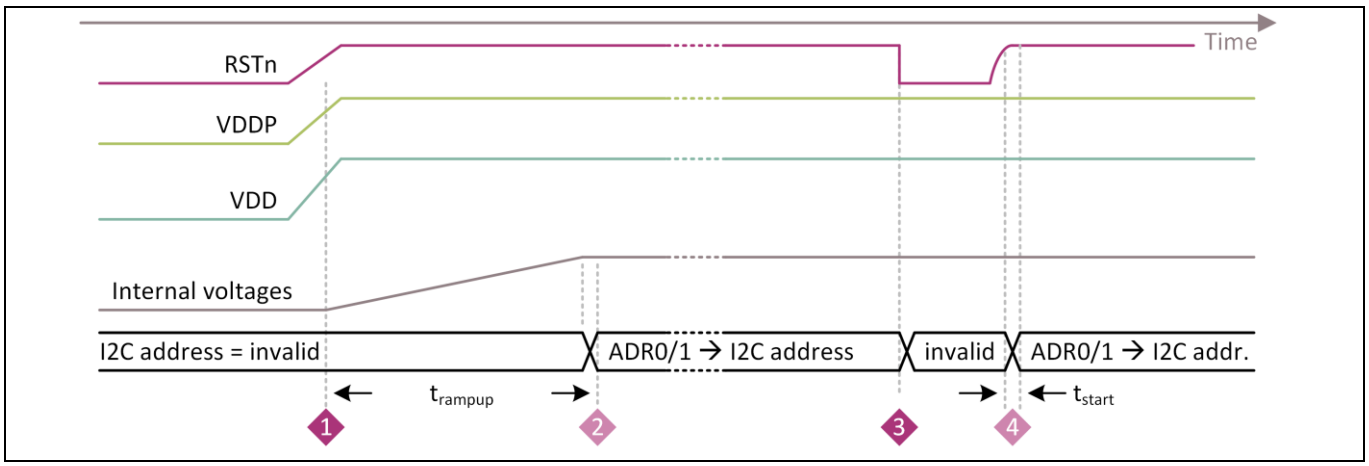

Figure 39 Power-Up and reset Timing

After the rampup time t_{rampup} the internal voltages are stable and the address pins ADR0/1 determine the I2C address (see time point #2). The address remains stable until the next power-down or reset via RSTn. Digital communication can now take place. Note that the voltages VDDA_A, VDDA_B, VREF_A and VREF_B will have no effect on the availability of the digital interface.

In case software decides to execute a reset by asserting RSTn low (see time point #3) the digital interface will be blocked during that time. After reset is released it takes maximum t_{start} to make the digital interface accessible again (see time point #4).

Once t_{rampup} elapsed and the internal voltages are available the temperature sensor (DTS), the voltage ADC (ADC) as well as the current sense ADC (CSA) can be used. To do so they need to be enabled first and their startup time needs to elapse first.

10.3 Voltage Monitoring

All voltages provided externally to the device are monitored. Once a voltage falls below its undervoltage limit ($UVLO_{lck}$) it needs to rise beyond its undervoltage release limit ($UVLO_{rel}$). The voltage difference between the two is the hysteresis:

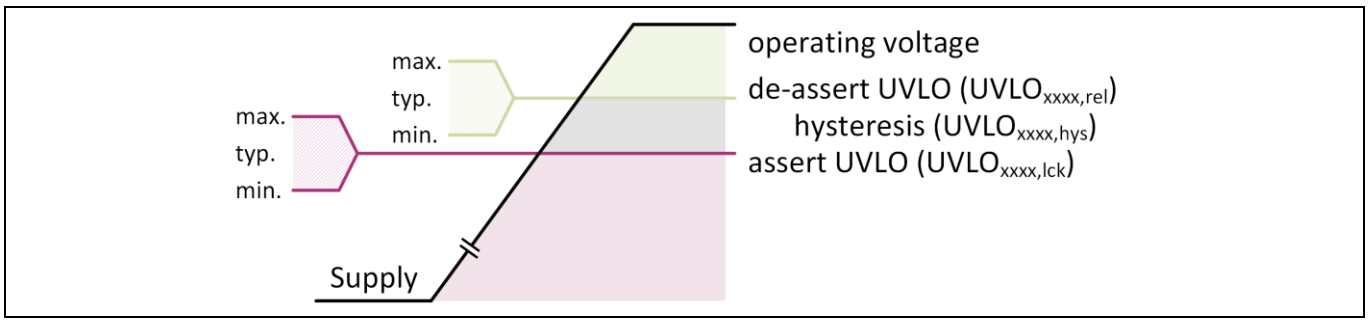

Figure 40 Voltage Monitoring

11 DAC Output Voltage Configuration

The DACs generate a voltage which is used by RF transistors as their gate bias. Two pins, EN_OUT_A and EN_OUT_B, allow switching this voltage between two voltage levels. One voltage is used to bring RF transistors into their active/conductive region (DAC_A0...DAC_B3). The second voltage (clamping voltage) is used to bring the RF transistors into their pinch-off region.

Only half of the DACs, the ones with an even channel number (DAC_A0, DAC_A2, DAC_B0, DAC_B2), provide a clamping voltage (OUT_A0, OUT_A2, OUT_B0, OUT_B2).

A simplified block diagram is given in the following figure:

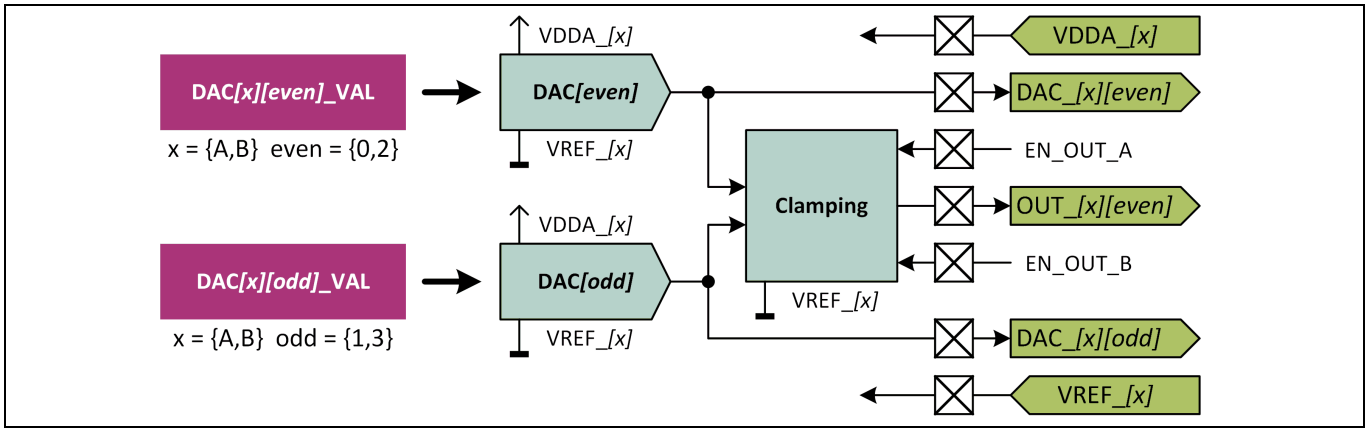

Figure 41 DAC Simplified Block Diagram

The generated voltages depend on various register settings. The following figure shows the entry point for each register setting:

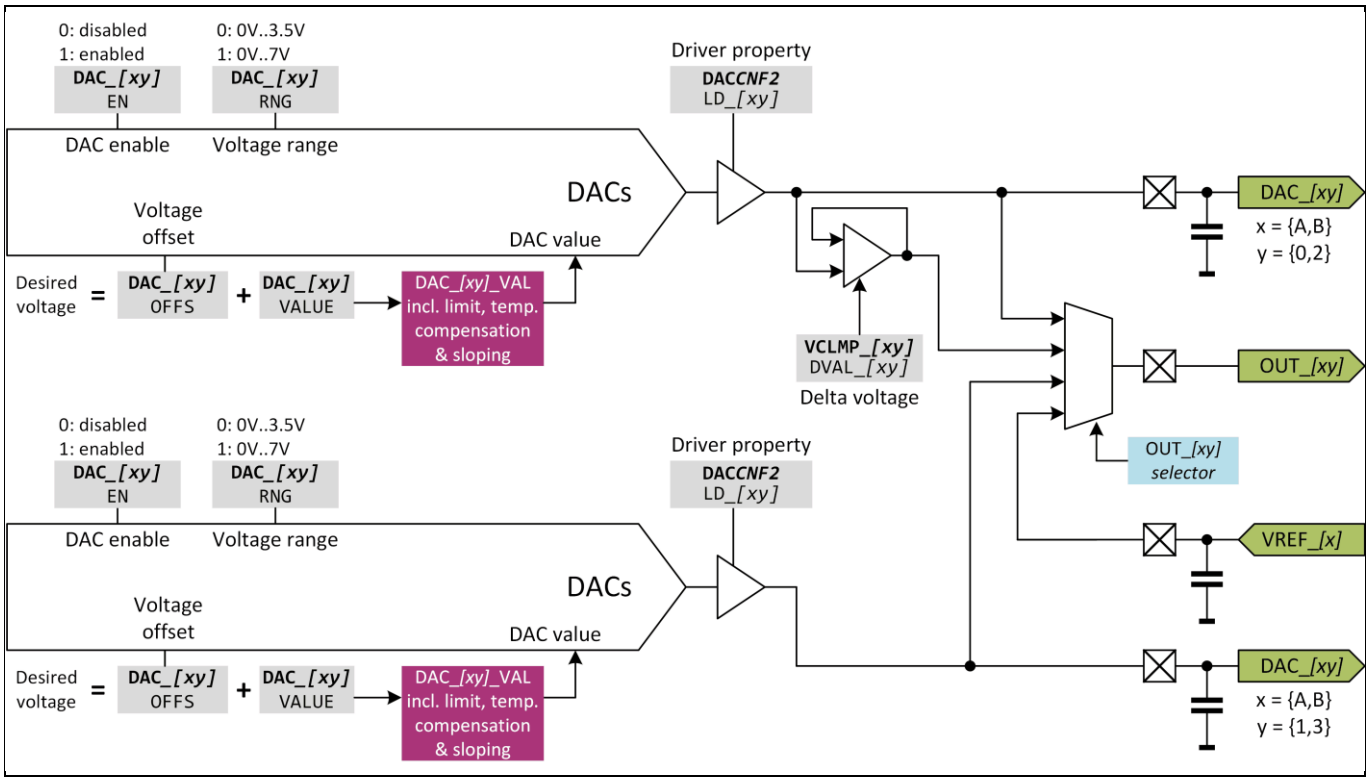

Figure 42 DACs and their Registers

DAC Output Voltage Configuration

The clamping voltage can be chosen from:

- Neighboring odd DAC (e.g. for DAC_A0 it is DAC_A1 etc.)
- A 6-bit offset DAC (VCLMP buffer) adding a delta voltage to an even channel
- The corresponding VREF_[x]

When clamping is enabled the OUT_[xy] shows the corresponding DAC_[xy] voltage. When no clamping is enabled then OUT_[xy] shows the selected clamping voltage. The following figure gives an overview about the register bits and their influence on the clamping:

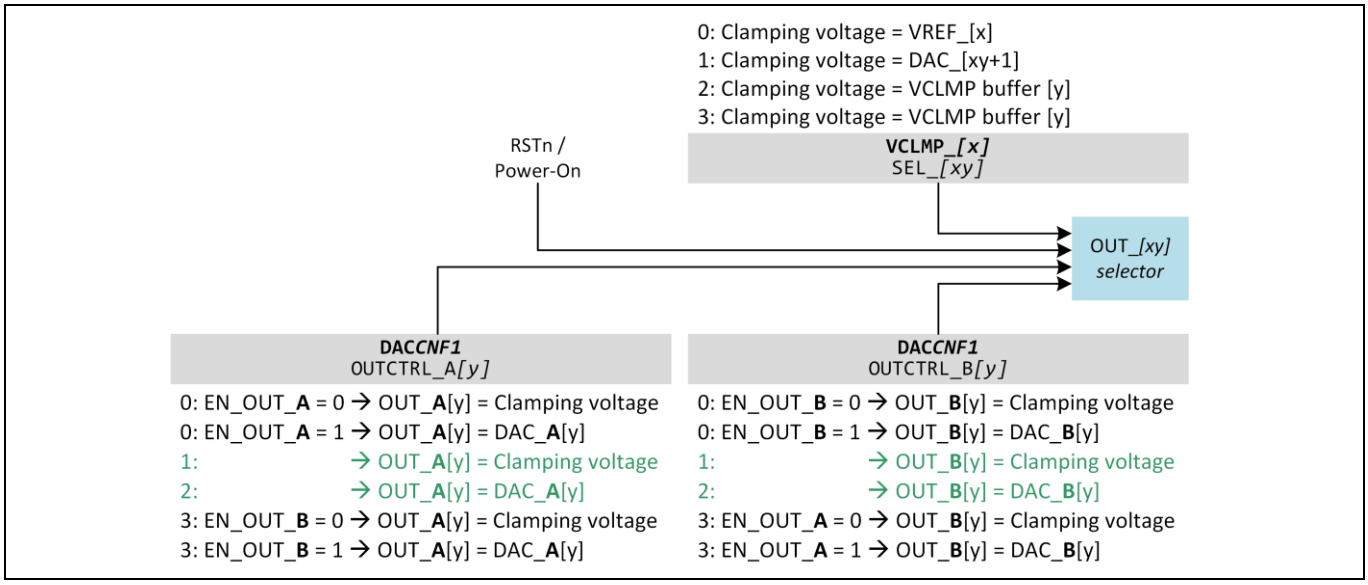

Figure 43 OUT_[xy] Selection

How to use clamping will be explained in the following sections.

11.1 DAC and OUT Voltages during Power-On or Reset

A software and power-on reset will cause all register settings to revert to their reset values. This also disables the DACs. During such a situation the device needs to drive a defined output voltage at the DAC_[xy] and OUT_[xy] outputs to protect the RF transistors from electrical damage e.g. in case always-on transistors are used. The following figure gives a simplified overview about the electrical behavior during a reset condition:

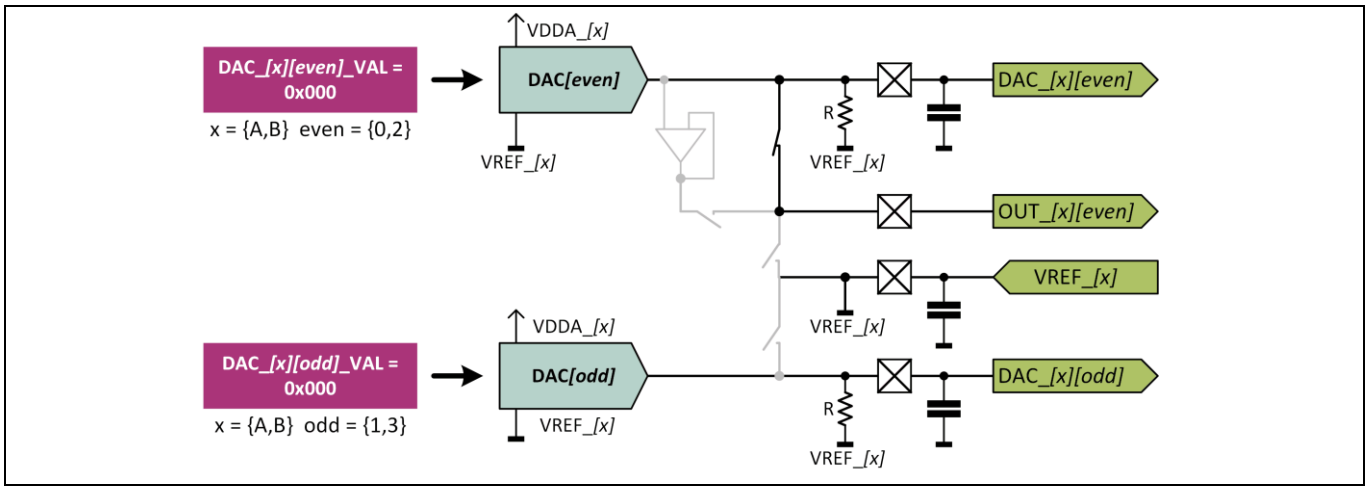

Figure 44 DAC Power-On / Reset Behavior

11.2 DAC Basic Settings Overview

It is recommended to program the DAC related registers in the following order:

- DAC_[xy].RNG: Output voltage range either 3.5V or 7.0V. The DAC resolution (12-bit) divides this range into 2^12 – 1 = 4095 voltage steps (0.855mV for 3.5V and 1.71mV for 7V)
- DAC_[xy].OFFS: Offset voltage with respect to VREF_[X]. It can be either [0V; 0.5V; 1.5V; 2.5V] for 3.5V range or [0V; 1V] for 7V range
- DAC_[xy].VALUE: Offset plus DAC value results in the desired output voltage (temperature compensation not considered)
- DACCNF2.LD[xy]: DAC current drive capability and stability

Some DAC channels allow toggling between two voltages in order to clamp RF transistors. Mainly the signals EN_OUT_A and EN_OUT_B are used for this purpose. Also during debugging phase it may be necessary to force DACs to fixed values independent of EN_OUT_A or EN_OUT_B.

Below is a list of registers to be configured when using the clamping/forcing feature for the OUT_[xy] channels:

- DACCNF1.OUT_CTRL_[xy]: Clamp enabled by either EN_OUT_A = 0, EN_OUT_B = 0, never or always
- VCLM_[x].SEL_[xy]: Clamping voltage can be chosen from VREF_[x], DAC_[xy] or VCLMP buffer
- VCLMP_[x].DVAL_[xy]: Defines 6-bit offset voltage when using VCLMP buffer as clamping voltage

It is also possible to have DAC channels track other DAC channels. This can become useful when one RF-transistor bias point requires a fixed offset to another transistor. Then the following registers can be programmed:

- DACCNF1.TRK_A1toA0 … DACCNF1.TRK_B3toB2: Odd DAC channels track their neighboring even channels

11.3 DAC Value Computation

To calculate the appropriate DAC_[xy].VALUE the following parameters must be known:

DAC supply voltages VDDA_[x] and VREF_[x]

Desired output voltage for DAC channel [xy] relative to VREF_[x]

DAC range

DAC offset

The figure below shows how those parameters define the DAC output voltage:

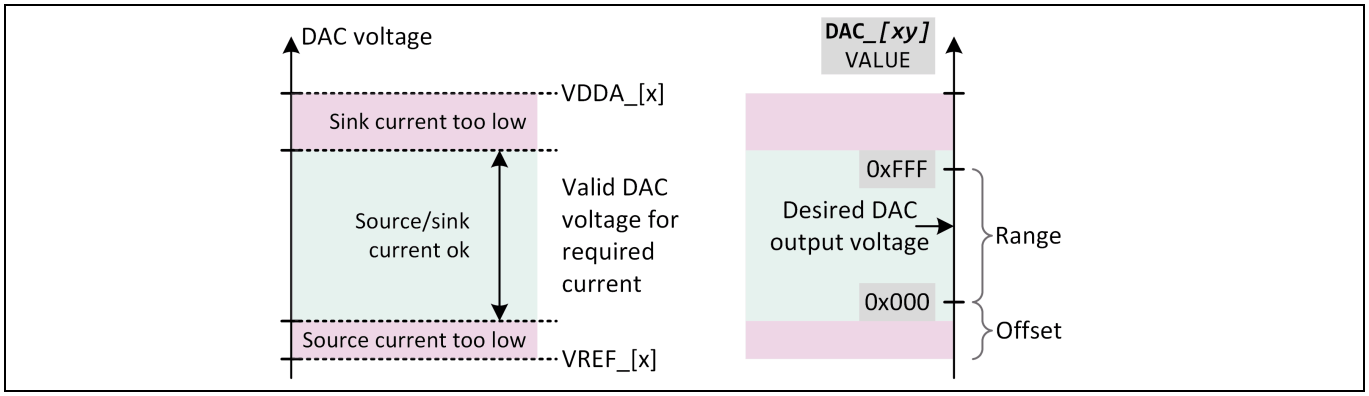

Figure 45 Parameters Relevant for DAC Value

The DAC output voltage should have a safe voltage distance to VDDA_[x] and VREF_[x] as the DAC cannot drive rail-to-rail. Depending on the required current to be sourced/sinked there is a voltage drop which limits the maximum output voltage. The parameters I_{src} and $I_{src,hi}$ as well as I_{snk} and $I_{snk,hi}$ specify the maximum source/sink current at a given voltage drop.

To set a fixed voltage distance from VREF_[x] an analog offset for each individual channel can be defined by DAC_[xy].OFFS. Preferrably the offset is chosen to have the DAC voltage range in the middle of VDDA_[x] + VREF_[x]. To maximize DAC granularity ideally the 3.5V voltage range is used.

As the final step the DAC value DAC_[xy].VALUE can be calculated as the voltage difference relative to the offset voltage. Please note that in a real-world application there will be drifts/variations which require compensation. As an example a transistor bias point will vary over temperature. To guarantee a fixed bias point a DAC value set by DAC_[xy].VALUE will require adjustment over temperature. An automatic temperature compensation mechanism can be enabled for this purpose.

Figure 46 shows all steps executed in the device to determine the DAC value DAC_[xy]_VAL which is then translated into an output voltage. Further details are given in the following sections:

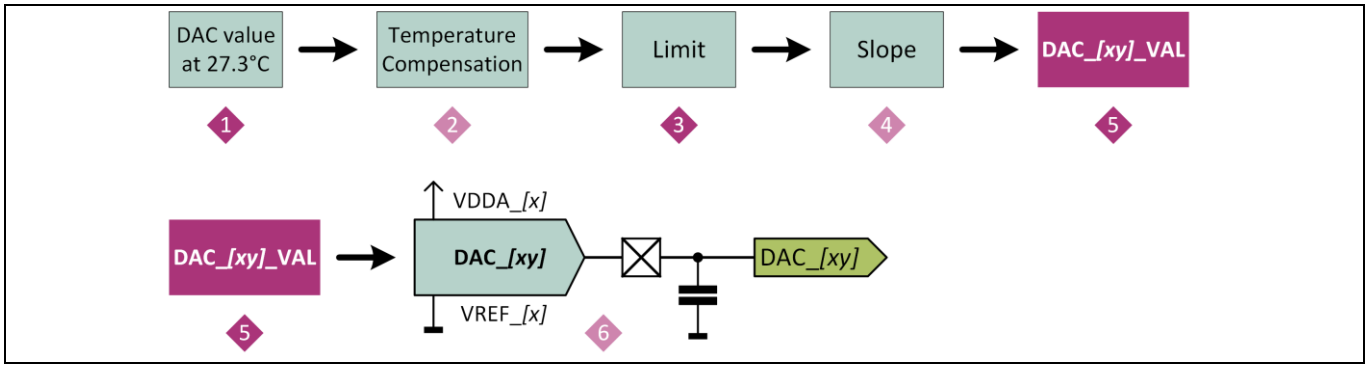

Figure 46 DAC[xy]_VAL Generation

11.3.1 DAC Value: Offset + Range

For a better understanding this section assumes an application which reqires a DAC output voltage of +/-3.6V at 27.3°C. Over temperature the DAC voltage must range only a few tens of millivolt to ensure a stable bias point for the RF transistor(s). The DAC voltage for biased and pinch-off mode the DC voltages differ by <=1V . Under all conditions approximately 20mA need to be sourced and sinked:

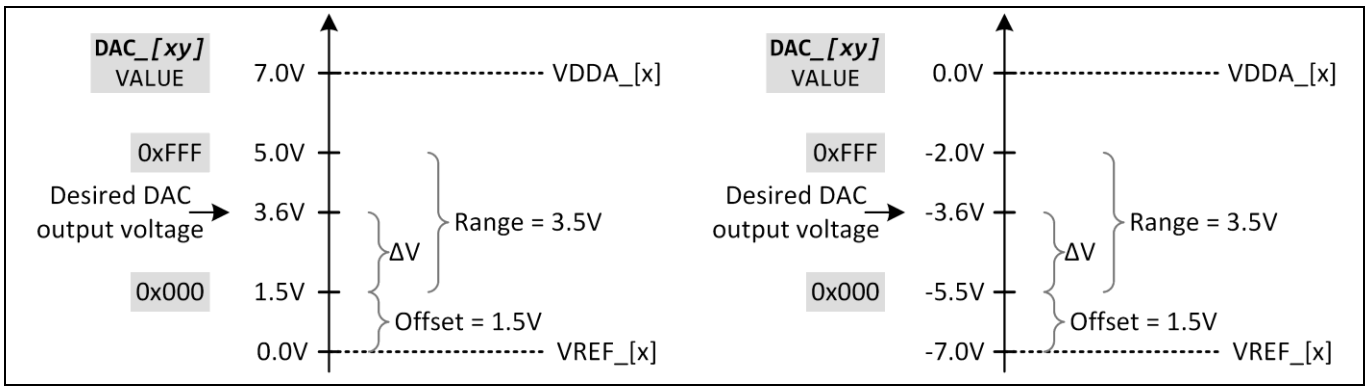

Figure 47 Parameters and their Influence on DAC Output Voltage

The DACs offer either 3.5V (DAC_[xy].RNG = 0) or 7.0V (DAC_[xy].RNG = 1) voltage range. Therefore DAC_[xy].RNG should be 0 to select 3.5V.

The required source current of 20mA allows DAC output voltages up to 1V lower than VDDA_[x] (see $I_{src, hi}$).
The required sink current of 20mA allows DAC output voltages up to 1V higher than VREF_[x].

For this application a voltage offset of >=1V will ensure proper functionality. The following voltage offsets can be selected by DAC_[xy].OFFS although the value 2 is recommended for this example:

0 = 0V offset: DAC voltage range is 0V…3.5V which is not sufficient for the desired DAC voltage of 3.6V

1 = 0.5V offset: DAC voltage range is 0.5V…4.0V which is just sufficient for the desired DAC voltage of 3.6V

2 = 1.5V offset: DAC voltage range is 1.5V…5.0V which is perfect for the desired DAC voltage of 3.6V

3 = 3.0V offset: DAC voltage range is 3.0V…6.5V which is just sufficient for the desired DAC voltage of 3.6V

The DAC value is used to generate a DAC voltage relative to VREF_[x] and the offset voltage set by DAC_[xy].OFFS (=ΔV). The following equation can be used to calculate the DAC value:

$$\text{DAC_[xy].VALUE} = \frac{4095}{\text{Range}} \cdot \Delta V \qquad \Delta V = \text{DAC_Voltage - Offset - VREF_[x]}$$

Figure 48 DAC Value Calculation Equation

In this example the DAC voltage should be 3.6V. The desired DAC range is 3.5V and the offset 1.5V. Therefore the DAC_[xy].VALUE register needs to have the value 2457 = 0x999:

$$\text{DAC_[xy].VALUE} = \frac{4095}{\text{Range}} \cdot \Delta V = \frac{4095}{3.5V} \cdot 2.1V = \underline{\underline{2457}} \qquad \Delta V = 3.6V - 1.5V - 0V = 2.1V$$

Figure 49 DAC Value Positive Calculation Example

The same example but with negative values: DAC output voltage needs to be -3.6V. The desired DAC range is -3.5V and the offset -1.5V. The DAC_[xy].VALUE register needs to have the value 2223 = 0x8AF:

$$\text{DAC_[xy].VALUE} = \frac{4095}{\text{Range}} \cdot \Delta V = \frac{4095}{3.5V} \cdot 1.9V = \underline{\underline{2223}} \qquad \Delta V = -3.6V - 1.5V - (-7V) = 1.9V$$

Figure 50 DAC Value Negative Calculation Example

11.3.2 DAC Value: Temperature compensation

Please see section 11.4 DAC Temperature compensation.

11.3.3 DAC Value: Limit

The DAC values coming from the temperature compensation are limited to 0xFFF at the upper end and 0x000 at the lower end. For the user it is not possible to exceed the limits simply by programming the DAC_[xy].VALUE registers. Therefore the limits are only relevant during temperature compensation. Please see section 11.4 DAC Temperature compensation for further details.

Also it is very unlikely that the limits will ever be reached. The DAC_[xy].OFFS and DAC_[xy].VALUE are usually programmed as such that the DAC values remain well around the middle of 0xFFF and 0x000 (=0x800).

11.3.4 DAC Value: Slope

To reduce inrush-currents especially after enabling a DAC it is possible to define a slope with which the DAC_[xy]_VAL is updated. This is mainly important after power-up. During operation the DAC values usually change only by a few counts e.g. by the temperature compensation.

Each time DAC_[xy]_VAL changes due to the temperature compensation or due to a changed DAC_[xy].VALUE the calculated DAC_[xy]_VAL value will be updated count by count with an update rate defined by DACCTRL.SLP: 0 = 50ns, 1 = 1us, 2 = 5us, 3 = 10us, 4 = 100us, 5 = 250us, 6 = 1ms, 7 = 4 ms. Note that the slope configured in DACCTRL.SLP is the same for all DACs.

Please note that the offset is not affected by sloping. In other words: when a DAC is enabled its output voltage will rapidly change from VREF_[x] to the offset voltage. Beyond the offset voltage the sloping effect will be visible. The following figure shows sloping without offset:

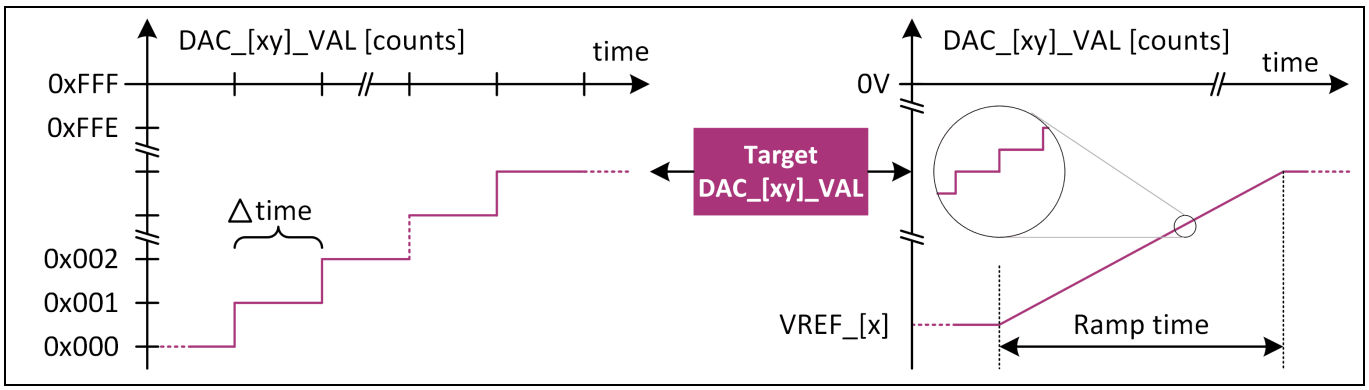

Figure 51 DAC Slope

If e.g. the software set DACCTRL.SLP = 1 = 1us per DAC count and the DAC_[xy].VALUE was programmed to 1900 (=76C) it will take 1900us to update DAC_[xy].VALUE to its final value.

11.3.5 DAC Value: Read Back Calculated Value

To verify that the DAC_[xy]_VAL has been calculated correctly it can be read via the digital interface. The register DAC_FB is used for this purpose. First, the register is used to tell the device from which channel the DAC_[xy]_VAL is requested. To do so one of the following values needs to be written to it:

Side	Channel	Bit 14 DAC_SIDE	Bits 13:12 DAC_CH	DAC_FB
A	0	0	00	0x0000
A	1	0	01	0x1000
A	2	0	10	0x2000
A	3	0	11	0x3000
B	0	1	00	0x4000
B	1	1	01	0x5000
B	2	1	10	0x6000
B	3	1	11	0x7000

Figure 52 DAC_FB Channel Selection

If e.g. the DAC_B2_VAL is of interest then DAC_FB needs to be written with 0x6000 first. After the write access the same register can be read. DAC_FB.VALUE will now contain the value for DAC_B2_VAL. Reading the register another time will always return the most recent value for DAC_B2_VAL.

11.4 DAC Temperature compensation

In general temperature influences silicon behavior. This is true for the DACs as well as for the RF transistors connected to them. The device built-in thermal compensation provides a convenient solution to minimize such effects. In case the user application requires a temperature compensation it is advised to read through the following sections.

Compensation is implemented with a Look-Up Table (LUT), in which temperature coefficients (gradients) for the DACs can be configured. Depending on the temperature measured by the DTS a delta to the reference DAC value at 27.3°C is calculated and provided to the DAC via DAC_[xy]_VAL.

In total nine equidistant interpolation points at fixed temperatures are needed to calculate the eight gradients (see Figure 54). The gradients need to be defined in such a way that the piecewise interpolated values approximate the Delta DAC curve best.

The following example is a real-world example where the DACs are used in a GaN-based power amplifier. It describes the process how to find the best gradients. The starting point is always a measurement over temperature to determine the DAC values required to achieve the desired DAC output voltage. In Figure 53 an example measurement is shown:

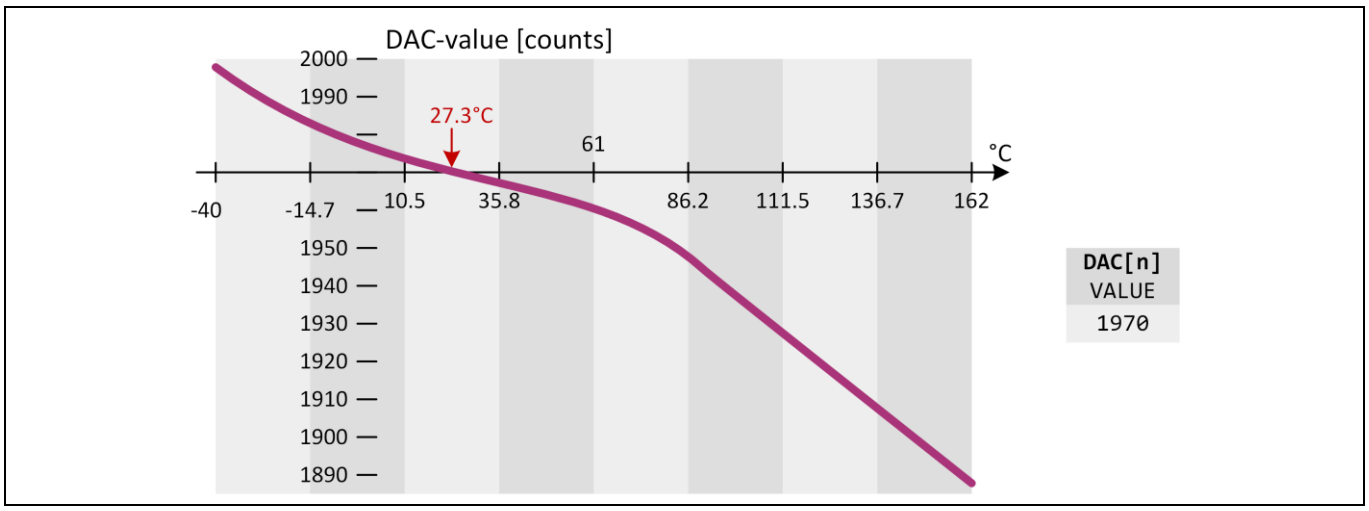

Figure 53 DAC Value Over Temperature

In this example a DAC value of 1970 is required to achieve the desired output voltage at the reference temperature of 27.3°C measured by the DTS temperature sensor. This value is used for the DAC[n].VALUE register. It will also be the reference point for the gradient fitting.

The temperature points shown on the X-axis match the temperatures at which one gradient starts/ends. Gradient #0 starts at -40°C while gradient #1 starts at -14.7°C and so on. Therefore it makes sense to measure the DAC value at least for these temperatures. For better fitting more measurements are advised. Figure 53 shows such a graph when using many measurement points.

DAC Output Voltage Configuration

The graph in Figure 53 can then be plottet relative to the DAC value at 27.3°C:

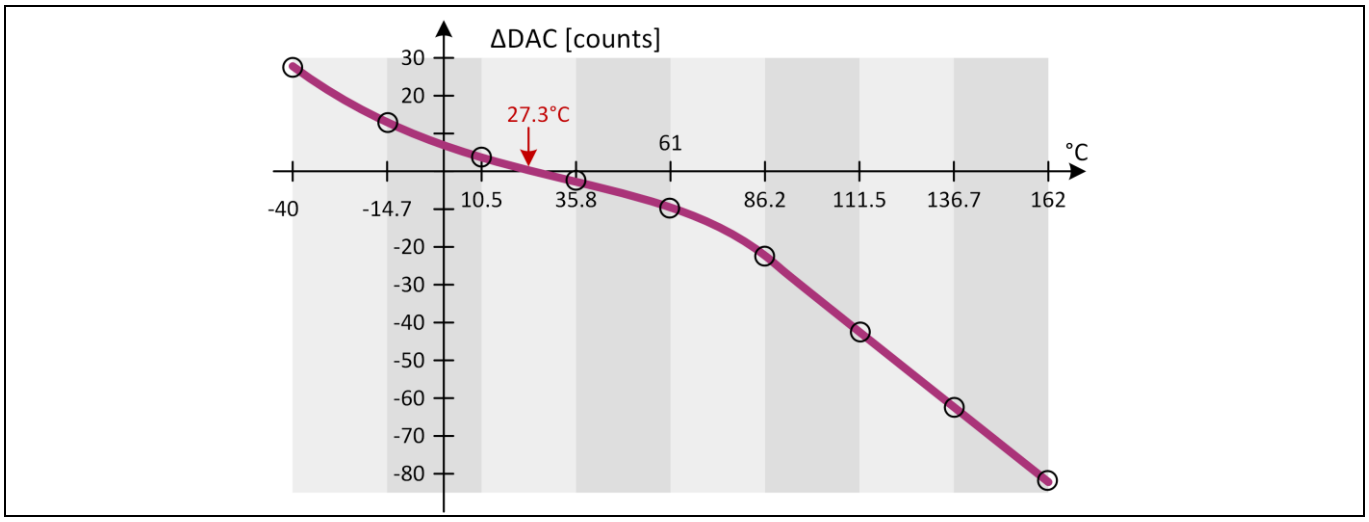

Figure 54 Delta DAC Over Temperature

The delta values can now be used to calculate the gradients as such that they best-fit the previously shown curve. Each gradient is valid for a temperature band of 24.5K. This odd number is calculated like this:
(32 counts in the TEMP.TEMPERATURE register) * (0.7648K per count).

Gradient #0 for example is used only for temperatures between -40°C … -15.5°C. Gradient #1 starts at -14.7°C (-15.5°C + 0.7648K) and ends at +9.7°C (10.5°C – 0.7648K) and so on.

A gradient describes the delta between two DAC values measured at two temperatures 8 Kelvin apart from each other. The gradients reach from -8…+7 in steps of 1 and are programmed using the two's complement:

$$\text{grad}[n] = \frac{\text{DAC deviation [counts]}}{\text{per 8 Kelvin}}$$

Decimal	Binary	Hex	Decimal	Binary	Hex
7	0111	7	-1	1111	F
6	0110	6	-2	1110	E
5	0101	5	-3	1101	D
4	0100	4	-4	1100	C
3	0011	3	-5	1011	B
2	0010	2	-6	1010	A
1	0001	1	-7	1001	9
0	0000	0	-8	1000	8

Figure 55 Gradient Two's Complement

For example if the DAC value for -40°C is 2000 counts and for -15.5°C it is 1985 counts the DAC-Delta is 15 counts. Since the temperature delta is 24.5K the gradient is calculated as:

(1985 counts - 2000 counts) / [-15.5°C – (-40.0°C)] = -15 counts / 24.5K = -4.9 counts / 8K

The nearest suitable gradient is -5 which stands for -5 counts / 8K. This procedure is repeated for each gradient.

DAC Output Voltage Configuration

Some gradient examples are shown in the following figure:

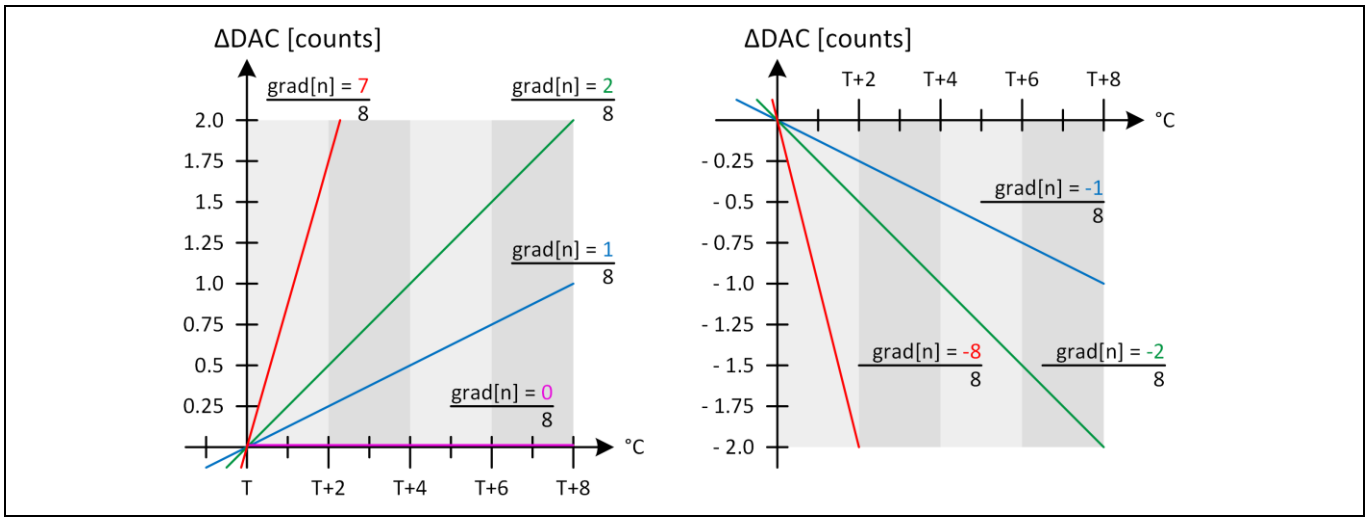

Figure 56 Gradient Examples

An example for a gradient fitted curve can be found in Figure 57. The curve from Figure 54 is shown as a white envelope:

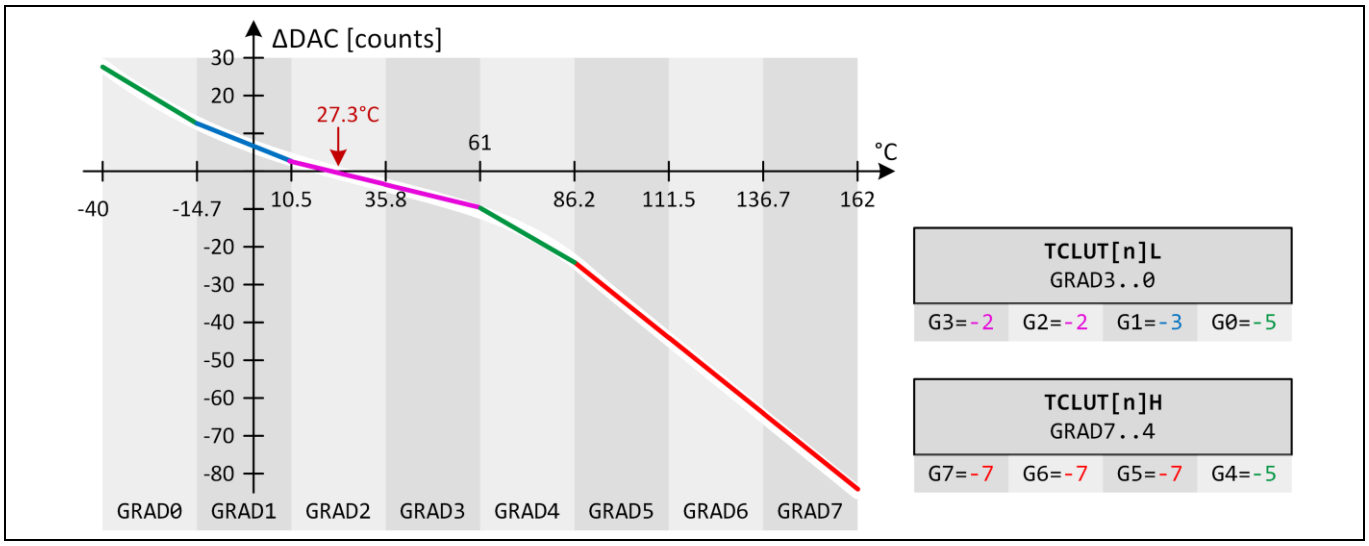

Figure 57 Gradient Example

Please note that the gradients in the registers TCLUT[n]H and TCLUT[n]L are shown with MSB on the left (gradient #0) and LSB on the right (gradient #7) while in Figure 57 they appear the other way around.

11.5 DTS: Die Temperature Sensor

The Die Temperature can be calculated from the register TEMP.TEMPERATURE according following relation:

$$T = 0.7648 \cdot TEMP.TEMPERATURE - 80.497$$

Some example values are given in the table below:

Decimal	Hex	Bin	Temperature	Decimal	Hex	Bin	Temperature	Decimal	Hex	Bin	Temperature
53	035	000110101	-40,0	151	097	010010111	35,0	250	0FA	011111010	110,7
85	055	001010101	-15,5	152	098	010011000	35,8	251	0FB	011111011	111,5
86	056	001010110	-14,7	184	0B8	010111000	60,2	283	11B	100011011	135,9
118	076	001110110	9,7	185	0B9	010111001	61,0	284	11C	100011100	136,7
119	077	001110111	10,5	217	0D9	011011001	85,5	316	13C	100111100	161,2
141	08D	010001101	27,3	218	0DA	011011010	86,2				

Figure 58 DTS Temperature Value Examples

12 Typical application information

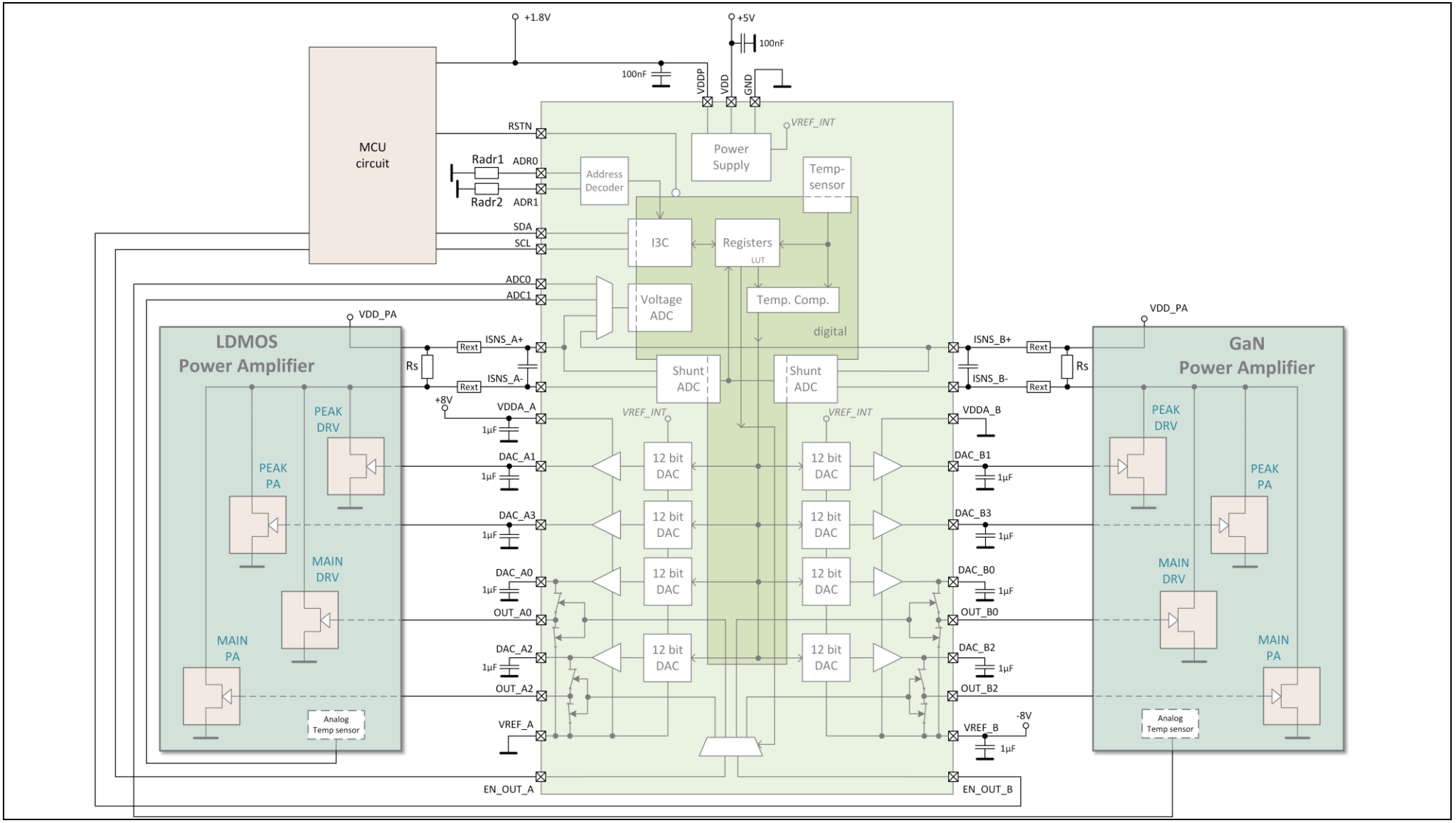

Figure 59 Typical application schematic circuit: biasing LDMOS and GaN Power Amplifiers

13 Register Map

13.1 Register summary

The registers of the Bias and Control IC provide information on actual status and measurements, and configure its hardware blocks.
The complete Register map is listed in Table 19.

Table 19 BGMC1210 Register Summary

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	r/w
0x00	VENDOR	VERSION								VENDOR								r
0x01	TEMP	RES								TEMPERATURE								r/(w)
0x02	V_ISNS_A	RES								VALUE								r
0x03	V_ISNS_B	RES								VALUE								r
0x04	ADC0	RES								VALUE								r
0x05	ADC1	RES								VALUE								r
0x06	VDD	RES								VALUE								r
0x07	VDDP	RES								VALUE								r
0x08	VDDA_A	RES								VALUE								r
0x09	VDDA_B	RES								VALUE								r
0x0A	Vref_A	RES								VALUE								r
0x0B	Vref_B	RES								VALUE								r
0x0C	I_ISNS_A	RES								VALUE								r
0x0D	I_ISNS_B	RES								VALUE								r
0x0F	DAC_FB	RES	DAC_ SIDE	DAC_CH						VALUE (read only)								r/w
0x10	ADC_EN	RES			DTS_EN	RES			VADC _EN	ISNS_B_RNG		ISNS _B_EN	ISNS_A_RNG				ISNS _A_EN	r/w
0x11	DACCNF1	TCOMP _EN	SLP			TRK_B3 toB2	TRK_B1 toB0	TRK_A3 toA2	TRK_A1 toA0	OUT_CTRL_B2		OUT_CTRL_B0		OUT_CTRL_A2		OUT_CTRL_A0		r/w
0x12	DACCNF2	LD_B3		LD_B2		LD_B1		LD_B0		LD_A3		LD_A2		LD_A1		LD_A0		r/w
0x13	VCLMP_A	DVAL_A2						SEL_A2		DVAL_A0						SEL_A0		r/w
0x14	VCLMP_B	DVAL_B2						SEL_B2		DVAL_B0						SEL_B0		r/w
0x15	DAC_A0	EN	RNG	OFFS		VALUE												r/w
0x16	DAC_A1	EN	RNG	OFFS		VALUE												r/w

Register Map

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	r/w
0x17	DAC_A2	EN	RNG	OFFS		VALUE												r/w
0x18	DAC_A3	EN	RNG	OFFS		VALUE												r/w
0x19	DAC_B0	EN	RNG	OFFS		VALUE												r/w
0x1A	DAC_B1	EN	RNG	OFFS		VALUE												r/w
0x1B	DAC_B2	EN	RNG	OFFS		VALUE												r/w
0x1C	DAC_B3	EN	RNG	OFFS		VALUE												r/w
0x1D	TCLUT_A0_L	grad3				grad2				grad1				grad0				r/w
0x1E	TCLUT_A0_H	grad7				grad6				grad5				grad4				r/w
0x1F	TCLUT_A1_L	grad3				grad2				grad1				grad0				r/w
0x20	TCLUT_A1_H	grad7				grad6				grad5				grad4				r/w
0x21	TCLUT_A2_L	grad3				grad2				grad1				grad0				r/w
0x22	TCLUT_A2_H	grad7				grad6				grad5				grad4				r/w
0x23	TCLUT_A3_L	grad3				grad2				grad1				grad0				r/w
0x24	TCLUT_A3_H	grad7				grad6				grad5				grad4				r/w
0x25	TCLUT_B0_L	grad3				grad2				grad1				grad0				r/w
0x26	TCLUT_B0_H	grad7				grad6				grad5				grad4				r/w
0x27	TCLUT_B1_L	grad3				grad2				grad1				grad0				r/w
0x28	TCLUT_B1_H	grad7				grad6				grad5				grad4				r/w
0x29	TCLUT_B2_L	grad3				grad2				grad1				grad0				r/w
0x2A	TCLUT_B2_H	grad7				grad6				grad5				grad4				r/w
0x2B	TCLUT_B3_L	grad3				grad2				grad1				grad0				r/w
0x2C	TCLUT_B3_H	grad7				grad6				grad5				grad4				r/w
0x2D	CCOMP_A0	EN	RES	AMP						SLP								r/w
0x2E	CCOMP_A2	EN	RES	AMP						SLP								r/w
0x2F	CCOMP_B0	EN	RES	AMP						SLP								r/w
0x30	CCOMP_B2	EN	RES	AMP						SLP								r/w

13.2 Register details

The registers of BGMC1210 are described below in detail.

13.2.1 VENDOR register

Address: **00_h**

Name: **VENDOR**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VERSION								VENDOR							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Table 20 VENDOR register details

Bit	Field	Type	Default	Description
15-8	VERSION	r	00_h	Version code
7-0	VENDOR	r	02_h	Vendor code

13.2.2 TEMP register

Address: **01_h**

Name: **TEMP**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES							TEMPERATURE								
Default:	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0

Table 21 TEMP register details

Bit	Field	Type	Default	Description
15-9	RES	r/(w)	00_h	Reserved bits
8-0	TEMPERATURE	r/(w)	$08C_h$	DTS enabled: actual measured die temperature (read only) DTS disabled: temperature for temperature compensation needs to be written here (read/write access)

13.2.3 V_ISNS_A register

Address: **02_h**

Name: **V_ISNS_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 22 V_ISNS_A register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits

Bit	Field	Type	Default	Description
10-0	VALUE	r	000_h	11 bit result of VADC measured at ISNS_A+

13.2.4 V_ISNS_B register

Address: **03_h**

Name: **V_ISNS_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 23 V_ISNS_B register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at ISNS_B+

13.2.5 ADC0 register

Address: **04_h**

Name: **ADC0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 24 ADC0 register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at ADC0

13.2.6 ADC1 register

Address: **05_h**

Name: **ADC1**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 25 ADC1 register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at ADC1

13.2.7 VDD register

Address: **06_h**

Name: **VDD**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 26 VDD register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at VDD

13.2.8 VDDP register

Address: **07_h**

Name: **VDDP**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 27 VDDP register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at VDDP

13.2.9 VDDA_A register

Address: **08_h**

Name: **VDDA_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 28 VDDA_A register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at VDDA_A

13.2.10 VDDA_B register

Address: **09h**

Name: **VDDA_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 29 VDDA_B register details

Bit	Field	Type	Default	Description
15-11	RES	r	00h	Reserved bits
10-0	VALUE	r	000h	11 bit result of VADC measured at VDDA_B

13.2.11 Vref_A register

Address: **0Ah**

Name: **Vref_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 30 Vref_A register details

Bit	Field	Type	Default	Description
15-11	RES	r	00h	Reserved bits
10-0	VALUE	r	000h	11 bit result of VADC measured at Vref_A

13.2.12 Vref_B register

Address: **0Bh**

Name: **Vref_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 31 Vref_B register details

Bit	Field	Type	Default	Description
15-11	RES	r	00h	Reserved bits
10-0	VALUE	r	000h	11 bit result of VADC measured at Vref_B

13.2.13 I_ISNS_A register

Address: **0C$_h$**

Name: **I_SNS_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES				VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 32 I_ISNS_A register details

Bit	Field	Type	Default	Description
15-12	RES	r	0_h	Reserved bits
11-0	VALUE	r	000_h	12 bit result of Current Shunt ADC measured across (ISNS_A+ - ISNS_A-)

13.2.14 I_ISNS_B register

Address: **0D$_h$**

Name: **I_SNS_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES				VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 33 I_ISNS_B register details

Bit	Field	Type	Default	Description
15-12	RES	r	0_h	Reserved bits
11-0	VALUE	r	000_h	12 bit result of Current Shunt ADC measured across (ISNS_B+ - ISNS_B-)

13.2.15 DAC feedback register

Address: **0F$_h$**

Name: **DAC_FB**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES	DAC_SIDE	DAC_CH		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 34 DAC_FB register details

Bit	Field	Type	Default	Description
15	RES	r/w	0_b	Reserved bit
14	DAC_SIDE	r/w	0_b	0_b: side A 1_b: side B
13-12	DAC_CH	r/w	00_b	Channel of DAC: 00_b: 0 01_b: 1

Bit	Field	Type	Default	Description
				10_b: 2 11_b: 3
11-0	VALUE	r	000_h	Digital representation of calculated 12 bit value of selected DAC. Note: this field is read only – any data attempted to be written ill be ignored

13.2.16 ADC enable register

Address: **10_h**

Name: **ADC_EN**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES			DTS_EN	RES			VADC_EN	ISNS_B_RNG			ISNS_B_EN	ISNS_A_RNG			ISNS_A_EN
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 35 ADC_EN register details

Bit	Field	Type	Default	Description
15-13	RES	r/w	000_b	Reserved bits
12	DTS_EN	r/w	0_b	Enable Die Temperature Sensor (DTS)
11-9	RES	r/w	0_b	Reserved bit
8	VADC_EN	r/w	0_b	Enable Voltage ADC
7-5	ISNS_B_RNG	r/w	000_b	Full Scale Range of ISNS_B ADC: 000_b: 15 mV 001_b: 30 mV 010_b: 60 mV 011_b: 120 mV 100_b - 111_b: 240mV
4	ISNS_B_EN	r/w	0_b	Enable Shunt ADC B
3-1	ISNS_A_RNG	r/w	000_b	Full Scale Range of ISNS_A ADC: 000_b: 15 mV 001_b: 30 mV 010_b: 60 mV 011_b: 120 mV 100_b - 111_b: 240 mV
0	ISNS_A_EN	r/w	0_b	Enable Shunt ADC A

13.2.17 DACCNF1 register

Address: **11h**

Name: **DACCNF1**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCOMP_EN	SLP			TRK_B3 toB2	TRK_B1 toB0	TRK_A3 toA2	TRK_A1 toA0	OUT_CTRL_B2		OUT_CTRL_B0		OUT_CTRL_A2		OUT_CTRL_A0	
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 36 DACCNF1 register details

Bit	Field	Type	Default	Description
15	TCOMP_EN	r/w	0_b	Enable Temperature Compensation
14-12	SLP	r/w	000_b	Slope settings for update rate of DAC value: 000_b: immediate update (1 count per 50 ns) 001_b: 1 µs (1 count per 1 µs) 010_b: 5 µs (1 count per 5 µs) 011_b: 10 µs (1 count per 10 µs) 100_b: 100 µs (1 count per 100 µs) 101_b: 250 µs (1 count per 250 µs) 110_b: 1 ms (1 count per 1 ms) 111_b: 4 ms (1 count per 4 ms)
11	TRK_B3toB2	r/w	0_b	Enables tracking of odd DAC (DAC_B3(1), DAC_A3(1)) to the even DAC (DAC_B2(0), DAC_A2(0))
10	TRK_B1toB0	r/w	0_b	
9	TRK_A3toA2	r/w	0_b	
8	TRK_A1toA0	r/w	0_b	
7-6	OUT_CTRL_B2	r/w	0_b	OUT_CTRL_xy: 00_b: use EN_OUT_xy for controlling OUT_xy 01_b: force clamping of OUT_xy (connect to VCLMP potential) 10_b: force enable of OUT_xy (connect to DAC_xy) 11_b: use EN_OUT_!xy from other side for controlling OUT_xy (!A = B, !B = A)
5-4	OUT_CTRL_B0	r/w	0_b	
3-2	OUT_CTRL_A2	r/w	0_b	
1-0	OUT_CTRL_A0	r/w	0_b	

13.2.18 DACCNF2 register

Address: **12h**

Name: **DACCNF2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LD_B3		LD_B2		LD_B1		LD_B0		LD_A3		LD_A2		LD_A1		LD_A0	
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 37 DACCNF register details

Bit	Field	Type	Default	Description
15-14	LD_B3	r/w	00_b	LD_xy: 00_b: normal mode
13-12	LD_B2	r/w	00_b	

Bit	Field	Type	Default	Description
11-10	LD_B1	r/w	00_b	01_b: enables high current mode 10_b, 11_b: enables stability for low cap values in normal mode
9-8	LD_B0	r/w	00_b	
7-6	LD_A3	r/w	00_b	
5-4	LD_A2	r/w	00_b	
3-2	LD_A1	r/w	00_b	
1-0	LD_A0	r/w	00_b	

13.2.19 VCLMP_A register

Address: **13_h**

Name: **VCLMP_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DVAL_A2						SEL_A2		DVAL_A0						SEL_A0	
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1 VCLMP_A register details

Bit	Field	Type	Default	Description
15-10	DVAL_A2	r/w	00_h	Value of delta voltage referred to DAC_A2
9-8	SEL_A2	r/w	00_b	Select clamping potential: 00_b: VREF_A 01_b: DAC_A3 (also enables DAC_A3) 10_b, 11_b: VCLMP buffer
7-2	DVAL_A0	r/w	00_h	Value of delta voltage referred to DAC_A0
1-0	SEL_A0	r/w	00_b	Select clamping potential: 00_b: VREF_A 01_b: DAC_A1 (also enables DAC_A1) 10_b, 11_b: VCLMP buffer

13.2.20 VCLMP_B register

Address: **14_h**

Name: **VCLMP_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DVAL_B2						SEL_B2		DVAL_B0						SEL_B0	
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2 VCLMP_A register details

Bit	Field	Type	Default	Description
15-10	DVAL_B2	r/w	00_h	Value of delta voltage referred to DAC_B2
9-8	SEL_B2	r/w	00_b	Select clamping potential: 00_b: VREF_B 01_b: DAC_B3 (also enables DAC_B3)

Bit	Field	Type	Default	Description
				10_b, 11_b: VCLMP buffer
7-2	DVAL_B0	r/w	00_h	Value of delta voltage referred to DAC_B0
1-0	SEL_B0	r/w	00_b	Select clamping potential: 00_b: VREF_B 01_b: DAC_B1 (also enables DAC_B1) 10_b, 11_b: VCLMP buffer

13.2.21 DAC_A0 register

Address: **15_h**

Name: **DAC_A0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3 DAC_A0 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_A0
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_A0 output value

13.2.22 DAC_A1 register

Address: **16_h**

Name: **DAC_A1**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4 DAC_A1 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_A1
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V

Bit	Field	Type	Default	Description
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_A1 output value

13.2.23 DAC_A2 register

Address: **17_h**

Name: **DAC_A2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5 DAC_A2 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_A2
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_A2 output value

13.2.24 DAC_A3 register

Address: **18_h**

Name: **DAC_A3**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6 DAC_A3 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_A3
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V

Bit	Field	Type	Default	Description
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 3.0V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_A3 output value

13.2.25 DAC_B0 register

Address: **19_h**

Name: **DAC_B0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7 DAC_B0 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_B0
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_B0 output value

13.2.26 DAC_B1 register

Address: **$1A_h$**

Name: **DAC_B1**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8 DAC_B1 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_B1
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V

Bit	Field	Type	Default	Description
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_B1 output value

13.2.27 DAC_B2 register

Address: **$1B_h$**

Name: **DAC_B2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9 DAC_B2 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_B2
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_B2 output value

13.2.28 DAC_B3 register

Address: **$1C_h$**

Name: **DAC_B3**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 10 DAC_B3 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_B3
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V

Bit	Field	Type	Default	Description
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_B3 output value

13.2.29 TCLUT_A0_L register

Address: **$1D_h$**

Name: **TCLUT_A0_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 11 TCLUT_A0_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	LUT1: 4 Low half-bytes for temperature compensation of DAC_A0 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0_h	
7-4	grad1	r/w	0_h	
3-0	grad0	r/w	0_h	

13.2.30 TCLUT_A0_H register

Address: **$1E_h$**

Name: **TCLUT_A0_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 12 TCLUT_A0_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT1: 4 High half-bytes for temperature compensation of DAC_A0 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

13.2.31 TCLUT_A1_L register

Address: **1F$_h$**

Name: **TCLUT_A1_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 13 TCLUT_A1_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	LUT2: 4 Low half-bytes for temperature compensation of DAC_A1 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0_h	
7-4	grad1	r/w	0_h	
3-0	grad0	r/w	0_h	

13.2.32 TCLUT_A1_H register

Address: **20$_h$**

Name: **TCLUT_A1_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 14 TCLUT_A1_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT2: 4 High half-bytes for temperature compensation of DAC_A1 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

13.2.33 TCLUT_A2_L register

Address: **21$_h$**

Name: **TCLUT_A2_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15 TCLUT_A2_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	
11-8	grad2	r/w	0_h	

Bit	Field	Type	Default	Description
7-4	grad1	r/w	0_h	LUT3: 4 Low half-bytes for temperature compensation of DAC_A2 (signed values for each gradient -8 to 7)
3-0	grad0	r/w	0_h	

13.2.34 TCLUT_A2_H register

Address: **22_h**

Name: **TCLUT_A2_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 16 TCLUT_A2_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT3: 4 High half-bytes for temperature compensation of DAC_A2 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

13.2.35 TCLUT_A3_L register

Address: **23_h**

Name: **TCLUT_A3_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17 TCLUT_A3_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	LUT4: 4 Low half-bytes for temperature compensation of DAC_A3 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0_h	
7-4	grad1	r/w	0_h	
3-0	grad0	r/w	0_h	

13.2.36 TCLUT_A3_H register

Address: **24_h**

Name: **TCLUT_A3_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18 TCLUT_A3_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT4: 4 High half-bytes for temperature compensation of DAC_A3 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

13.2.37 TCLUT_B0_L register

Address: **25_h**

Name: **TCLUT_B0_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 19 TCLUT_B0_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	LUT5: 4 Low half-bytes for temperature compensation of DAC_B0 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0_h	
7-4	grad1	r/w	0_h	
3-0	grad0	r/w	0_h	

13.2.38 TCLUT_B0_H register

Address: **26_h**

Name: **TCLUT_B0_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 20 TCLUT_B0_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT5: 4 High half-bytes for temperature compensation of DAC_B0 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

13.2.39 TCLUT_B1_L register

Address: **27h**

Name: **TCLUT_B1_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 21 TCLUT_B1_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0h	LUT6: 4 Low half-bytes for temperature compensation of DAC_B1 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0h	
7-4	grad1	r/w	0h	
3-0	grad0	r/w	0h	

13.2.40 TCLUT_B1_H register

Address: **28h**

Name: **TCLUT_B1_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 22 TCLUT_B1_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0h	LUT6: 4 High half-bytes for temperature compensation of DAC_B1 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0h	
7-4	grad5	r/w	0h	
3-0	grad4	r/w	0h	

13.2.41 TCLUT_B2_L register

Address: **29h**

Name: **TCLUT_B2_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 23 TCLUT_B2_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0h	
11-8	grad2	r/w	0h	

Bit	Field	Type	Default	Description
7-4	grad1	r/w	0_h	LUT7: 4 Low half-bytes for temperature compensation of DAC_B2 (signed values for each gradient -8 to 7)
3-0	grad0	r/w	0_h	

13.2.42 TCLUT_B2_H register

Address: **$2A_h$**

Name: **TCLUT_B2_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 24 TCLUT_B2_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT7: 4 High half-bytes for temperature compensation of DAC_B2 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

13.2.43 TCLUT_B3_L register

Address: **$2B_h$**

Name: **TCLUT_B3_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 25 TCLUT_B3_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	LUT8: 4 Low half-bytes for temperature compensation of DAC_B3 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0_h	
7-4	grad1	r/w	0_h	
3-0	grad0	r/w	0_h	

13.2.44 TCLUT_B3_H register

Address: **$2C_h$**

Name: **TCLUT_B3_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 26 TCLUT_B3_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT8: 4 High half-bytes for temperature compensation of DAC_B3 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

13.2.45 CCOMP_A0 register

Address: **$2D_h$**

Name: **CCOMP_A0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RES	AMP						SLP							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 27 CCOMP_A0 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable clamping compensation
14	RES	r/w	0_b	Reserved bit
13-8	AMP	r/w	00_h	Amplitude setting: preliminary offset (in LSB) during OUT_EN_x=0
7-0	SLP	r/w	00_h	Returning slope update rate (multiples of 1 µs per decrement)

13.2.46 CCOMP_A2 register

Address: **$2E_h$**

Name: **CCOMP_A2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RES	AMP						SLP							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 28 CCOMP_A2 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable clamping compensation
14	RES	r/w	0_b	Reserved bit
13-8	AMP	r/w	00_h	Amplitude setting: preliminary offset (in LSB) during OUT_EN_x=0
7-0	SLP	r/w	00_h	Returning slope update rate (multiples of 1 µs per decrement)

13.2.47 CCOMP_B0 register

Address: **2F$_h$**

Name: **CCOMP_B0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RES	AMP						SLP							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 29 CCOMP_B0 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable clamping compensation
14	RES	r/w	0_b	Reserved bit
13-8	AMP	r/w	00_h	Amplitude setting: preliminary offset (in LSB) during OUT_EN_x=0
7-0	SLP	r/w	00_h	Returning slope update rate (multiples of 1 µs per decrement)

13.2.48 CCOMP_B2 register

Address: **30$_h$**

Name: **CCOMP_B2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RES	AMP						SLP							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 30 CCOMP_B2 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable clamping compensation
14	RES	r/w	0_b	Reserved bit
13-8	AMP	r/w	00_h	Amplitude setting: preliminary offset (in LSB) during OUT_EN_x=0
7-0	SLP	r/w	00_h	Returning slope update rate (multiples of 1 µs per decrement)

14 Package Outline

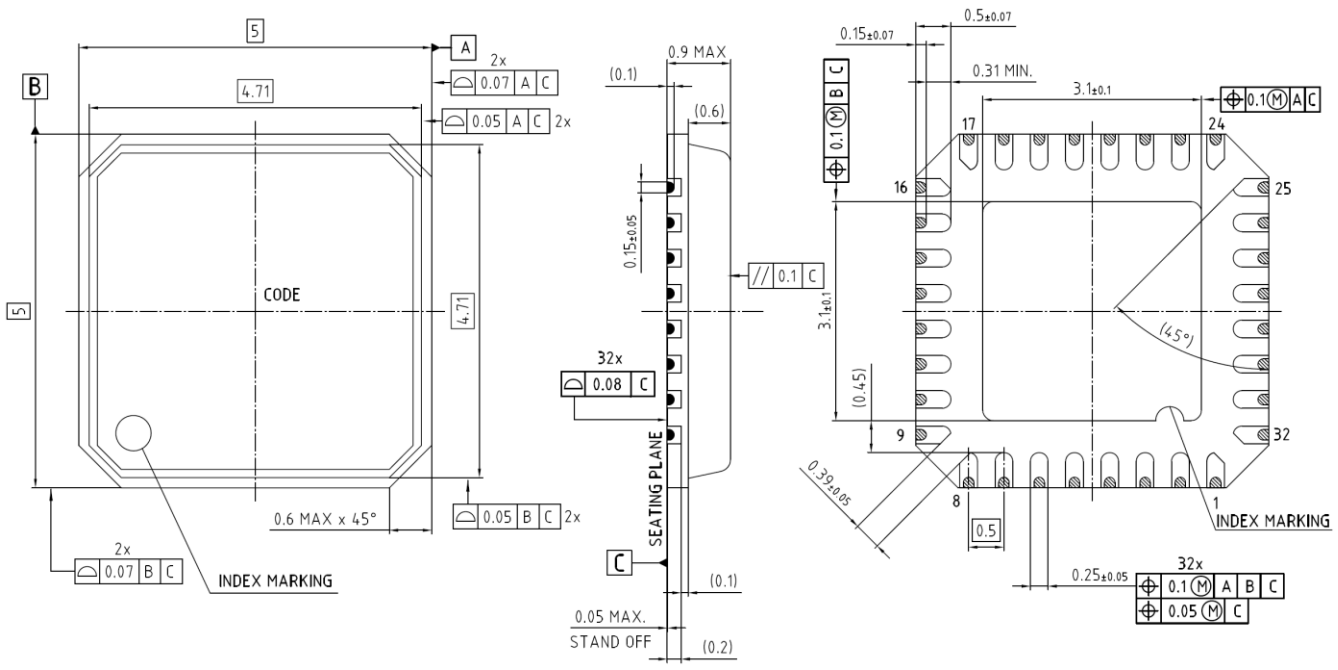

Figure 60 PG-VQFN-32-21 package outline

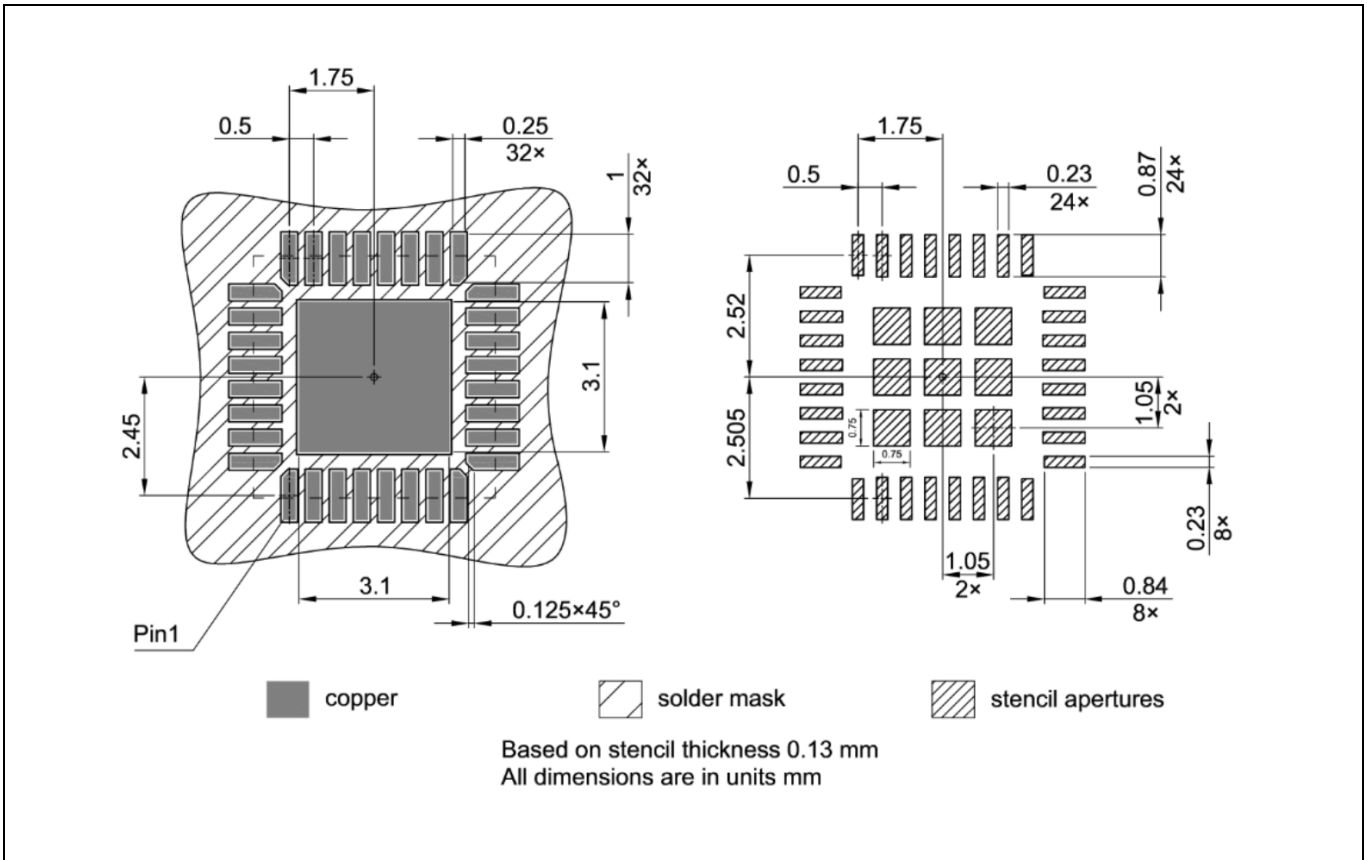

Figure 61 PG-VQFN-32-21 PCB footprint

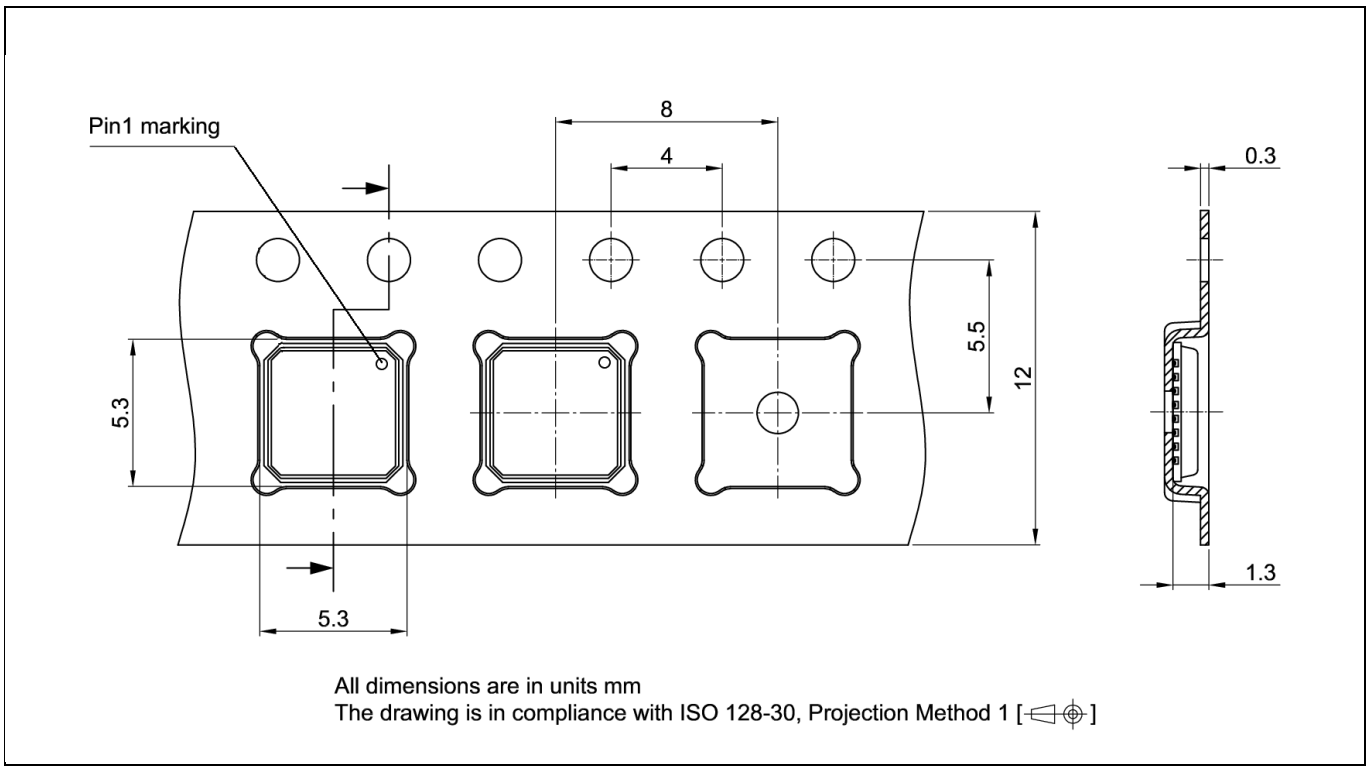

Figure 62 PG-VQFN-32-21 Tape information

Revision history

Document version	Date of release	Description of changes
V 1.0	2021-07-16	Initial version
V 1.1	2021-09-03	Package drawing update
V 1.2	2021-10-22	Features, electrical characteristics, tape information update
V1.3	2022-03-21	Features, electrical characteristics, multiple sections update, register map update
V1.4	2022-08-22	Corrections, Table 3.5.8 Digital logic added
V1.5	2023-02-13	DTS accuracy updated; Digital interface section updated; Added sections: Functional behavior, DAC Output Voltage configuration, Typical application information

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