MP28164

High-Efficiency, Single-Inductor, Buck-Boost Converter with 4.2A Switches

The Future of Analog IC Technology

DESCRIPTION

The MP28164 is a high-efficiency, low-quiescent current, buck-boost converter that operates from an input voltage above, equal to, or below the output voltage. The device provides a compact solution for products powered by one-cell Lithium-Ion or multi-cell alkaline batteries where the output voltage is within the battery voltage range.

The MP28164 uses current-mode control with fixed PWM frequency for optimal stability and transient response. The fixed 2MHz switching frequency and integrated low $R_{DS(ON)}$ MOSFETs minimize the solution footprint while maintaining high efficiency.

To ensure the longest possible battery life, the MP28164 uses an optional pulse skipping mode that reduces the switching frequency under light-load conditions. For other low-noise applications where pulse skipping mode may cause interference, a high-logic input on MODE/SYNC guarantees fixed-frequency PWM operation under all load conditions.

The MP28164 operates with an input voltage from 1.2V to 5.5V to provide an adjustable output voltage from 1.5V to 5V. With an input from 2.5V to 5.5V, the device can supply 2A of current to the load with a 3.3V output voltage.

The MP28164 is available in a small QFN-11 (2mmx3mm) package.

FEATURES

- 1.8V Minimum Start-Up Input Voltage
- 1.2V to 5.5V Input Work Range
- 1.5V to 5V Output Range
- 4.2A Switching Current Limit
- 3.3V/2A Load Capability from a 2.5V-to-5.5V Input Supply
- 2MHz Fixed or External Synchronous Switching Frequency
- Selectable PSM/PWM Mode
- Typical 25μA Quiescent Current
- High Efficiency up to 95%
- Load Disconnect during Shutdown
- Internal Soft Start and Compensation
- Power Good Indicator
- Hiccup Mode for Short-Circuit Protection (SCP)
- Over-Temperature Protection (OTP)
- Available in a Small QFN-11 (2mmx3mm) Package

APPLICATIONS

- Battery-Powered Devices
- Portable Instruments
- Tablet PC
- Super-Cap Charger

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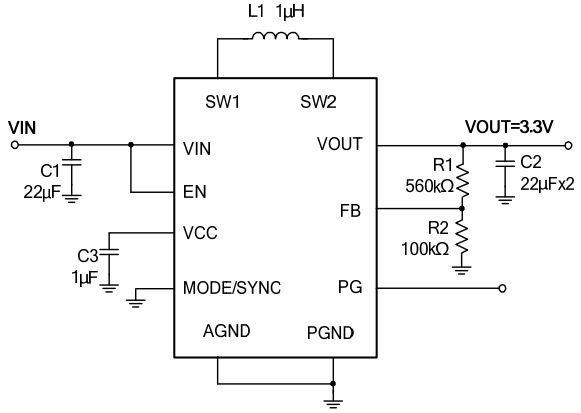
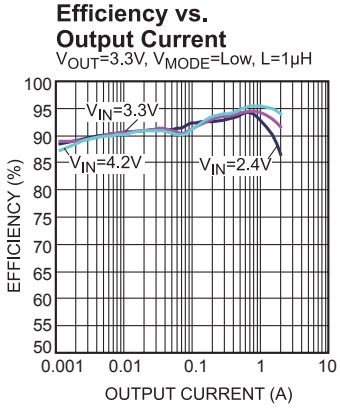
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP28164GD	QFN-11 (2mmx3mm)	*See Below*

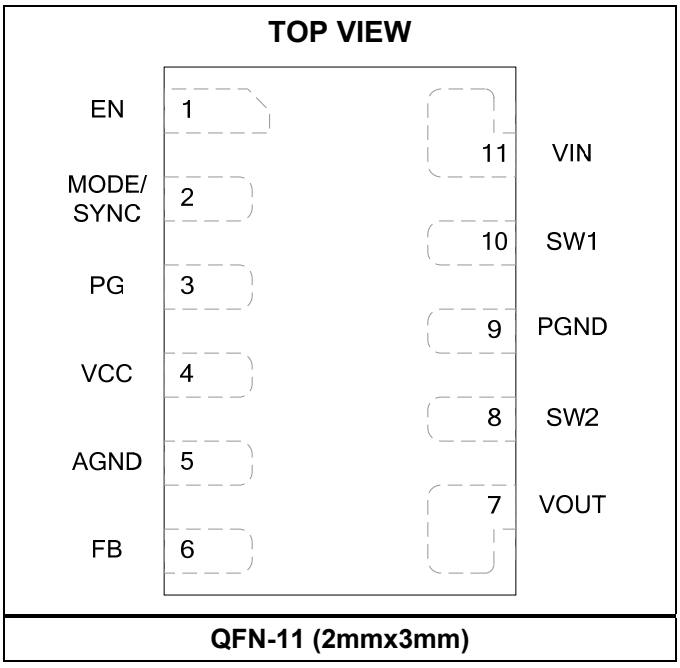
* For Tape & Reel, add suffix –Z (e.g. MP28164GD–Z)

TOP MARKING

ANA
YWW
LLL

ANA: Product code of MP28164GD
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-11 (2mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

VIN to GND .....-0.3V to 6V
SW1/2 to GND .....-0.3V (-2V for <10ns) to 6.5V (8.5V for <10ns)
All other pins .....-0.3V to 6V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = +25°C) (2)
QFN-11 (2mmx3mm)..... 1.78W
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Startup supply voltage (V_{ST}).....1.8V to 5.5V
Operation voltage (V_{IN}) .....1.2V (4) to 5.5V
Output voltage (V_{OUT}).....1.5V to 5V
Operating junction. temp. (T_J)...-40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-11 (2mmx3mm)	70	15	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) If V_{CC} is powered from a source higher than 1.8V (such as V_{OUT}), the MP28164 can work down to V_{IN} = 1.2V, but the load capability is lower when V_{IN} = 1.2V because of the high $R_{DS(ON)}$ of SWA and low current limit.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = V_{OUT} = 3.3V, T_J = -40°C to 125°C. Typical value is tested at 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN under-voltage lockout rising threshold	$V_{IN-UVLO-R}$	V_{CC} floating, V_{IN} rising, test V_{IN} when IC starts up	1.63	1.7	1.77	V
VIN under-voltage lockout falling threshold	$V_{IN-UVLO-F}$	V_{OUT} = 3.3V, V_{IN} falling		0.69		V
VCC under-voltage lockout falling threshold	$V_{CC-UVLO-F}$	V_{IN} = 1.2V, V_{CC} falling	1.45	1.56	1.67	V
Feedback voltage reference	V_{REF}	T_J = 25°C	495	500	505	mV
		T_J = -40°C to +125°C	492.5	500	507.5	mV
Oscillator frequency	F_{REQ}		1700	2000	2300	kHz
Frequency range for synchronization			1000		3000	kHz
Steady state current limit	I_{SW1}	V_{FB} > 60%V_{REF}	3.5	4.2	5	A
Start-up current limit	I_{SW2}	V_{FB} < 60%V_{REF}	1.7	2.5		A
NMOS switch on resistance	$R_{DS(ON)}$-N	SWB, SWC		22		mΩ
PMOS switch on resistance	$R_{DS(ON)}$-P	SWA, SWD		27.5		mΩ
Quiescent current	I_Q	V_{FB} = 0.55V, V_{IN} = 2.5V, V_{OUT} = 3.3V, test VOUT		25		μA
		V_{FB} = 0.55V, V_{IN} = 2.5V, V_{OUT} = 3.3V, test VIN		3.3		μA
Shutdown current	I_S	V_{EN} = 0V			3	μA
Soft-start time	T_{SS}	Internal V_{REF} from 0V to 0.5V		1.5		ms
EN/MODE input low voltage					0.4	V
EN/MODE input high voltage			1.2			V
EN input current	I_{EN}	V_{EN} = 3.3V		2.1		μA
		V_{EN} = 0V		0		μA
Power good rising threshold	PG_{VTH-HI}		87.5%	91.5%	95.5%	V_{REF}
Power good falling threshold	PG_{VTH-LO}		72%	76%	80%	V_{REF}
Power good delay	PG_{DT}	Low to high		118		μs
		High to low		19		
Power good sink current capability	V_{PG}	Sink 3mA			0.3	V
Thermal shutdown(6)	T_{SHDN}			160		°C
Thermal shutdown hysteresis(6)	T_{HYS}			20		°C

NOTE:

6) Guaranteed by characterization, not tested in production.

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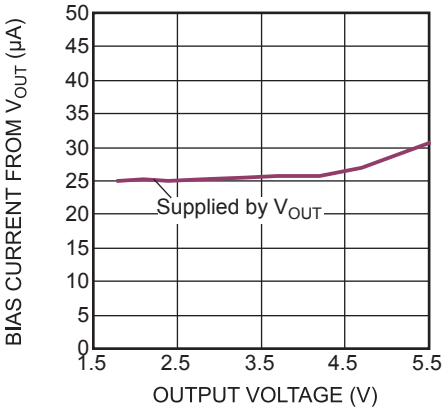
TYPICAL PERFORMANCE CHARACTERISTICS

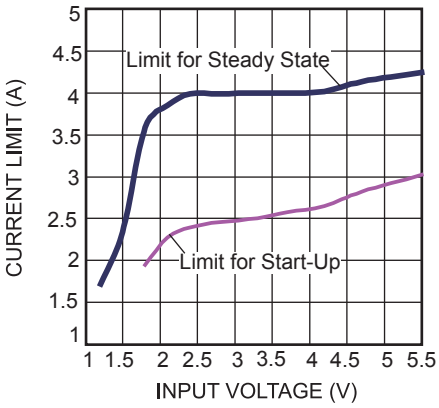
V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 2x22µF, T_A = 25°C, unless otherwise noted.

Quiescent Current

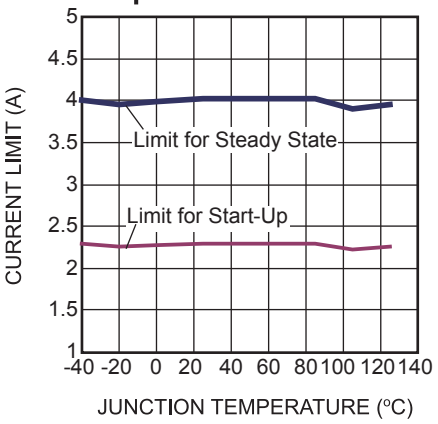
V_{IN}=1.2V, V_{EN}=High



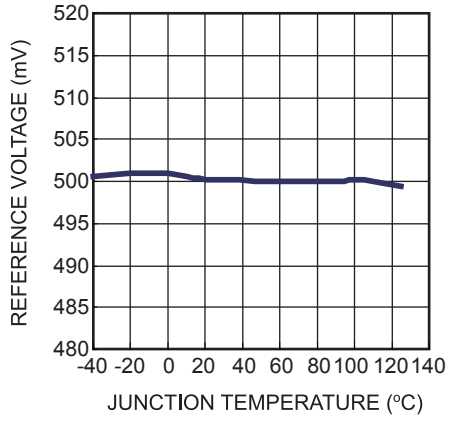
Current Limit vs. Input Voltage



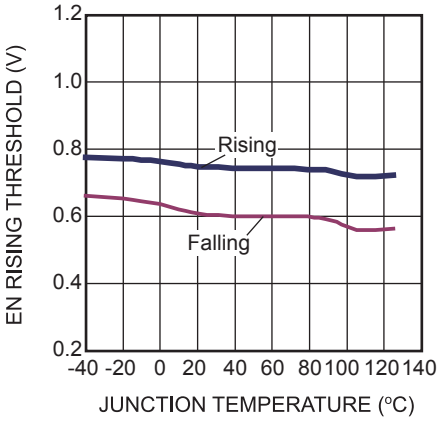
Current Limit vs. Temperature



Feedback Reference Voltage

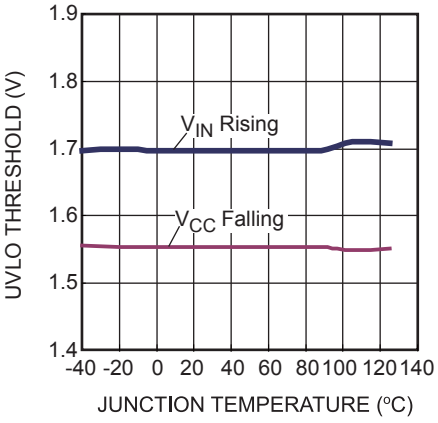


EN Threshold



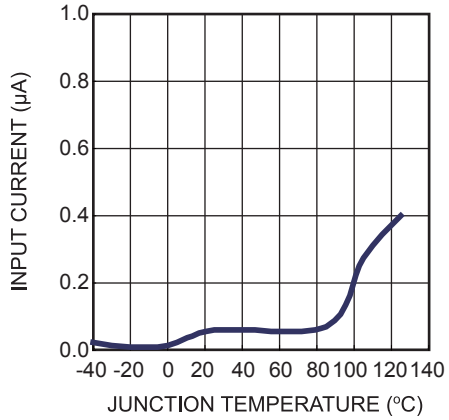
UVLO Threshold

V_{EN}=High



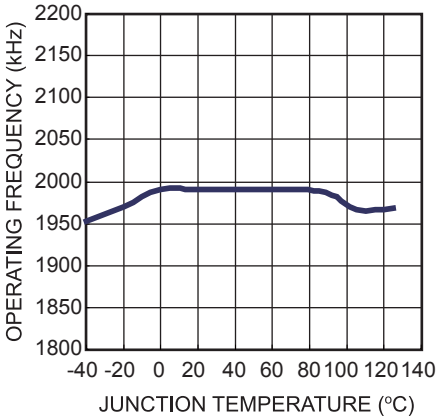
EN Shutdown Current

V_{EN}=Low



Frequency vs. Temperature

V_{MODE}=High



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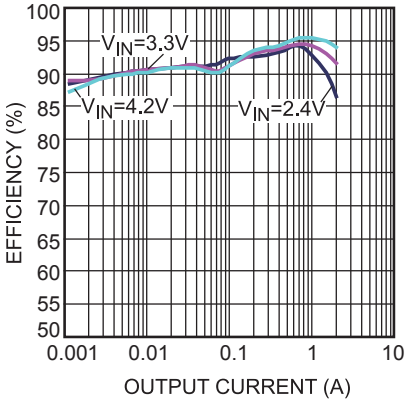
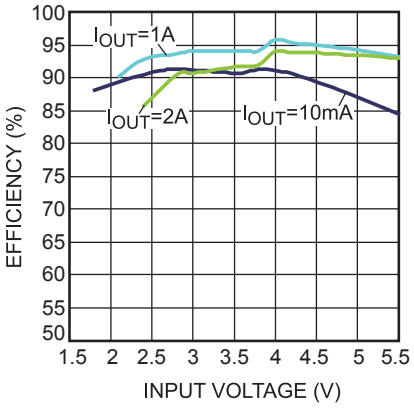
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 2x22µF, T_A = 25°C, unless otherwise noted.

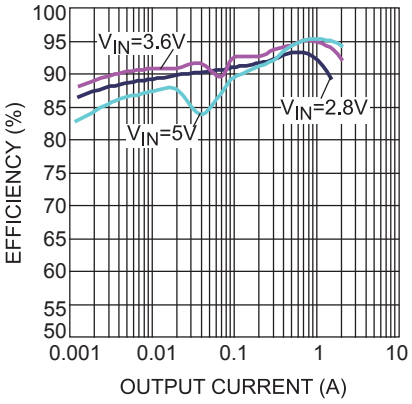
Efficiency vs. Output Current
V_{OUT}=3.3V, V_{MODE}=Low, L=1µH



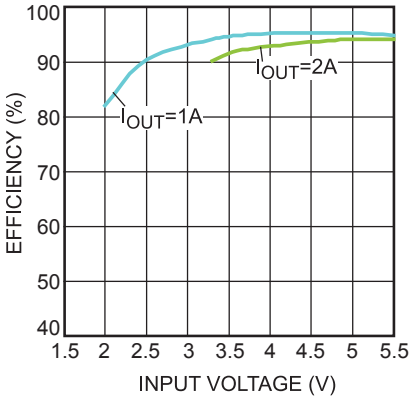
Efficiency vs. Input Voltage
V_{OUT}=3.3V, V_{MODE}=Low, L=1µH



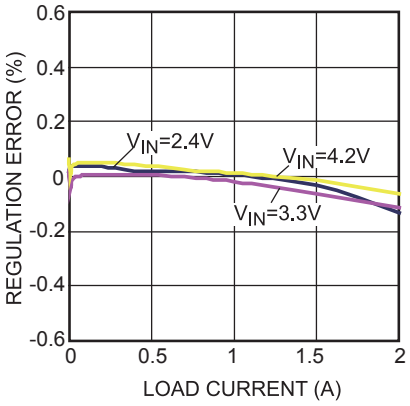
Efficiency vs. Output Current
V_{OUT}=5V, V_{MODE}=Low, L=1.5µH



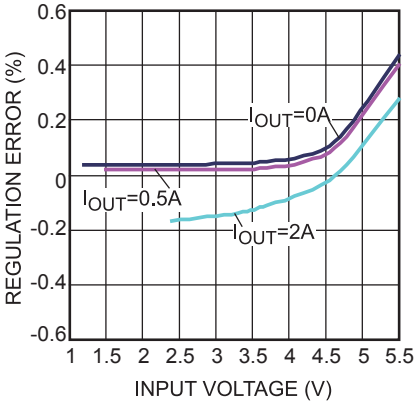
Efficiency vs. Input Voltage
V_{OUT}=5V, V_{MODE}=Low, L=1.5µH



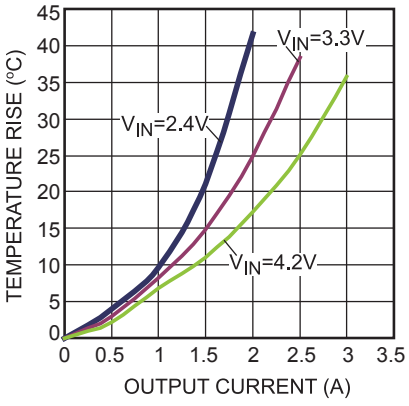
Load Regulation
V_{MODE}=High



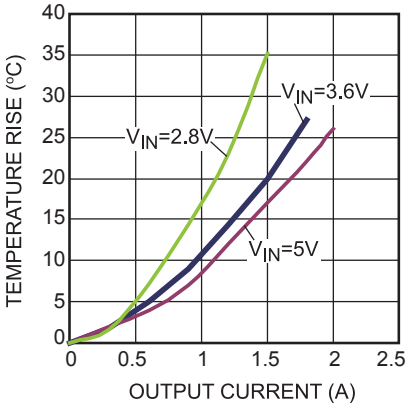
Line Regulation
V_{MODE}=High



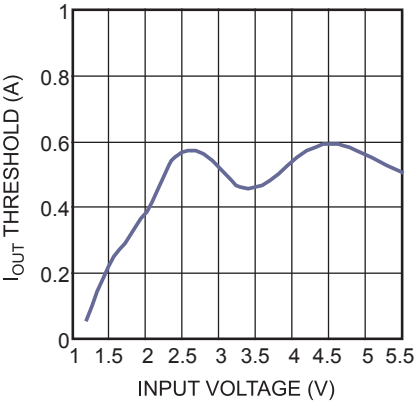
Case Temperature Rise
V_{OUT}=3.3V



Case Temperature Rise
V_{OUT}=5V



PSM to PWM Transition Threshold
V_{MODE}=Low



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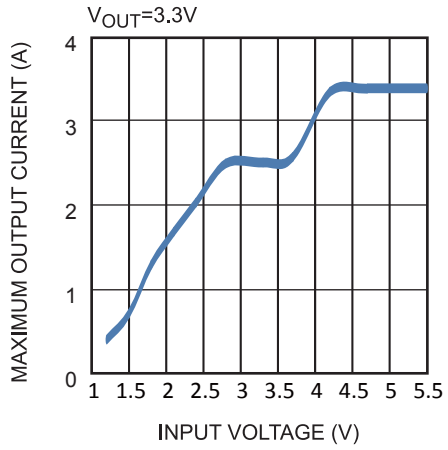
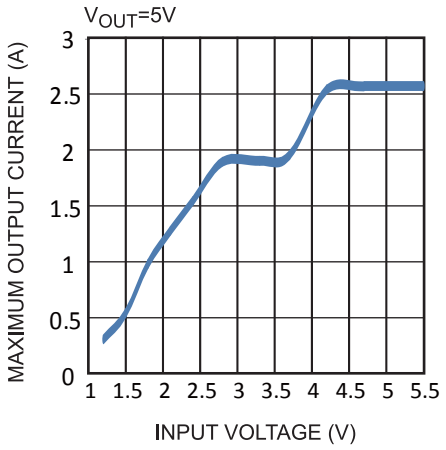
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 2x22µF, T_A = 25°C, unless otherwise noted.

Maximum Output Current vs. Input Voltage (7)



Maximum Output Current vs. Input Voltage (7)



NOTE:

7) Tested with a 3.5A inductor peak current at a 3.3V input.

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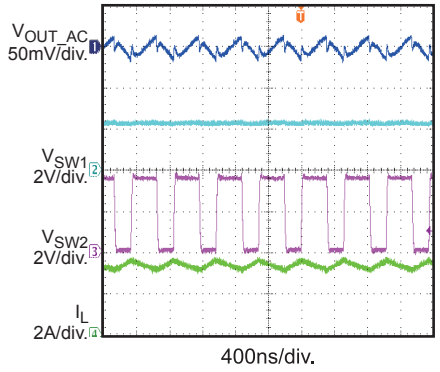
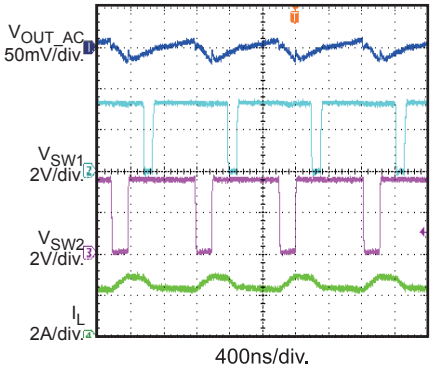
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 2x22µF, T_A = 25°C, unless otherwise noted.

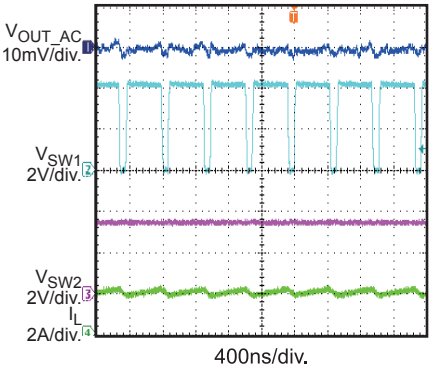
Steady State
V_{IN} = 2.4V, I_{OUT} = 2A,
V_{MODE} = High



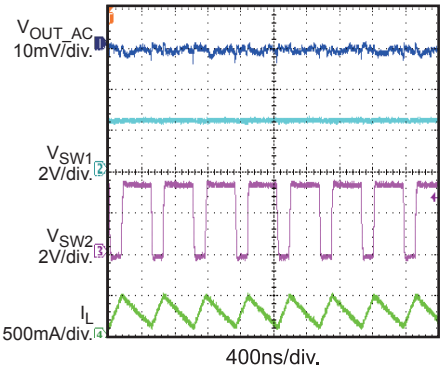
Steady State
V_{IN} = 3.3V, I_{OUT} = 2A,
V_{MODE} = High



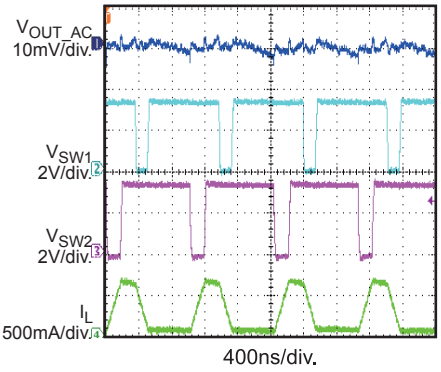
Steady State
V_{IN} = 4.2V, I_{OUT} = 2A,
V_{MODE} = High



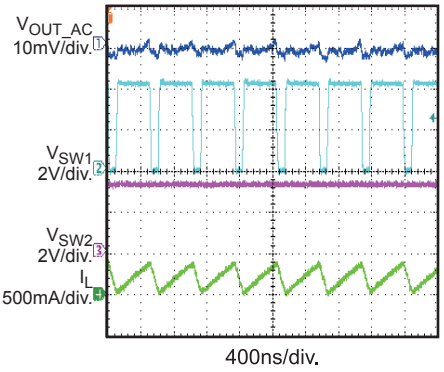
Steady State
V_{IN} = 2.4V, I_{OUT} = 0.2A,
V_{MODE} = High



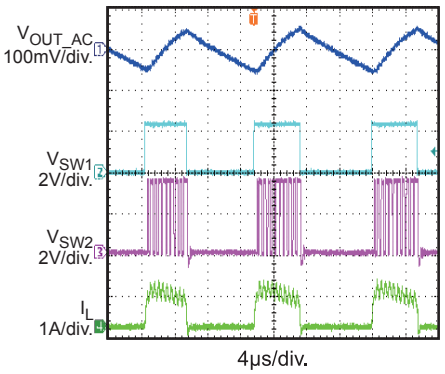
Steady State
V_{IN} = 3.3V, I_{OUT} = 0.2A,
V_{MODE} = High



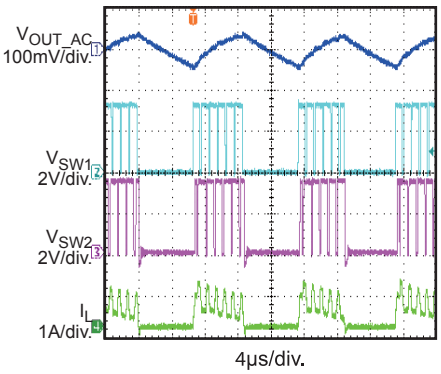
Steady State
V_{IN} = 4.2V, I_{OUT} = 0.2A,
V_{MODE} = High



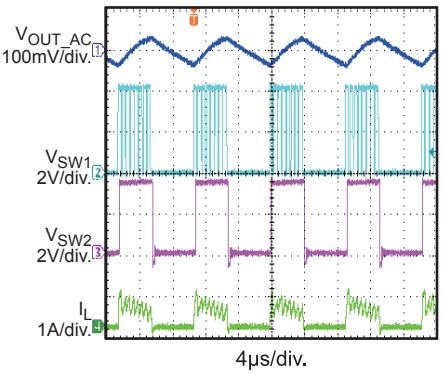
Steady State
V_{IN} = 2.4V, I_{OUT} = 0.2A,
V_{MODE} = Low



Steady State
V_{IN} = 3.3V, I_{OUT} = 0.2A,
V_{MODE} = Low



Steady State
V_{IN} = 4.2V, I_{OUT} = 0.2A,
V_{MODE} = Low



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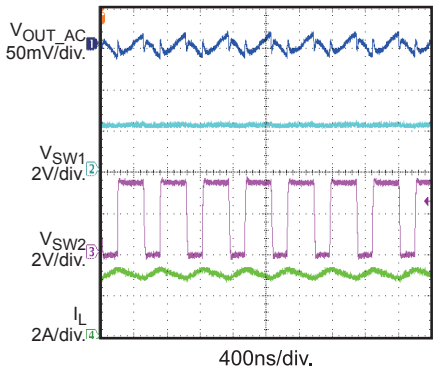
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 2x22µF, T_A = 25°C, unless otherwise noted.

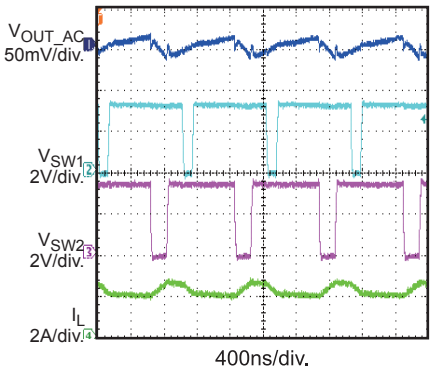
Steady State

V_{IN} = 2.4V, I_{OUT} = 2A, V_{MODE} = Low



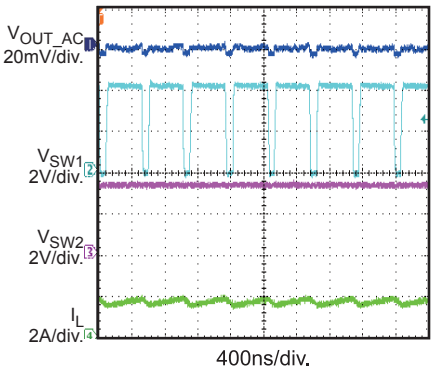
Steady State

V_{IN} = 3.3V, I_{OUT} = 2A, V_{MODE} = Low



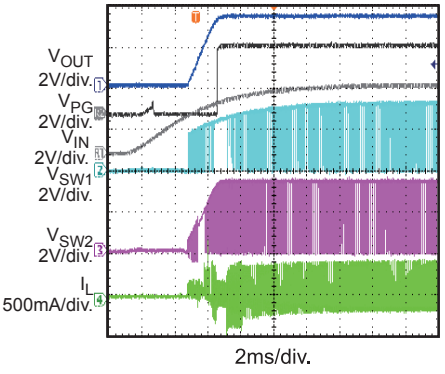
Steady State

V_{IN} = 4.2V, I_{OUT} = 2A, V_{MODE} = Low



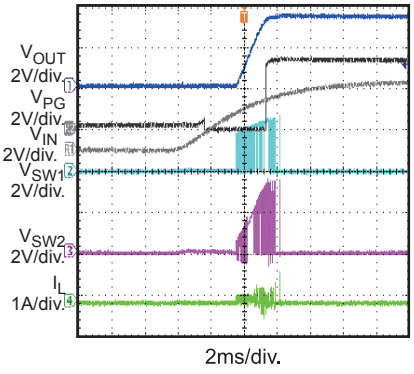
Power On

I_{OUT} = 0A, V_{MODE} = High



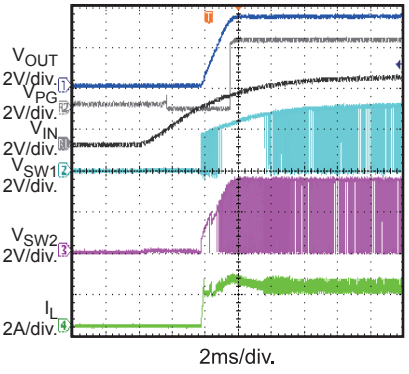
Power On

I_{OUT} = 0A, V_{MODE} = Low



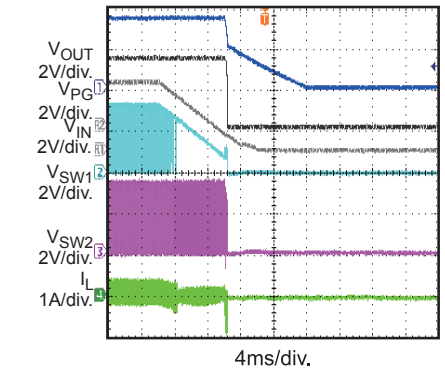
Power On

I_{OUT} = 1A, V_{MODE} = Low



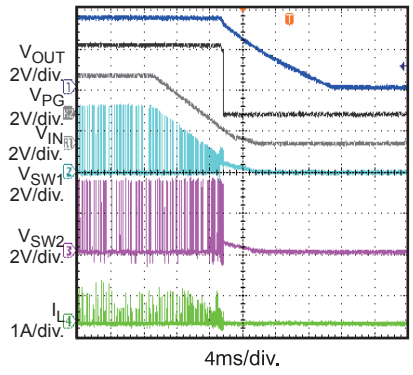
Power Off

I_{OUT} = 0.01A, V_{MODE} = High



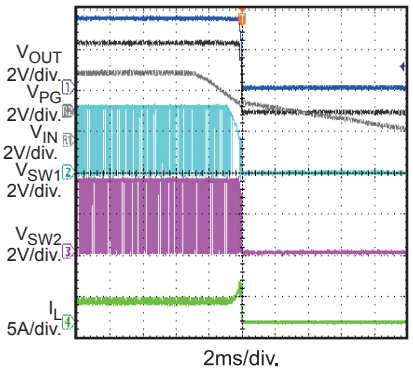
Power Off

I_{OUT} = 0.01A, V_{MODE} = Low



Power Off

I_{OUT} = 2A, V_{MODE} = Low



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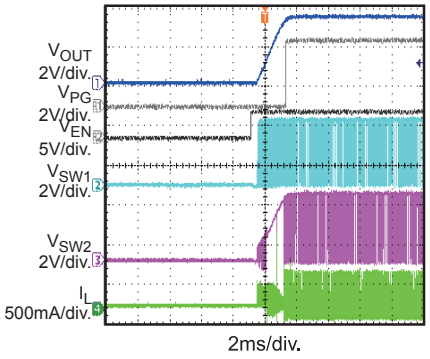
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 2x22µF, T_A = 25°C, unless otherwise noted.

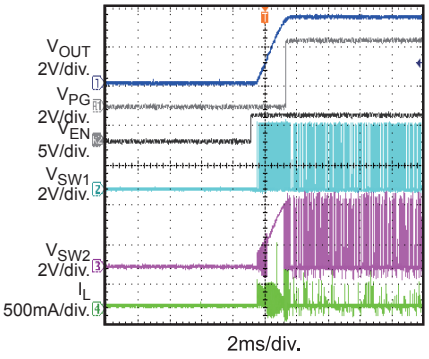
EN Start-Up

I_{OUT} = 0A, V_{MODE} = High



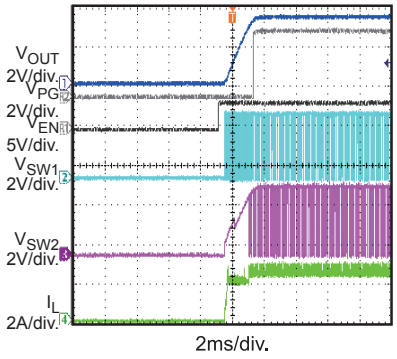
EN Start-Up

I_{OUT} = 0A, V_{MODE} = Low



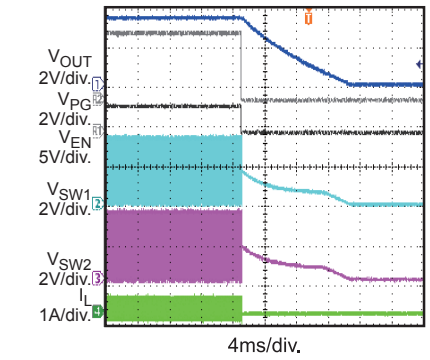
EN Start-Up

I_{OUT} = 2A, V_{MODE} = Low



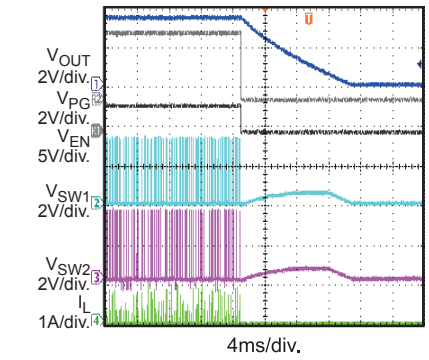
EN Shutdown

I_{OUT} = 0.01A, V_{MODE} = High



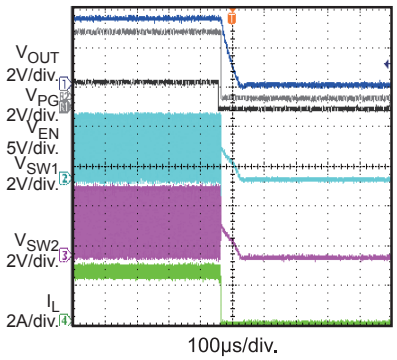
EN Shutdown

I_{OUT} = 0.01A, V_{MODE} = Low



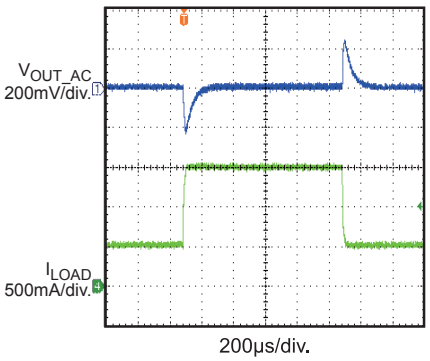
EN Shutdown

I_{OUT} = 2A, V_{MODE} = Low



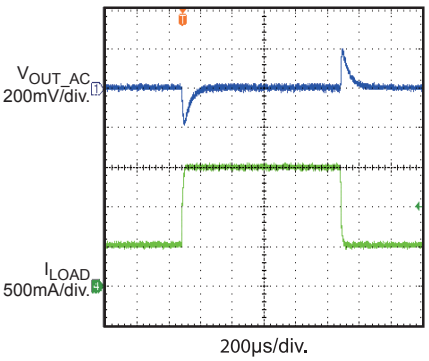
Response to Transient Load

V_{IN} = 2.4V, I_{OUT} = 0.5A to 1.5A,
V_{MODE} = High



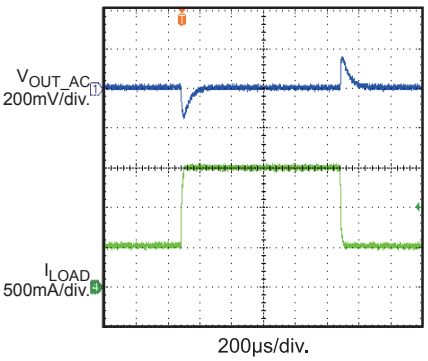
Response to Transient Load

V_{IN} = 3.3V, I_{OUT} = 0.5A to 1.5A,
V_{MODE} = High



Response to Transient Load

V_{IN} = 4.2V, I_{OUT} = 0.5A to 1.5A,
V_{MODE} = High



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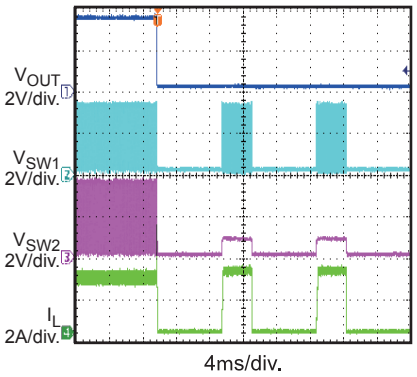
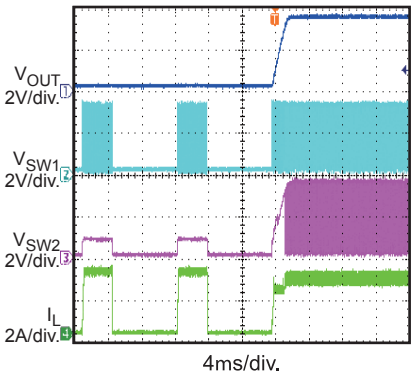
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 1µH, C_{OUT} = 2x22µF, T_A = 25°C, unless otherwise noted.

Protection for Output Short
I_{OUT} = 2A



Recovery from Output Short Protection
I_{OUT} = 2A



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PIN FUNCTIONS

Pin #	Name	Description
1	EN	**On/off control.** Pull EN high to enable the MP28164; pull EN down or leave EN floating to disable all internal circuits. EN is pulled down to AGND with 1.5MΩ internally.
2	MODE/ SYNC	**Operation mode selection.** If MODE/SYNC is low, the MP28164 switches between PSM and fixed frequency PWM automatically, according to the load level. If MODE/SYNC is high, the MP28164 works in fixed frquency PWM mode continuously. An external clock can be applied to MODE/SYNC for switching frequency synchronization. MODE/SYNC is pulled down to AGND with 1MΩ internally. MODE/SYNC should be pulled high or low through a resistor smaller than 10kΩ.
3	PG	**Power good indicator.** PG switches high and low based on the feedback voltage (FB).
4	VCC	**Supply voltage for control stage.** VCC is powered by the higher value of VIN or VOUT. Decouple VCC with a 1μF capacitor.
5	AGND	**Signal ground.**
6	FB	**Output voltage feedback.** Keep FB and its associated traces far from noise sources like SW.
7	VOUT	**Buck-boost converter output.** An output capacitor should be placed close to VOUT and PGND.
8	SW2	**Switch.** Internal switches are connected to SW2. Connect an inductor between SW1 and SW2.
9	PGND	**Power ground.**
10	SW1	**Switch.** Internal switches are connected to SW1. Connect an inductor between SW1 and SW2.
11	VIN	**Supply voltage for power stage.**

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BLOCK DIAGRAM

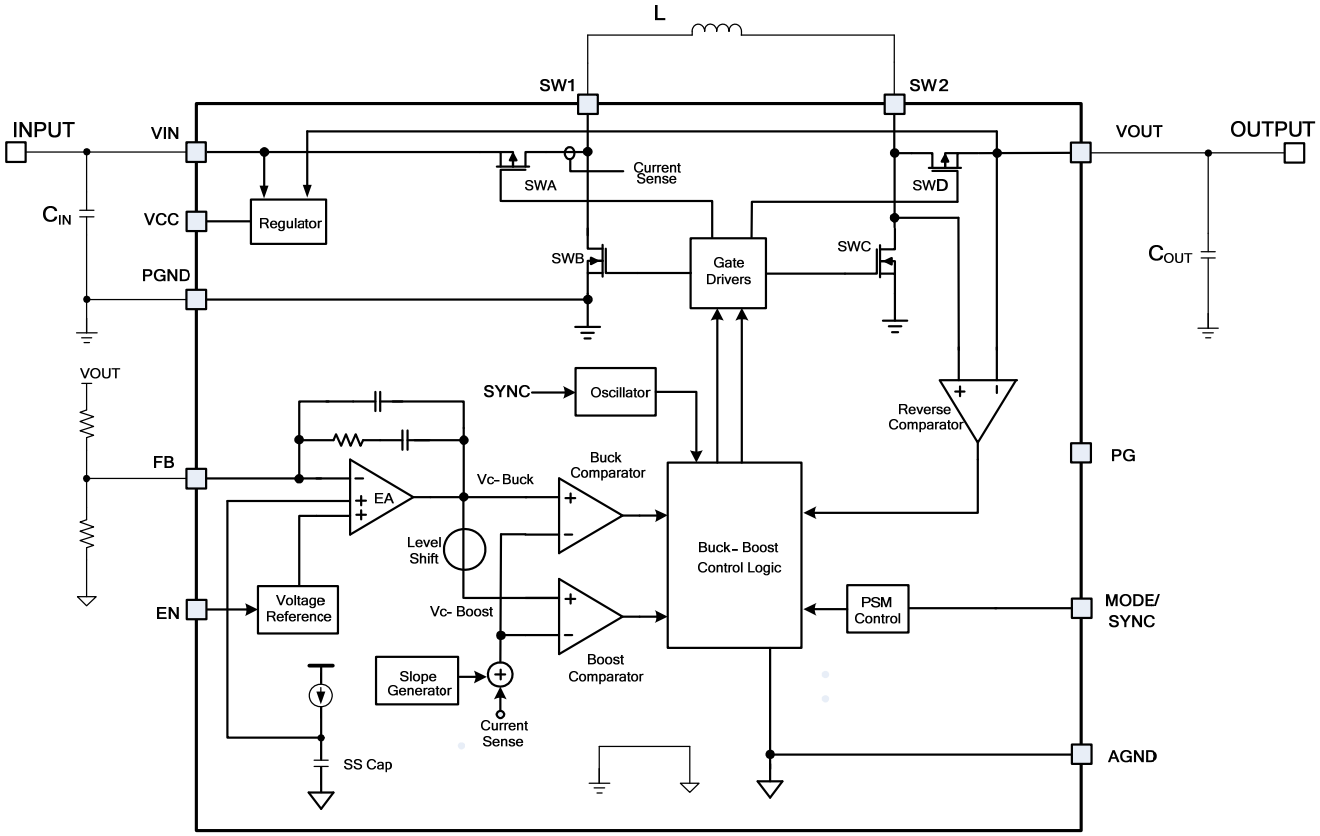

Figure 1: Functional Block Diagram

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OPERATION

The MP28164 is a high-efficiency, dual-mode, buck-boost converter that provides an output voltage above, equal to, or below the input voltage. The output voltage is sensed via FB through an external resistor divider from the output to ground (see Figure 1). The voltage difference between FB and the internal reference is amplified by the error amplifier to generate a control signal (V_{C-Buck}). By comparing V_{C-Buck} with the internal current ramp signal (the sensed SWA's current with slope compensation) through the buck comparator, a pulse-width modulation (PWM) control signal for the buck leg (SWA, SWB) is generated.

Another control signal ($V_{C-Boost}$) is derived from V_{C-Buck} through the level shift. Similarly, $V_{C-Boost}$ is compared with the same ramp signal through the boost comparator and generates a PWM control signal for the boost leg (SWC, SWD). The switch topology for the buck-boost converter is shown in Figure 2.

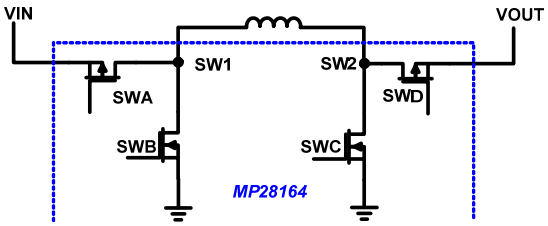

Figure 2: **Buck-Boost Switch Topology**

Buck Region (VIN > VOUT)

When the input voltage is significantly higher than the output voltage, the converter can deliver energy to the load within SWA's maximum duty cycle by switching SWA and SWB. The converter operates in buck mode. In this condition, SWD remains on and SWC remains off. V_{C-Buck} compares with the current ramp signal normally and generates a PWM output. Therefore, SWA/SWB are pulse-width modulated to produce the required duty cycle and eventually support the output voltage.

Buck-Boost Region (VIN ≈ VOUT)

When VIN is close to VOUT, the converter is unable to provide enough energy to load due to SWA's maximum duty cycle, so the current ramp signal cannot trigger V_{C-Buck} in the first period, and SWA remains on with 100% duty cycle. If SWB is not turned on in the first period, boost begins working in the secondary period (SWC switches in the secondary period) and an offset voltage is added to the current ramp signal to allow it to reach V_{C-Buck}. SWC turns off when the current ramp signal intersects with $V_{C-Boost}$ in the secondary period, and SWD conducts the inductor current when SWC is off. This is called boost operation.

SWA turns off when the current ramp signal intersects with V_{C-Buck} in the secondary period, and SWB turns on to conduct the inductor current after SWA turns off. This is called buck operation.

If SWB turns on in the secondary period, the boost operation (SWC on) is disabled in the following cycle. If SWA continues to conduct with 100% duty in the secondary cycle, the boost operation is also enabled in the following duty cycle. SWA/SWB and SWC/SWD switch during this condition simultaneously. This is called buck-boost mode.

Boost Region (VIN < VOUT)

When the input voltage is significantly lower than the output voltage, the control voltage (V_{C-Buck}) is always higher than the current ramp signal. The offset voltage is added to the current signal, so SWB cannot turn on in all cycles. The boost operation (SWC on) is enabled in every cycle based on the logic, so only SWC and SWD switch. This is called boost mode. In this condition, SWC/SWD are pulse-width modulated to produce the required duty cycle and eventually support the output regulation voltage.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is used to protect the device from operating at an insufficient supply voltage. The MP28164's UVLO circuit monitors the VCC voltage. During start-up, VIN must rise higher than $V_{IN-UVLO-R}$ to support enough VCC voltage and enable the IC. After the IC is enabled, VCC is powered by VIN or VOUT (depending on which is higher), so the IC can work, even if VIN drops to 1.2V, unless VCC drops to the $V_{CC-UVLO-F}$ threshold.

During start-up, if VCC has a bias voltage from another power supply, the MP28164 can work with 1.2V of input power. If VIN is much lower than 1.2V, SWA $R_{DS(ON)}$ is high, and the MP28164 cannot supply high power to the output. If VIN drops to 0.69V, the MP28164 stops working.

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VCC Power Supply

When EN is high and VIN ramps up, VIN charges VCC. If VIN is higher than $V_{IN-UVLO-R}$, the MP28164 begins working. All internal circuits of the MP28164 are supplied by VCC, and VCC only needs to be decoupled with a ceramic capacitor less than 1μF. After the system starts up, VCC is powered by the higher value of VIN or VOUT internally. If VCC is powered by VOUT, the MP28164 does not shut down until VIN drops to the UVLO falling threshold (0.69V) or VCC drops to the VCC UVLO falling threshold (1.56V). It is not suggested to supply the MP28164 with an input lower than 1.2V, even if VCC has a bias voltage due to SWA (P-FET) having an $R_{DS(ON)}$ that is too high when VIN is low. Even with 1.2V of input power, the load capability is weaker than the high input condition due to the $R_{DS(ON)}$.

Internal Soft Start (SS)

When EN is high and VIN is above the UVLO rising threshold, the MP28164 starts up with a soft-start function. The internal soft-start (SS) signal ramps up and controls the feedback reference voltage. After 4ms of blank time, if VOUT has not risen to 60% of the normal output voltage, or if VOUT is pulled down to 60% of the normal output voltage due to an overload, the soft-start signal is pulled down to GND and hiccup protection is initiated. During start-up or hiccup recovery condition, an internal SS signal is clamped to V_{FB} + 0.3V if VOUT does not rise up. This limit can prevent a VOUT overshoot if the heavy load disappears suddenly during start-up.

During start-up or recovery from hiccup, if there is already some voltage on the output, this voltage is discharged by the negative current limit (-1A when the MP28164 operates in PWM mode regardless of the MODE/SYNC setting) to equal the SS voltage. VOUT then rises normally.

MODE/SYNC Setting

The MP28164 can be set in PSM or fixed-frequency PWM mode in light load through the MODE/SYNC setting. When MODE/SYNC is pulled high, the MP28164 operates in fixed-frequency PWM mode. The current conducts while the inductor current direction reverses. In this mode, the VOUT ripple is lower than in power-save mode (PSM), but the power loss is higher due to the high-frequency switching.

When MODE/SYNC is pulled low, the MP28164 enters PSM automatically when the load decreases. In PSM, a group of switching pulses are initiated when the internal V_{C-Buck} rises higher than the PSM threshold (group pulses start with SWA/SWC on and end with SWB/SWD on). SWD is turned off if the SWD current flows from VOUT to SW2 in each period.

During start-up or short-circuit protection (SCP) recovery condition, the MP28164 works in fixed-frequency PWM mode, even if MODE/SYNC is low. The negative inductor current is limited to -1A, the same as in constant frequency mode.

OCP/SCP and Two Current Limits

There are two peak-current limits in the MP28164. One is a steady-state switching current limit with a 4.2A typical value. Another one is a start-up switching current limit with a 2.5A typical value. The start-up current limit can control the input inrush current at a lower level when V_{FB} < 60% x V_{REF} during start-up.

In overload or short-circuit condition, VOUT drops due to the steady-state switching current limit. If VOUT drops below 60% of its normal output, the MP28164 stops switching and recovers after ~8ms with hiccup mode protection. After the switching stops in hiccup protection, the internal soft-start signal is clamped to V_{FB} + 0.3V, where V_{FB} is the divided voltage from the residual VOUT. This smooths the soft start-up when the MP28164 recovers from hiccup protection.

During the soft-start time, the MP28164 blanks during hiccup protection for about 4ms. After the 4ms blank time, if VOUT is still lower than 60% of the normal voltage, the MP28164 resumes hiccup mode. If VOUT rises above 60% of the normal value, the MP28164 enters normal operation.

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Power Good (PG)

The MP28164 has a power-good (PG) output. PG is the open drain of the MOSFET. Pull PG up to VCC through a resistor (typically 100kΩ) during application. After the FB voltage reaches 91.5% of the V_{REF} voltage, PG is pulled high. When the FB voltage drops to 76% of the V_{REF} voltage, PG is pulled low.

PG has self-driving capability. If the MP28164 is off and PG is pulled up to another DC power source through a resistor, PG can also be pulled low (~0.7V) by the self-driving circuit.

Over-Voltage Protection (OVP)

If VOUT is higher than the typical 6.3V value, the switching stops. This helps protect the device from high-voltage stress. After the output drops below 5.3V, the switching recovers automatically.

Over-Temperature Protection (OTP)

An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds 160°C, the device stops operating. Once the temperature falls below 140°C, normal operation resumes.

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APPLICATION INFORMATION

Setting the Output Voltage

A resistor divider from VOUT to FB is necessary to set the MP28164's output voltage. The high-side feedback resistor (R1) can be calculated with Equation (1):

$$R1 = (\frac{V_{OUT}}{V_{FB}} - 1) \times R2 \quad (1)$$

Where R2 is the low-side feedback resistor with a recommended value from 60kΩ through 360kΩ to balance the stability and transient response.

Inductor Selection

With one buck-boost topology circuit, the inductor must support the buck application with the maximum input voltage and boost application with the minimum input voltage. Two critical inductance values can be determined according to the buck mode and boost mode current ripple, as shown in Equation (2) and Equation (3):

$$L_{MIN-BUCK} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times F_{REQ} \times \Delta I_L} \quad (2)$$

$$L_{MIN-BOOST} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times F_{REQ} \times \Delta I_L} \quad (3)$$

Where F_{REQ} is the switching frequency, and ΔI_L is the peak-to-peak inductor current ripple. The peak-to-peak ripple can be set to 10%-30% of the inductor current. The minimum inductor value for the application must be higher than the calculated value from both Equation 2 and Equation 3.

In addition to the inductance value, the inductor must support the peak current based on Equation (4) and Equation (5) to avoid saturation:

$$I_{PEAK-BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times F_{REQ} \times L} \quad (4)$$

$$I_{PEAK-BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times V_{OUT} \times F_{REQ} \times L} \quad (5)$$

Where η is the estimated efficiency.

Input and Output Capacitor Selection

It is recommended to use ceramic capacitors with a low ESR as input and output capacitors to filter any disturbance present in the input and output line and to achieve stable operation.

Output capacitors with a minimum 10μF input and 22μF output are required to achieve optimal behavior from the device. The output capacitor affects loop stability. The input and output capacitors must be placed as close as possible to the device. Refer to the Typical Application Circuits section for optimized capacitor selection details.

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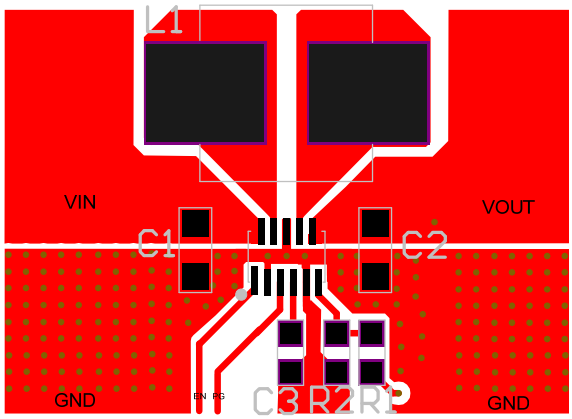
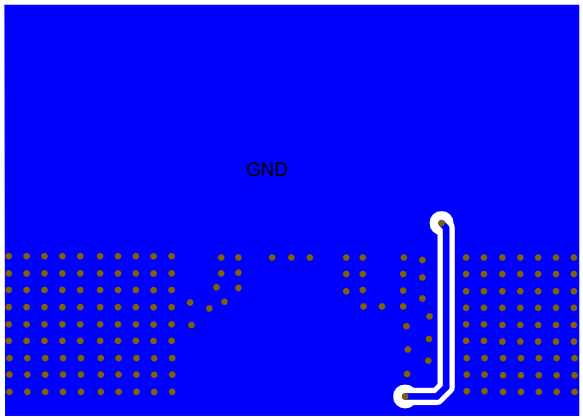
PCB Layout Guidelines

Efficient PCB layout of the high-frequency switching power supplies is critical for stable operation. Poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the input capacitor and output capacitor close to VIN, VOUT, and PGND.
2. Place the VCC decoupling capacitor close to VCC and AGND.
3. Keep the FB resistor divider very close to FB.
4. Keep the FB trace far away from noise sources, such as SW1 and SW2.
5. Ensure the layout of the copper of GND, VIN, and VOUT is wide enough to conduct high current and lower the die temperature.
6. Place vias in the GND copper around the chip for better thermal performance.



Top Layer



Bottom Layer

Figure 3: PCB Layout Recommendation

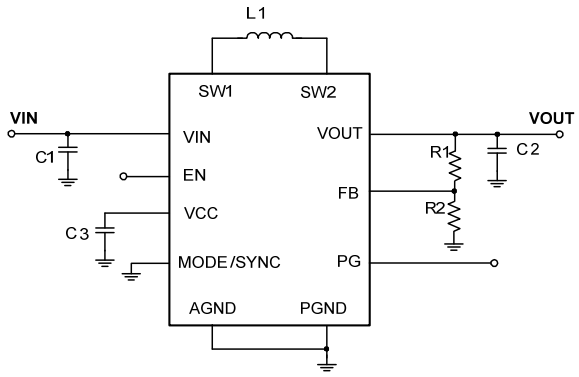


Figure 4: Reference Circuit for PCB Guide

Design Example

Table 1 is a design example following the application guidelines for the specifications below:

Table 1: Design Example

Start-Up V_{IN} (V)	1.8 - 5.5
Operation V_{IN} (V)	1.2 - 5.5
V_{OUT} (V)	3.3V

The detailed application schematic is shown in Figure 5, and the performance can be found in the Typical Performance Characteristics sections.

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TYPICAL APPLICATION CIRCUITS

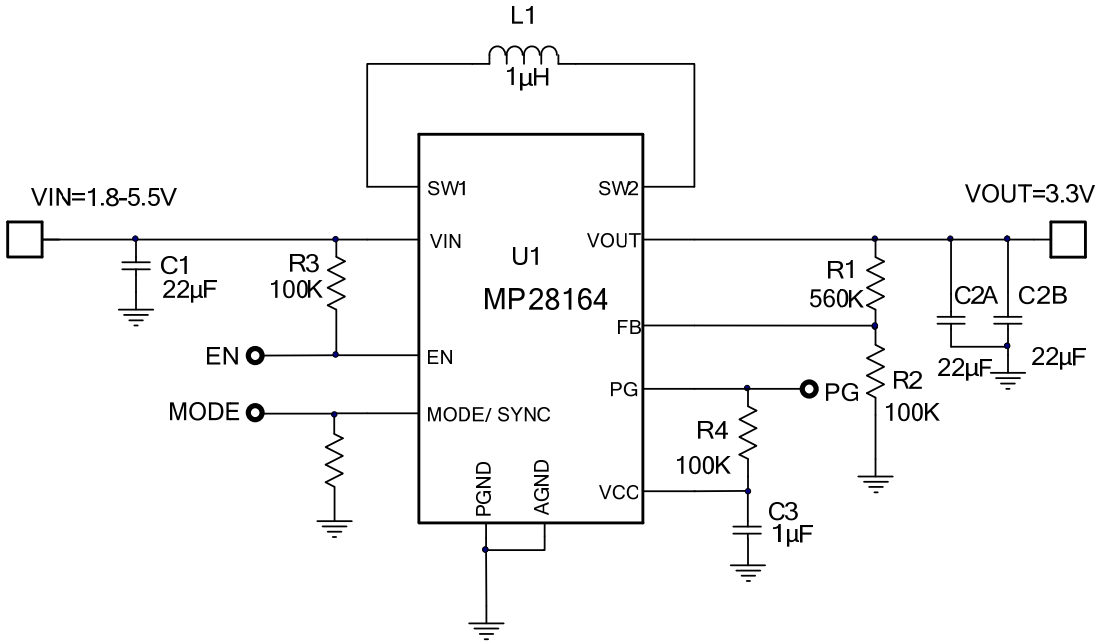

Figure 5: 3.3V Output Application Circuit

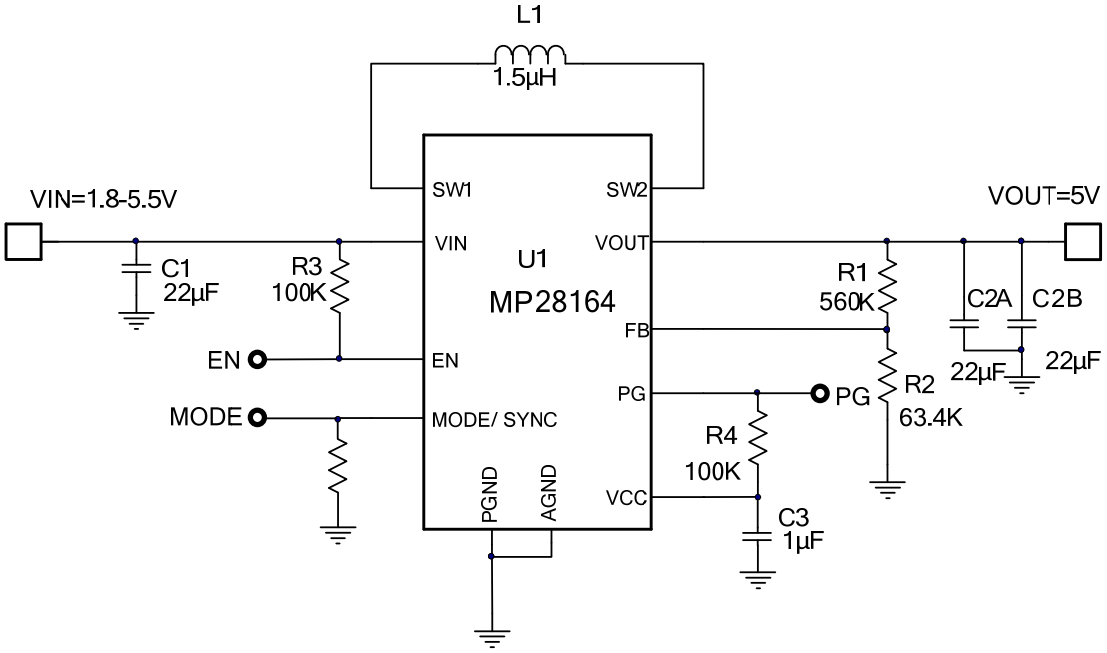

Figure 6: 5V Output Application Circuit

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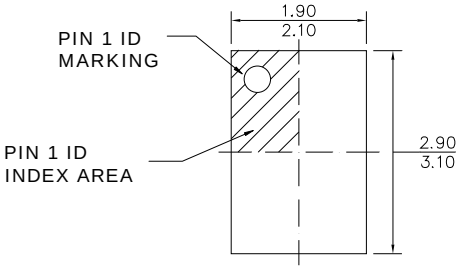
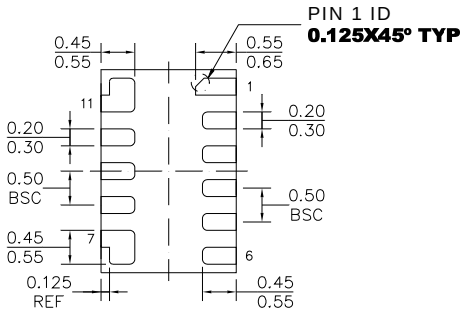
PACKAGE INFORMATION

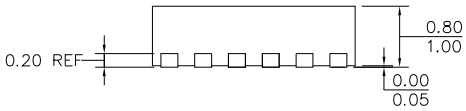
QFN-11 (2mmx3mm)



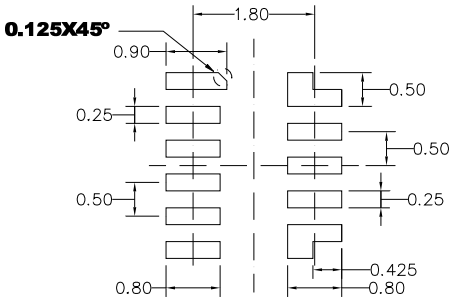
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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