DSC1103/23

Low-Jitter Precision LVDS Oscillator

Features

- Low RMS Phase Jitter: <1 ps (typ.)
- High Stability: ±10 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range:
  - Ext. Industrial –40°C to +105°C
  - Industrial –40°C to +85°C
  - Ext. Commercial –20°C to +70°C
- High Supply Noise Rejection: –50 dBc
- Wide Frequency Range:
  - 2.3 MHz – 460 MHz
- Small Industry Standard Footprints
  - 2.5 mm x 2.0 mm
  - 3.2 mm x 2.5 mm
  - 5.0 mm x 3.2 mm
  - 7.0 mm x 5.0 mm
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x better MTF than quartz-based devices
- Low Current Consumption
- Supply Range of 2.25V to 3.63V
- Standby and Output Enable Functions
- Lead Free and RoHS-Compliant

Applications

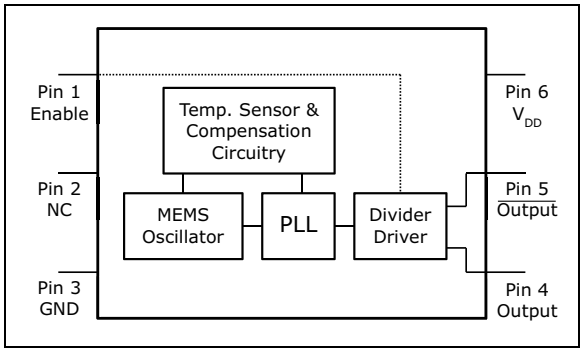
- Storage Area Networks
  - SATA, SAS, Fibre Channel
- Passive Optical Networks
  - EPON, 10G-EPON, GPON, 10G-PON
- HD/SD/SDI Video and Surveillance
- PCI Express Gen 1/Gen 2/Gen 3
- Display Port

General Description

The DSC1103 and DSC1123 series of high performance oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC1103 has a standby feature allowing it to completely power-down when EN pin is pulled low. For DSC1123, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the smallest 2.5 mm x 2.0 mm, and are drop-in replacements for standard 6-pin LVDS crystal oscillators.

Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... –0.3V to +4.0V
Input Voltage ..... –0.3V to V_{DD}+0.3V
ESD Protection (HBM) ..... 4 kV
ESD Protection (MM) 400V
ESD Protection (CDM) ..... 1.5 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Specifications: V_{DD} = 3.3V; T_A = +25°C unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	2.25	—	3.63	V	—
Supply Current	I_{DD}	—	—	0.095	mA	DSC1103, EN pin low; all outputs disabled.
		—	20	22		DSC1123, EN pin low; all outputs disabled.
Frequency Stability	Δf	—	—	±10	ppm	Includes frequency variations due to initial tolerance, temp., and power supply voltage.
		—	—	±25		
		—	—	±50		
Aging - First Year	Δf_{Y1}	—	—	±5	ppm	One year at +25°C
Aging - After First Year	Δf_{Y2+}	—	—	<±1	ppm/yr	Year two and beyond at +25°C
Start-up Time (Note 2)	t_{SU}	—	—	5	ms	T = +25°C
Input Logic Levels	V_{IH}	0.75 x V_{DD}	—	—	V	Input logic high
	V_{IL}	—	—	0.25 x V_{DD}		Input logic low
Output Disable Time (Note 3)	t_{DA}	—	—	5	ns	—
Output Enable Time	t_{EN}	—	—	5	ms	DSC1103
		—	—	20	ns	DSC1123
Enable Pull-Up Resistor (Note 4)	R_{PU}	—	40	—	kΩ	Pull-up resistor exist.
LVDS Outputs						
Supply Current	I_{DD}	—	29	32	mA	Output enabled, R_L = 100Ω
Output Offset Voltage	V_{OS}	1.125	—	1.4	V	R = 100Ω Differential
Delta Offset Voltage	ΔV_{OS}	—	—	50	mV	—
Peak-to-Peak Output Swing	V_{PP}	—	350	—	mV	Single-Ended

Note 1: V_{DD} pin should be filtered with a 0.1 µF capacitor.
2: t_{SU} is time to 100 ppm stable output frequency after V_{DD} is applied and outputs are enabled.
3: See the Output Waveform section and the Test Circuit for more information.
4: Output is enabled if pad is floated or not connected.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Specifications: V_{DD} = 3.3V; T_A = +25°C unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Transition Rise/Fall Time (Note 3)	t_R/t_F	—	200	—	ps	20% to 80% R_L = 50Ω, C_L = 2 pF
Frequency	f_0	2.3	—	460	MHz	–20°C to +70°C & –40°C to +85°C
		3.3	—	460		–40°C to +105°C
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter	J_{PER}	—	2.5	—	ps_{RMS}	—
Integrated Phase Noise	J_{PH}	—	0.28	—	ps_{RMS}	200 kHz to 20 MHz @156.25 MHz
		—	0.4	—		100 kHz to 20 MHz @156.25 MHz
		—	1.7	2		12 kHz to 20 MHz @156.25 MHz

Note 1: V_{DD} pin should be filtered with a 0.1 µF capacitor.

2: t_{SU} is time to 100 ppm stable output frequency after V_{DD} is applied and outputs are enabled.

3: See the Output Waveform section and the Test Circuit for more information.

4: Output is enabled if pad is floated or not connected.

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	–20	—	+70	°C	Ordering Option E
	T_A	–40	—	+85	°C	Ordering Option I
	T_A	–40	—	+105	°C	Ordering Option L
Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–55	—	+150	°C	—
Soldering Temperature	—	—	—	+260	°C	40 sec. max.

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature, and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number 7x5 with Pad	Pin Number 7x5 w/o Pad	Pin Number 5x3.2	Pin Number 3.2x2.5	Pin Number 2x2.5	Pin Name	Description
1	1	1	1	1	EN	Enable
2	2	2	2	2	NC	Do not connect
3	3	3	3	3	GND	Ground
4	4	4	4	4	OUT	LVDS clock output +
5	5	5	5	5	OUT–	LVDS clock output –
6	6	6	6	6	VDD	Supply voltage
PAD	—	—	—	—	PAD	Tie to Ground

TABLE 2-2: OUTPUT ENABLE MODES

EN Pin	DSC1103	DSC1123
High	Outputs Active	Outputs Active
NC	Outputs Active	Outputs Active
Low	Standby	Outputs Disabled

3.0 NOMINAL PERFORMANCE PARAMETERS

Unless otherwise specified, T = +25°C, V_{DD} = 3.3V.

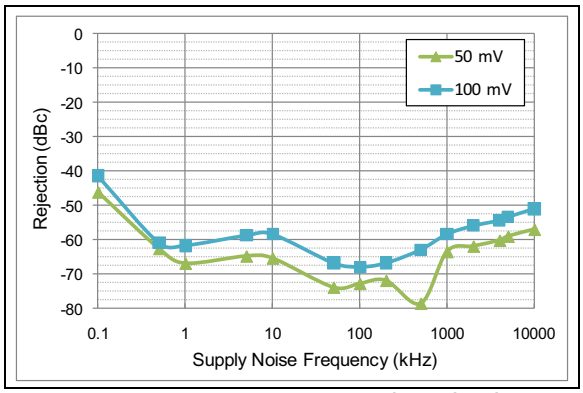


FIGURE 3-1: *Power Supply Rejection Ratio.*

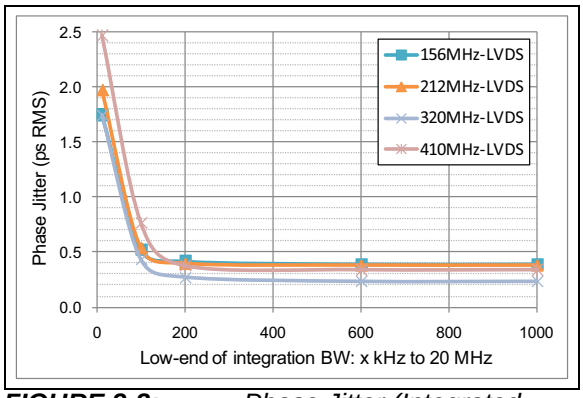


FIGURE 3-2: *Phase Jitter (Integrated Phase Noise).*

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4.0 TERMINATION SCHEME

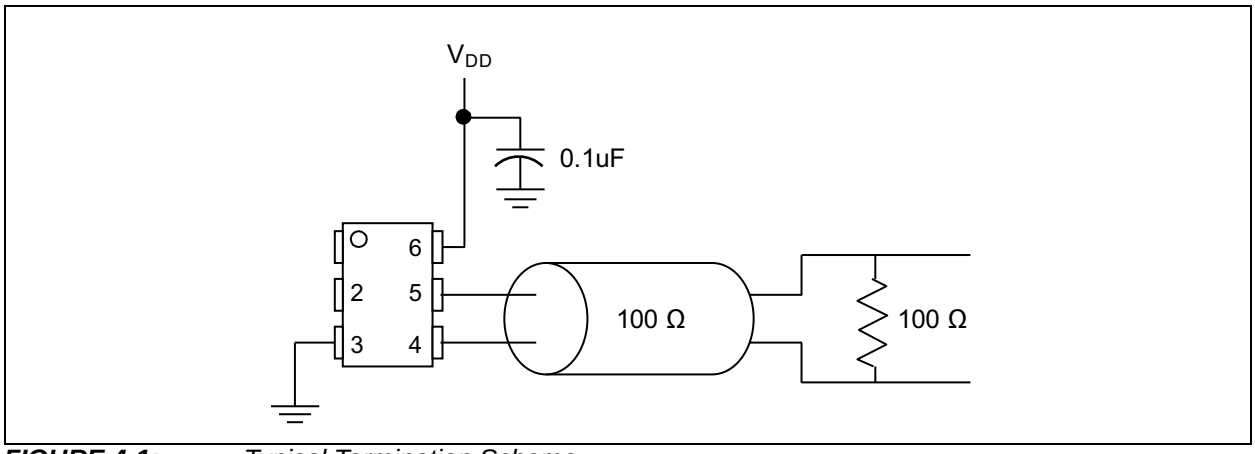


FIGURE 4-1: *Typical Termination Scheme.*

5.0 OUTPUT WAVEFORM

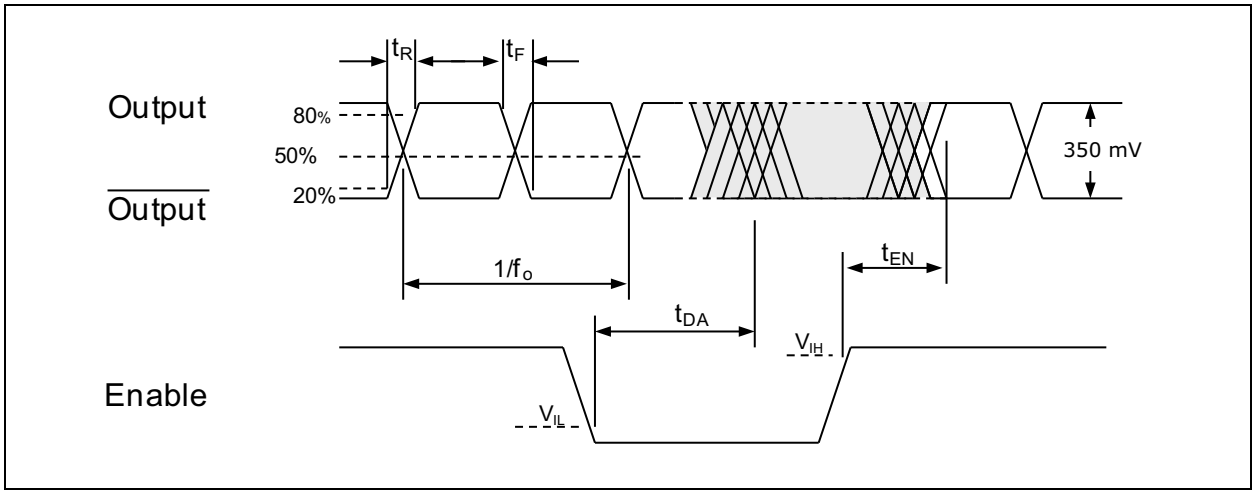


FIGURE 5-1: *Output Waveform.*

6.0 TEST CIRCUIT

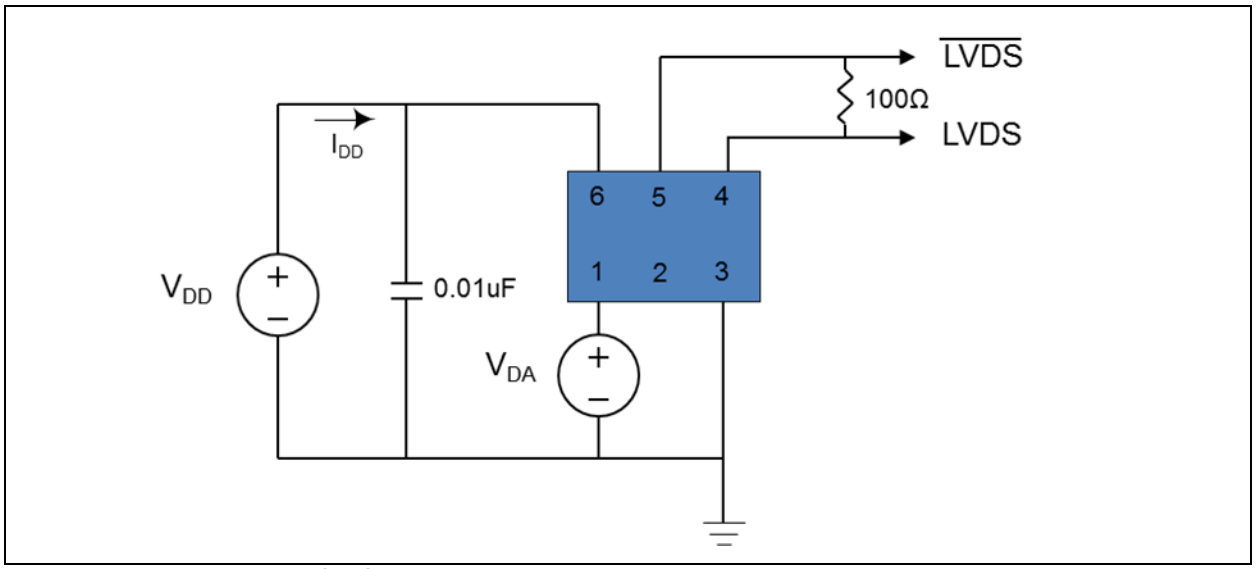
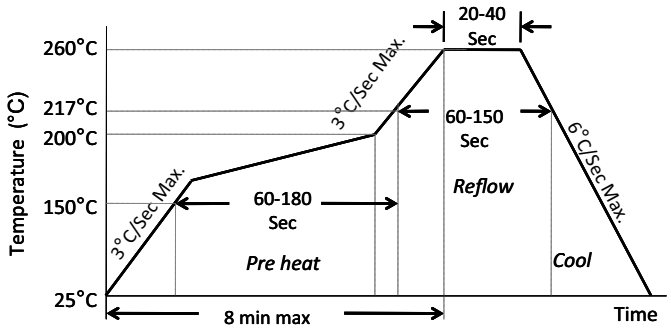


FIGURE 6-1: *Test Circuit.*

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7.0 SOLDER REFLOW PROFILE



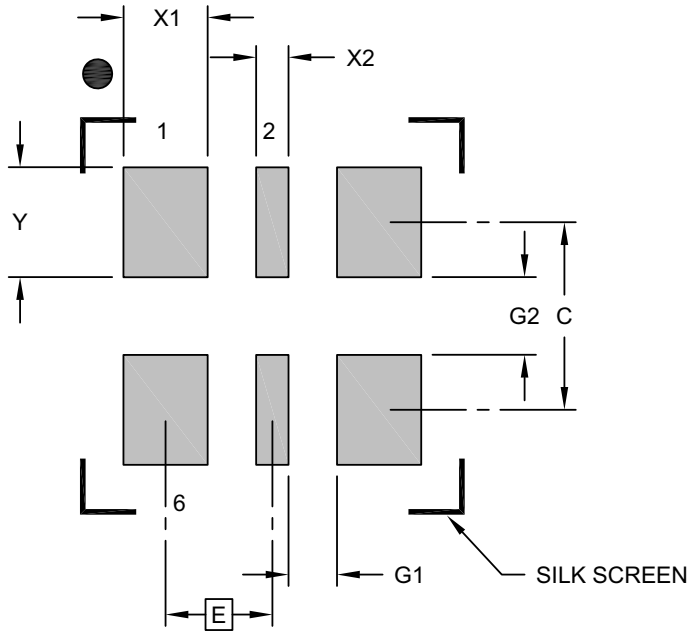
MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec. max.
Preheat Time 150°C to 200°C	60-180 sec.
Time Maintained above 217°C	60-150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20-40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

8.0 PACKAGE MARKING INFORMATION

6-Lead VDFN 2.5 mm x 2.0 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.825 BSC		
Contact Pad Width (X4)	X1			0.65
Contact Pad Width (X2)	X2			0.25
Contact Pad Length (X6)	Y			0.85
Contact Pad Spacing	C		1.45	
Space Between Contacts (X4)	G1	0.38		
Space Between Contacts (X3)	G2	0.60		

Notes:

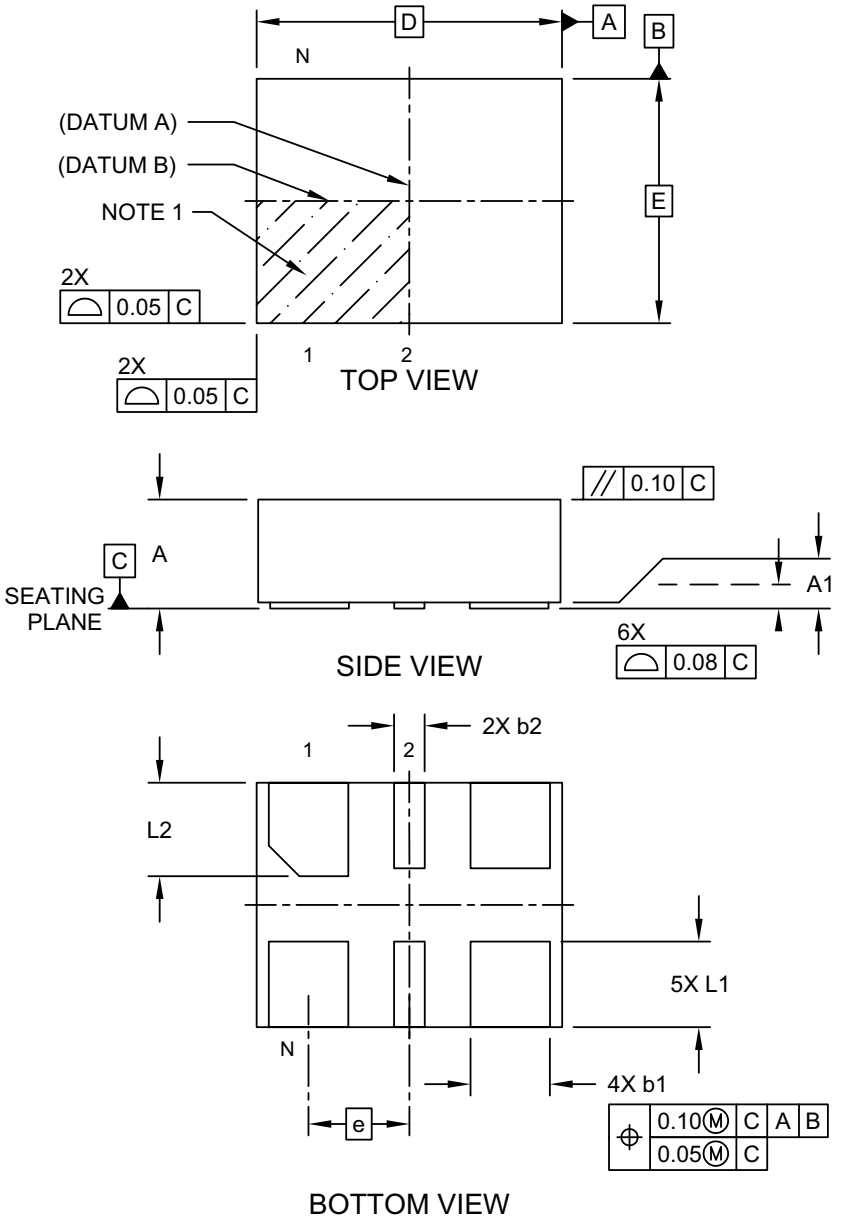
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

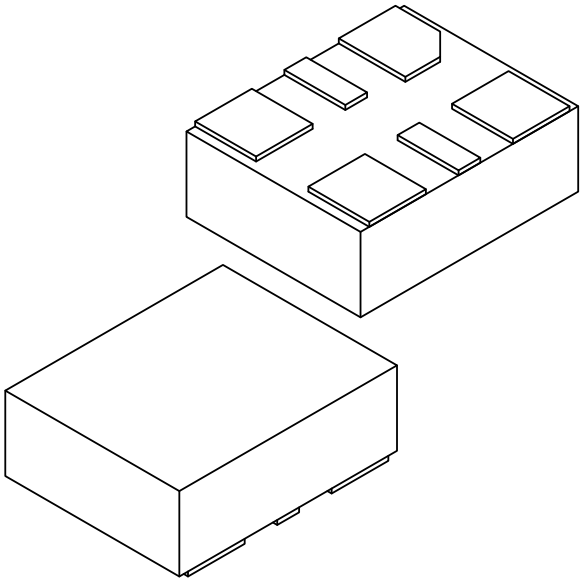
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.825 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		2.50 BSC	
Overall Width	E		2.00 BSC	
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.20	0.25	0.30
Terminal Length	L1	0.60	0.70	0.80
Terminal Length	L2	0.665	0.765	0.865

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

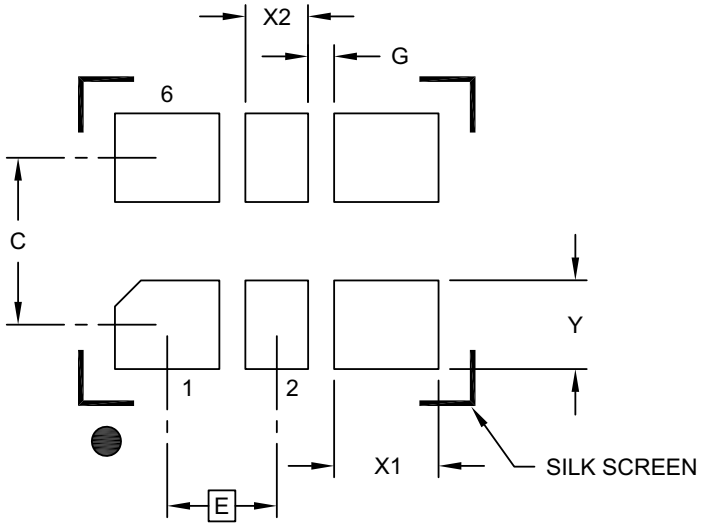
Microchip Technology Drawing C04-1005A Sheet 2 of 2

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6-Lead VDFN 3.2 mm x 2.5 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.05 BSC	
Contact Pad Spacing	C		1.60	
Contact Pad Width (X4)	X1			1.00
Contact Pad Width (X2)	X2			0.60
Contact Pad Length (X6)	Y			0.85
Space Between Contacts (X4)	G1	0.25		

Notes:

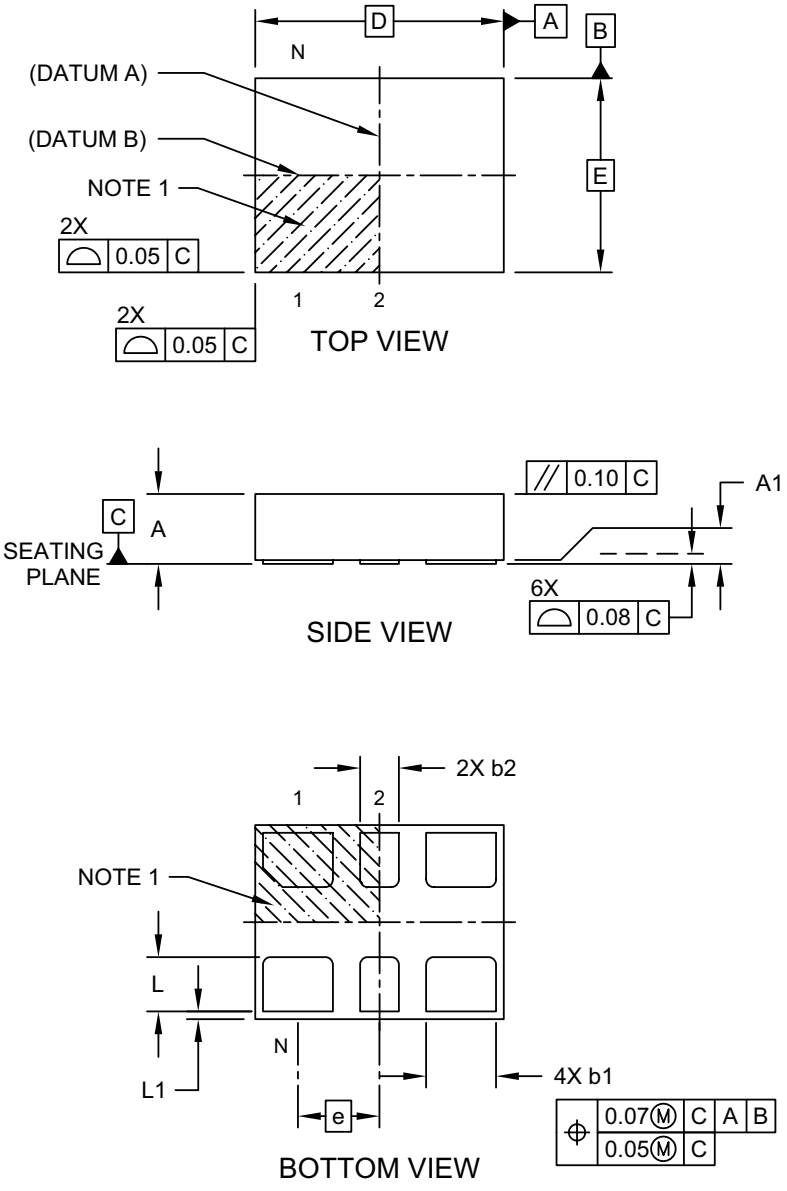
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3007A

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

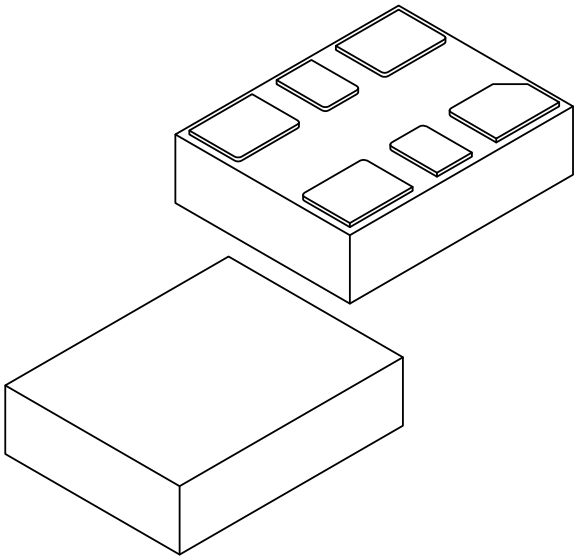


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6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		1.05 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		3.20 BSC	
Overall Width	E		2.50 BSC	
Terminal Width	b1	0.85	0.90	0.95
Terminal Width	b2	0.45	0.50	0.55
Terminal Length	L	0.65	0.70	0.75
Terminal Pullback	L1		0.10 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

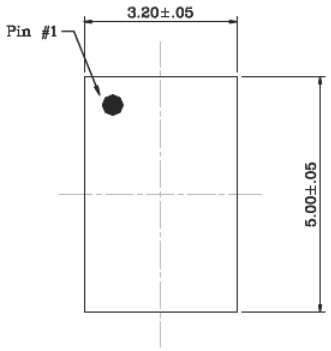
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1007A Sheet 2 of 2

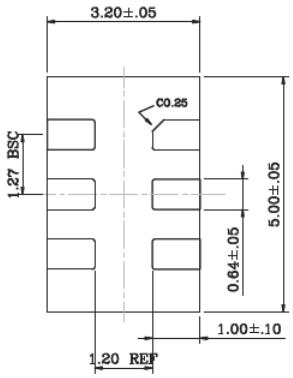
6-Lead CDFN 5.0 mm x 3.2 mm Package Outline and Recommended Land Pattern

TITLE
6 LEAD CDFN 5.0x3.2mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

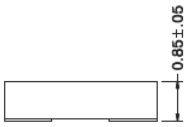
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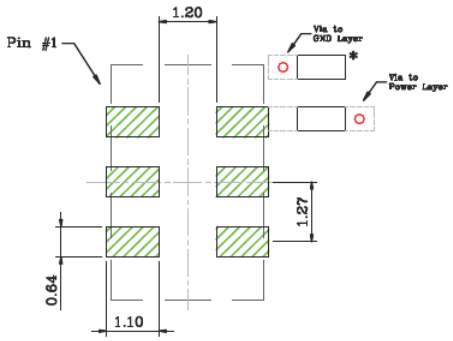
Top View



Bottom View



Side View



Recommended Land Pattern

NOTE:

1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

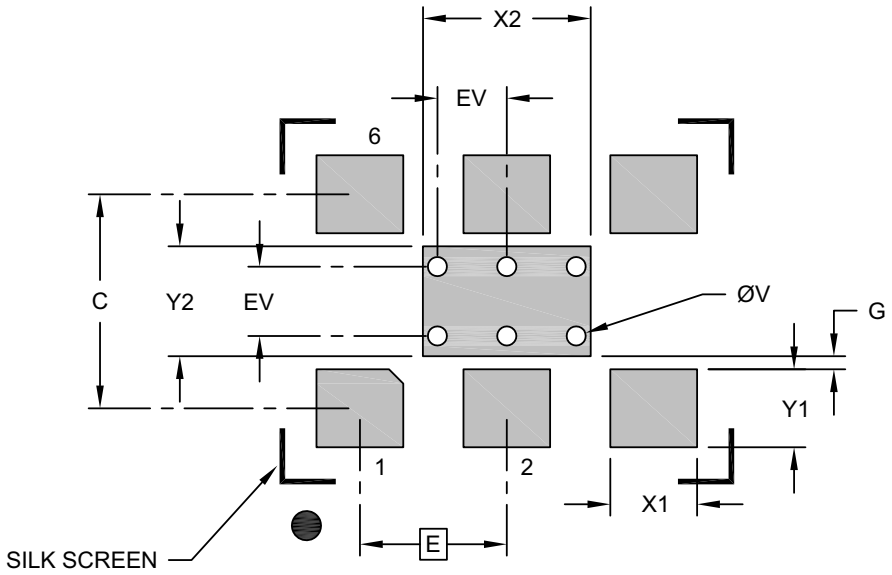
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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6-Lead VDFN 7.0 mm x 5.0 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		2.54 BSC	
Optional Center Pad Width	X2			2.90
Optional Center Pad Length	Y2			1.90
Contact Pad Spacing	C		3.70	
Contact Pad Width (X6)	X1			1.50
Contact Pad Length (X6)	Y1			1.35
Contact Pad to Center Pad (X2)	G	0.20		
Thermal Via Diameter (X6)	V		0.33	
Thermal Via Pitch	EV		1.20	

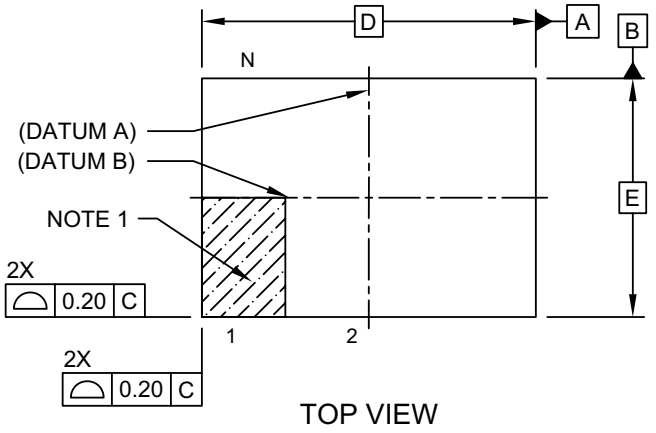
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

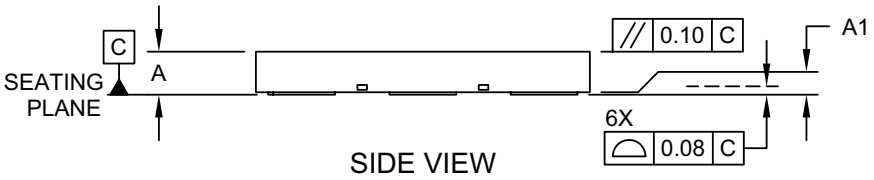
Microchip Technology Drawing C04-3010A

6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

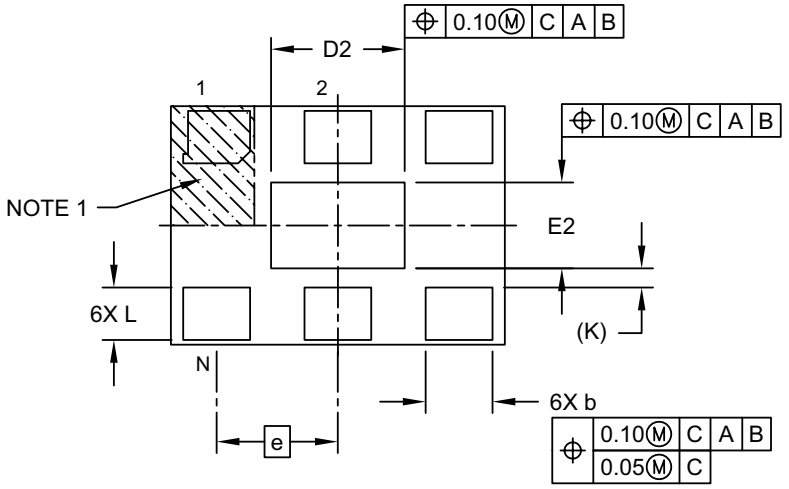
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



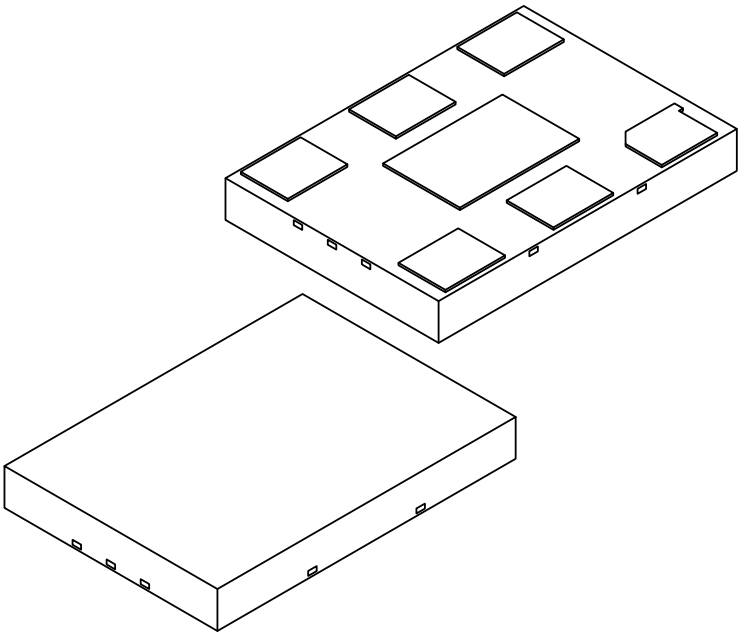
BOTTOM VIEW

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6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		2.54	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	2.70	2.80	2.90
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	1.70	1.80	1.90
Terminal Width	b	1.35	1.40	1.45
Terminal Length	L	1.00	1.10	1.20
Terminal-to-Exposed-Pad	K		0.20 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

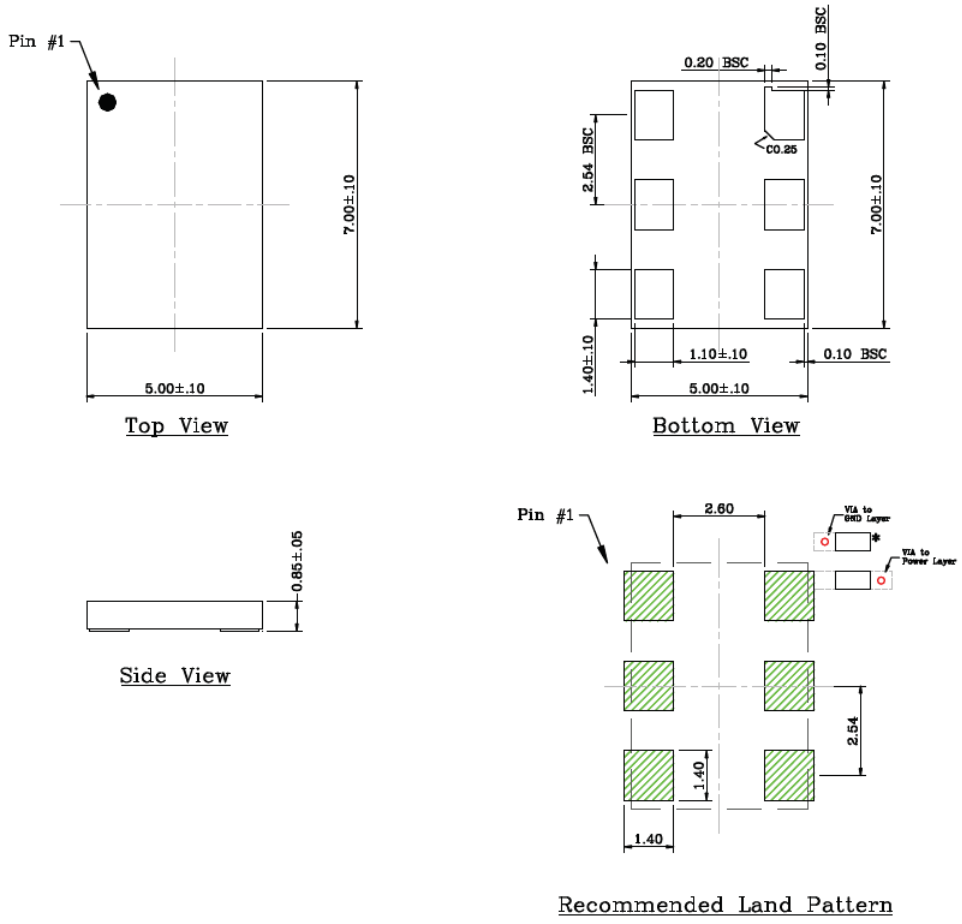
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1010A Sheet 2 of 2

6-Lead CDFN 7.0 mm x 5.0 mm Package Outline and Recommended Land Pattern

TITLE
6 LEAD CDFN 7.0x5.0mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	CDFN75-6LD-PL-1	UNIT	MM



NOTE:

1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision A (March 2017)

- Converted Micrel data sheet DSC1103/23 to Microchip DS20005745A.
- Minor text changes throughout.
- Updated Package Marking Information to MCHP-standard drawings where available.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	3	X	X	X	—	xxx.xxxx	X
Device (First 2 Digits)	Enable Modes	Device (Last Digit)	Package	Temp. Range	Stability		Frequency	Packing

Device:	DSC11x3:		Low-Jitter Precision LVDS Oscillator
Enable Modes:	0	=	Enable/Standby
	2	=	Enable/Disable
Package:	A	=	7.0 mm x 5.0 mm VDFN
	B	=	5.0 mm x 3.2 mm CDFN
	C	=	3.2 mm x 2.5 mm VDFN
	D	=	2.5 mm x 2.0 mm VDFN
	N	=	7.0 mm x 5.0 mm CDFN (no center pad)
Temperature Range:	E	=	–20°C to +70°C
	I	=	–40°C to +85°C
	L	=	–40°C to +105°C
Stability:	1	=	±50 ppm
	2	=	±25 ppm
	5	=	±10 ppm
Frequency Code:	xxx.xxxx	=	2.3 MHz to 460 MHz (user-defined)
Packing:	T	=	1,000/Reel
	(blank)	=	100/Tube

Examples:

a) DSC1103AE1-125.0000: Low-Jitter Precision LVDS Oscillator, Enable/Standby, 7x5 VDFN, –20°C to +70°C, ±50 ppm, 125 MHz, 100/Tube

b) DSC1123BI2-400.0000T: Low-Jitter Precision LVDS Oscillator, Enable/Disable, 5x3.2 CDFN, –40°C to +85°C, ±25 ppm, 400 MHz, 1,000/Reel

c) DSC1103CL5-074.2500: Low-Jitter Precision LVDS Oscillator, Enable/Standby, 3.2x2.5 VDFN, –40°C to +105°C, ±10 ppm, 74.25 MHz, 100/Tube

d) DSC1123DE1-082.5000T: Low-Jitter Precision LVDS Oscillator, Enable/Disable, 2.5x2.0 VDFN, –20°C to +70°C, ±50 ppm, 82.5 MHz, 1,000/Reel

e) DSC1103NI2-056.0000: Low-Jitter Precision LVDS Oscillator, Enable/Standby, 7x5 CDFN (no center pad), –40°C to +85°C, ±25 ppm, 56 MHz, 100/Tube

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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