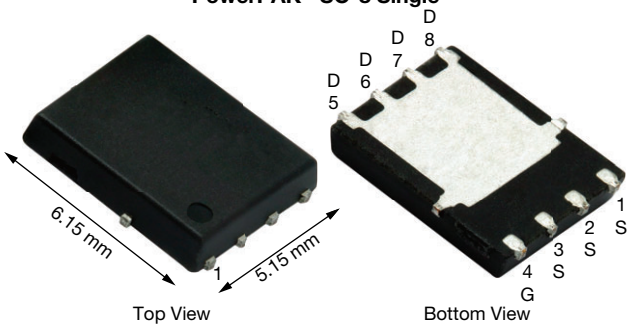
N-Channel 20 V (D-S) Fast Switching MOSFET

PowerPAK® SO-8 Single



FEATURES

- TrenchFET® power MOSFET
- New low thermal resistance PowerPAK® package with low 1.07 mm profile
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

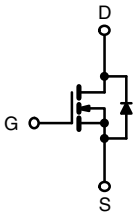
RoHS COMPLIANT

HALOGEN FREE Available

APPLICATIONS

- Synchronous rectifier low output voltage
- Portable computer battery selection or protection

PRODUCT SUMMARY	
V_{DS} (V)	20
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.0065
$R_{DS(on)}$ max. (Ω) at V_{GS} = 2.5 V	0.0090
Q_g typ. (nC)	38
I_D (A)	22
Configuration	Single



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free	Si7448DP-T1-E3
Lead (Pb)-free and halogen-free	Si7448DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	10 s	STEADY STATE	UNIT
Drain-source voltage		V_{DS}	20	20	V
Gate-source voltage		V_{GS}	± 12	± 12	
Continuous drain current (T_J = 150 °C) [a]	T_A = 25 °C	I_D	22	13.4	A
	T_A = 70 °C		17.6	10.7	
Pulsed drain current		I_{DM}	50	50	
Continuous source current (diode conduction) [a]		I_S	4.3	1.6	
Maximum power dissipation [a]	T_A = 25 °C	P_D	5.2	1.9	W
	T_A = 70 °C		3.3	1.2	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [b, c]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a]	t ≤ 10 s	R_{thJA}	19	24	°C/W
	Steady state		52	65	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.5	1.8	

Notes

a. Surface mounted on 1" x 1" FR4 board

b. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

For technical questions, contact: pmostechsupport@vishay.com

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.6	-	1.5	V
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 85°C	-	-	20	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	50	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 22 A	-	0.0054	0.0065	Ω
		V_{GS} = 2.5 V, I_D = 19 A	-	0.0075	0.0090	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 22 A	-	90	-	S
Diode forward voltage [a]	V_{SD}	I_S = 3 A, V_{GS} = 0 V	-	0.8	1.2	V
Dynamic [b]						
Total gate charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 21 A	-	38	50	nC
Gate-source charge	Q_{gs}		-	8	-	
Gate-drain charge	Q_{gd}		-	8.5	-	
Gate resistance	R_g		0.2	0.9	1.1	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 6 Ω	-	22	35	ns
Rise time	t_r		-	22	35	
Turn-off delay time	$t_{d(off)}$		-	125	190	
Fall time	t_f		-	60	90	
Source-drain reverse recovery time	t_{rr}	I_F = 3 A, di/dt = 100 A/µs	-	60	90	

Notes

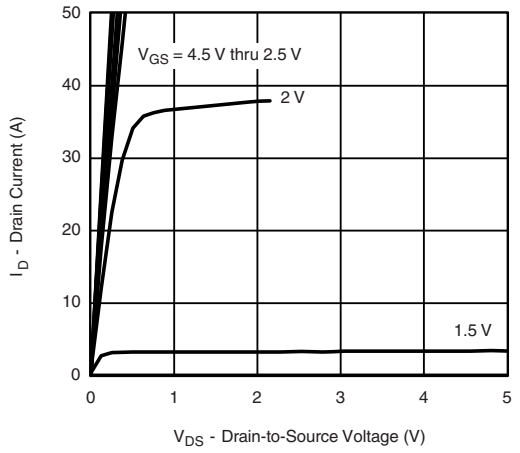
a. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

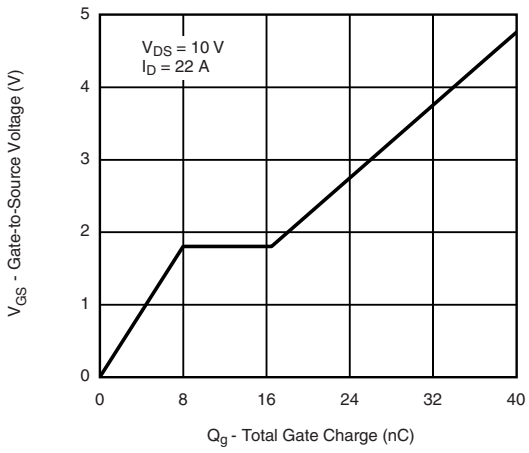
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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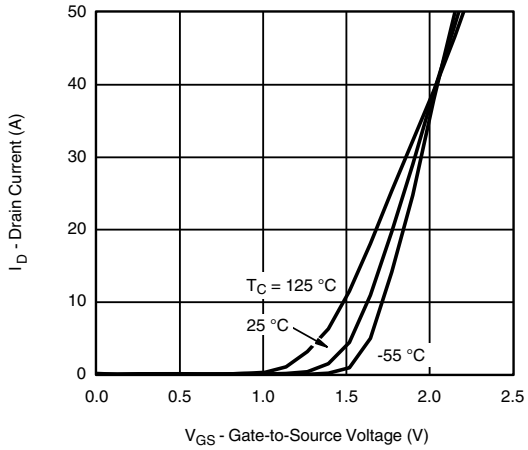
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



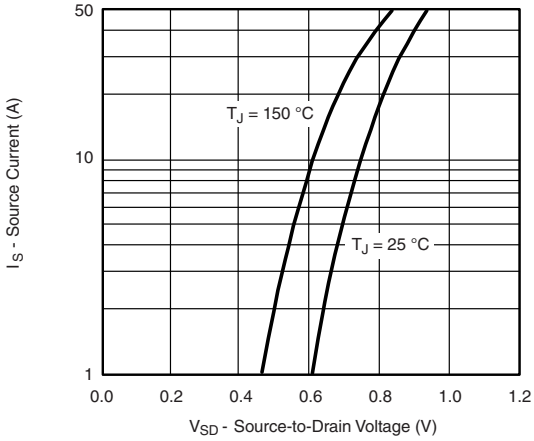
Output Characteristics



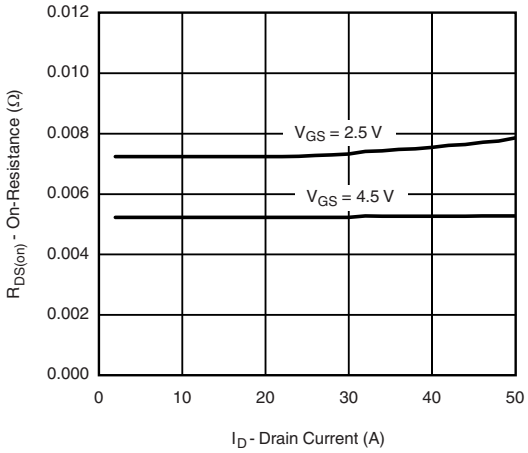
Gate Charge



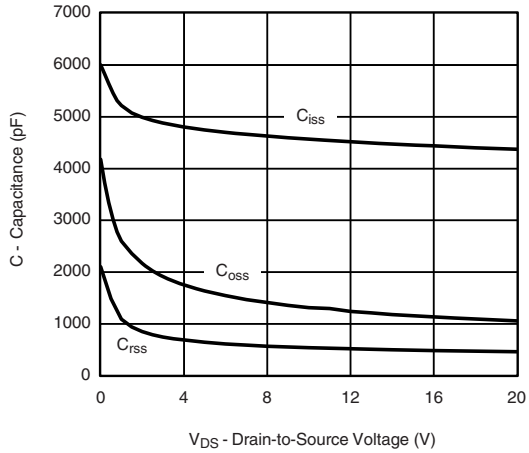
Transfer Characteristics



Source-Drain Diode Forward Voltage



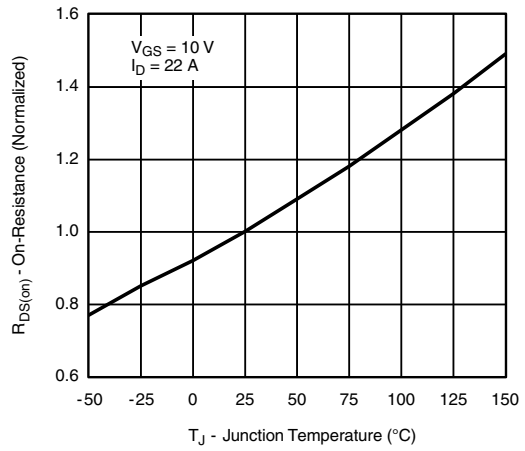
On-Resistance vs. Drain Current



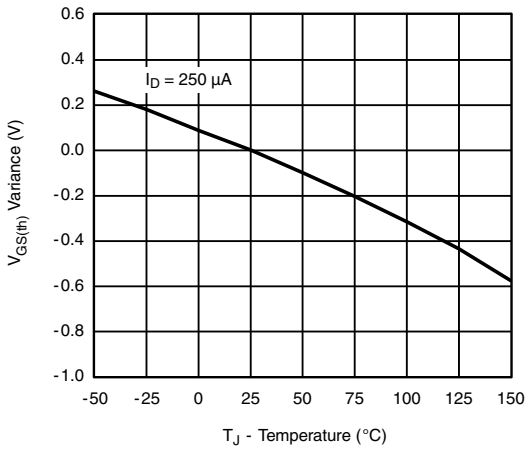
Capacitance

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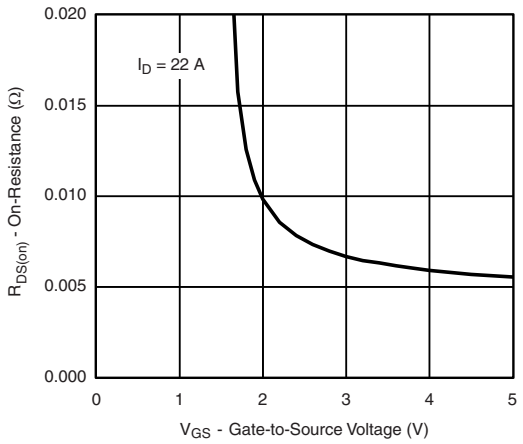
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



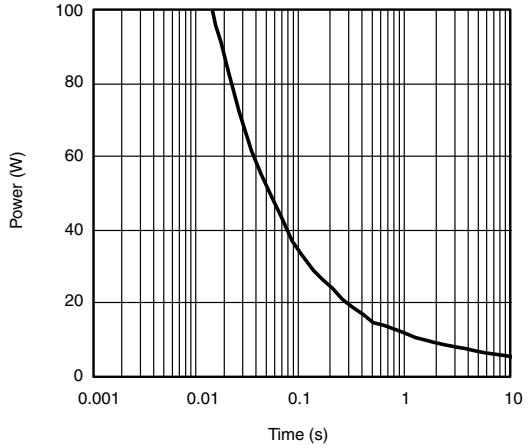
On-Resistance vs. Junction Temperature



Threshold Voltage



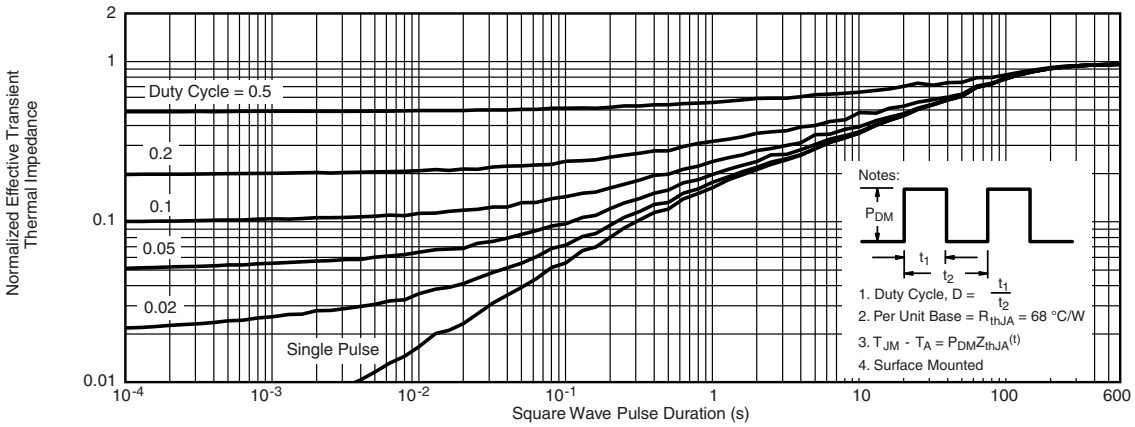
On-Resistance vs. Gate-to-Source Voltage



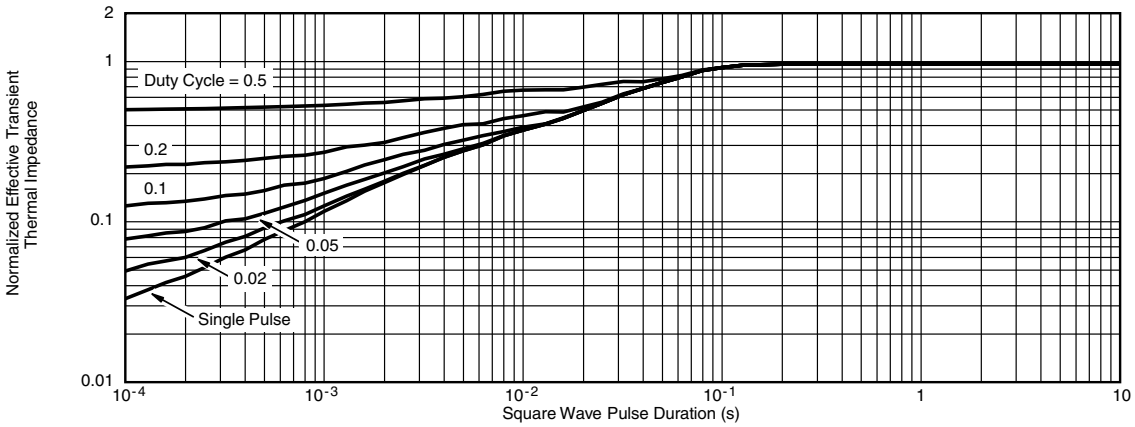
Single Pulse Power, Junction-to-Ambient

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

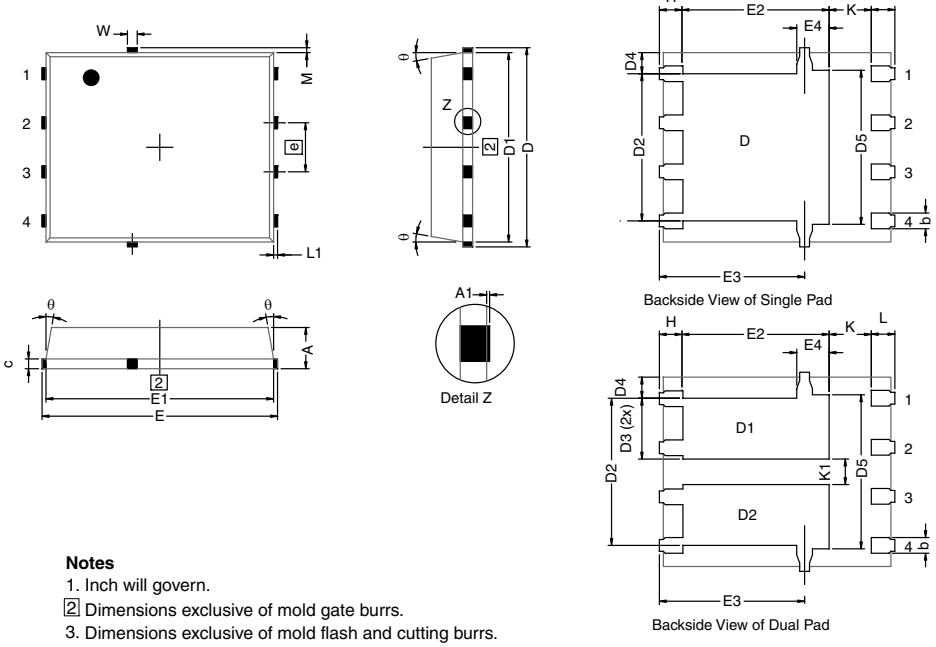


Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK® SO-8, (Single/Dual)



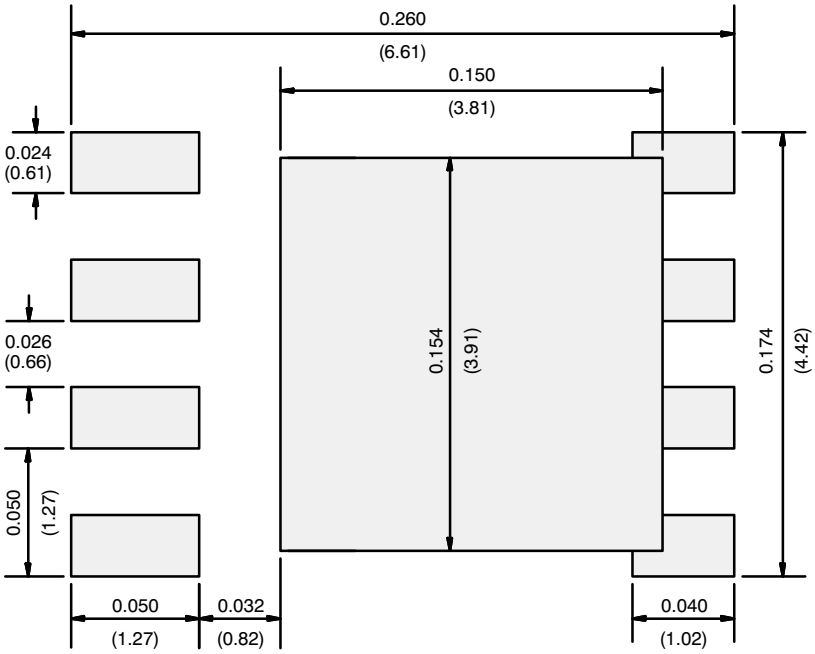
Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S17-0173-Rev. L, 13-Feb-17 DWG: 5881						

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RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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