MP2490

1.5A, 36V, 700KHz Step-Down Converter with Programmable Output Current Limit

The Future of Analog IC Technology

DESCRIPTION

The MP2490 is a monolithic step-down switch mode converter with a programmable output current limit. It achieves 1.5A continuous output current over a wide input supply range with excellent load and line regulation.

The maximum output current can be programmed by sensing current through the inductor DC resistance (DCR) or an accurate sense resistor.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2490 requires a minimum number of readily available standard external components. The MP2490 is available in QFN10 (3mm x 3mm), 8-pin SOIC and PDIP packages.

FEATURES

- Wide 4.5V to 36V Operating Input Range
- Programmable up to 1.5A Output Current
- Output Adjustable from 0.8V to 15V
- Programmable Output Current Limit without power loss
- 0.25Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- 95% Efficiency @ 500mA (Vo=5V)
- Fixed 700kHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Available in QFN10 (3mm x 3mm), 8-Pin SOIC and PDIP Packages

APPLICATIONS

- USB Power Supplies
- Automotive Cigarette Lighter Adapters
- Power Supply for Linear Chargers

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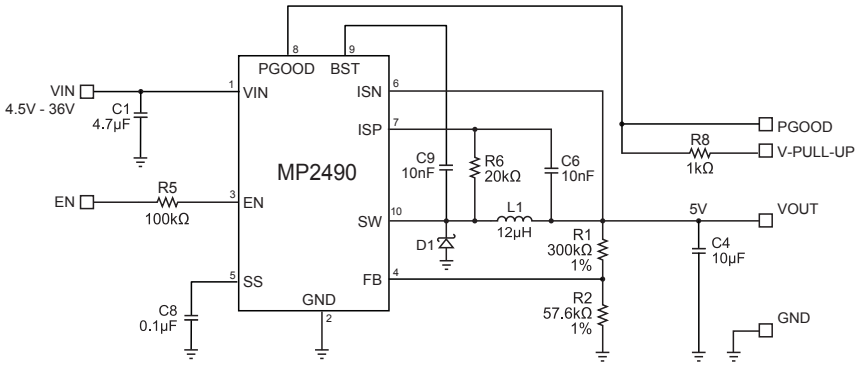
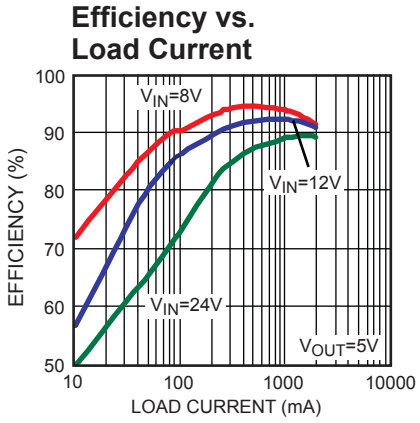
TYPICAL APPLICATION





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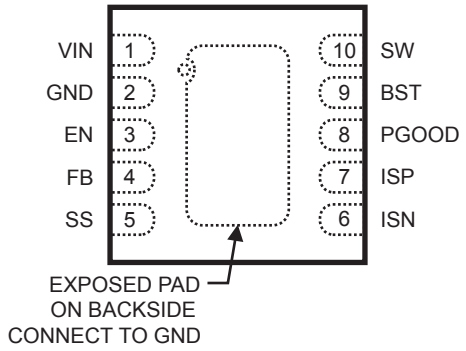
ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP2490DQ *	QFN10 (3mm X 3mm)	T6	–40°C to +85°C
MP2490DS	SOIC8	MP2490DS	–40°C to +85°C
MP2490CP	PDIP8	MP2490CP	0°C to +70°C

* For Tape & Reel, add suffix –Z (e.g. MP2490DQ–Z);
For RoHS, compliant packaging, add suffix –LF (e.g. MP2490DQ–LF–Z).

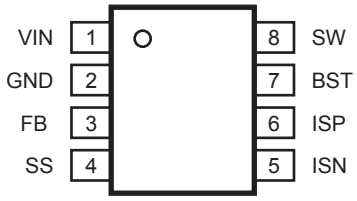
PACKAGE REFERENCE

TOP VIEW



QFN10 (3mm X 3mm)

TOP VIEW



SOIC/PDIP

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 40V
V_{SW} ..... –0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6.5V
V_{ISN}, V_{ISP} 0V to15V
All Other Pins ..... –0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
QFN10 (3mm x 3mm) 2.5W
SOIC8 ..... 1.39W
PDIP8 ..... 1.32W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 36V
Output Voltage V_{OUT} (V_{IN}>16.5V) ..... 0.8V to 15
Output Voltage V_{OUT} (V_{IN}<=16.5V) .....
..... 0.8V to (V_{IN}–1.5)V
Operating Junction Temperature (T_J)
..... –40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN10 (3mm x 3mm)	50	12	°C/W
SOIC8	90	45	°C/W
PDIP8	95	55	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JEDEC51-7 4 layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 36V	0.785	0.805	0.825	V
Feedback Bias Current	$I_{BIAS(FB)}$	V_{FB} = 0.8V		10		nA
Switch On Resistance	$R_{DS(ON)}$			0.25		Ω
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0.1	10	μA
Current Limit (5)			2.2	2.6	3	A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	560	700	840	KHz
Fold-Back Frequency		V_{FB} = 0V		200		KHz
Boot-Strap Voltage	V_{BST} - V_{SW}			5		V
Minimum On Time (5)	t_{ON}	V_{FB} = 1V		100		ns
Under Voltage Lockout Threshold Rising			3.0	3.3	3.6	V
Under Voltage Lockout Threshold Hysteresis				200		mV
EN Input Low Voltage (6)					0.4	V
En Input High Voltage (6)			1.8			V
EN Input Bias Current (6)		V_{EN} = 0-6V	–10	–2	10	μA
Supply Current (Shutdown)		V_{EN} = 0V		4	10	μA
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 1V		500	800	μA
Thermal Shutdown (5)				150		°C
Current Sense Voltage	V_{ISP} –V_{ISN}	V_{ISP}, V_{ISN} 0.4–15V	90	100	110	mV
Input Bias Current (ISN, ISP)	$I_{BIAS\ (ISN,ISP)}$	V_{ISP}, V_{ISN} 0.4–15V	–1	0.1	+1	uA
PGOOD Sink Current		Sink Current 5mA			0.3	V

Note:

5) Guaranteed by design

6) Enable function is only available for the MP2490DQ

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PIN FUNCTIONS

QFN10-3 Pin #	SOIC-8 / PDIP-8 Pin#	Name	Description
1	1	VIN	Supply Voltage. The MP2490 operates from a +4.5V to +36V unregulated input. C_{IN} is needed to prevent large voltage spikes from appearing at the input. Put C_{IN} as close to the IC as possible. It is the drain of the internal power device and power supply for the whole chip.
2	2	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C_{IN} ground path to prevent switching current spikes from inducing voltage noise into the part.
3		EN	On/Off Control Input. (Only available for the MP2490DQ)
4	3	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency-fold-back comparator lowers the oscillator frequency when the FB voltage is below 250mV.
5	4	SS	Connect to an external capacitor used for Soft-Start and compensation for current limiting loop.
6	5	ISN	Negative Current Sense Input for load current limiting.
7	6	ISP	Positive Current Sense
8		PGOOD	Power good signal. When FB is less than 90% of 0.8V, PGOOD is low. It is an open-drain output. Use a high value pull-up resistor externally to pull it up to system power supply.
9	7	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BST pins to form a floating supply across the power switch driver. An on-chip regulator is used to charge up the external boot-strap capacitor. If the on-chip regulator is not strong enough, one optional diode can be connected from IN or OUT to charge the external boot-strap capacitor.
10	8	SW	Switch Output. It is the source of power device.

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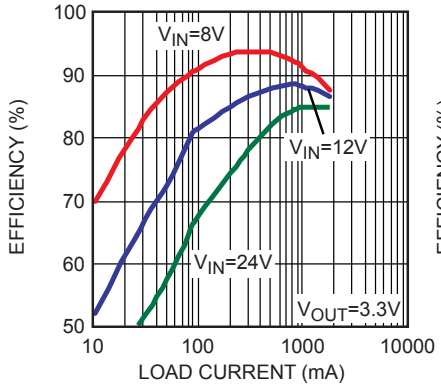
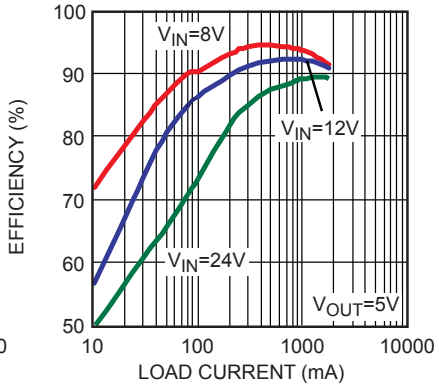
TYPICAL PERFORMANCE CHARACTERISTICS

C1=C2=4.7µF, C3=C4=10µF, C8=0.1µF, L=12µH, T_A=25ºC, unless otherwise noted

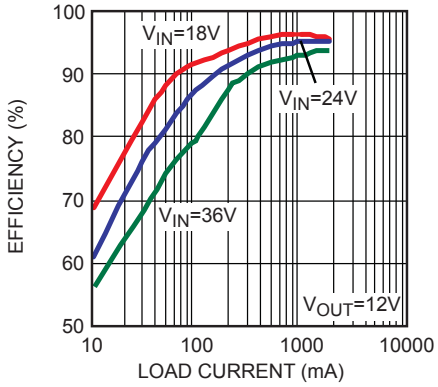
Efficiency vs. Load Current



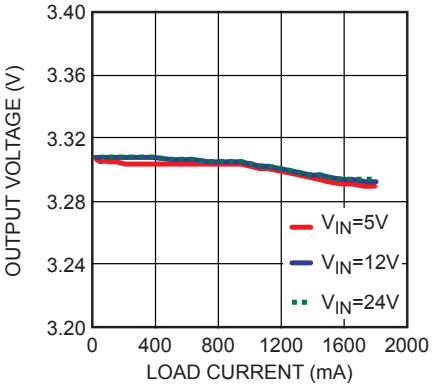
Efficiency vs. Load Current



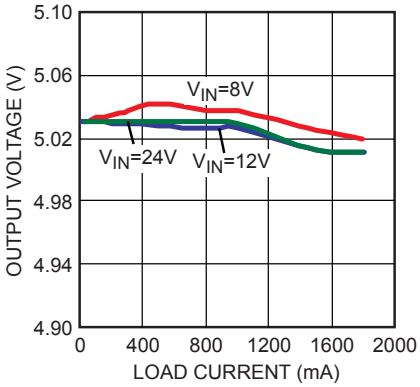
Efficiency vs. Load Current



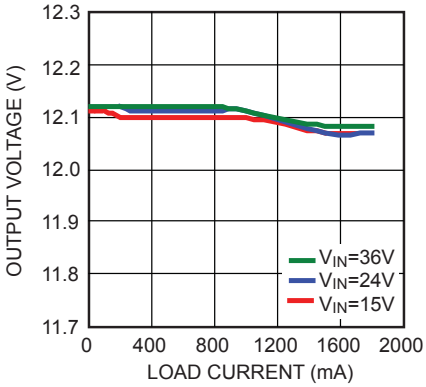
Load Regulation



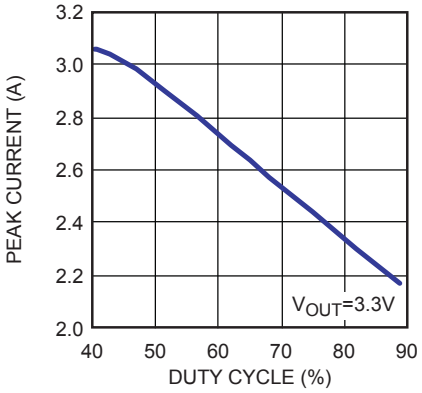
Load Regulation



Load Regulation



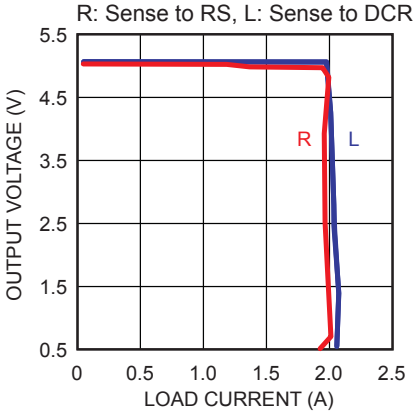
Peak Current vs. Duty Cycle



Current Regulation

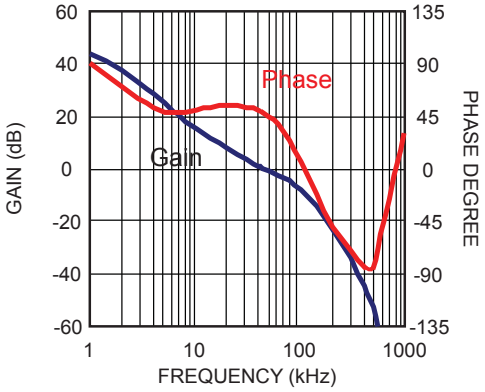
V_{IN} =12V, V_{OUT}=5V

R: Sense to RS, L: Sense to DCR



Loop Gain Bode Plot

V_{IN} =12V, V_{OUT}=5V, I_{OUT}=0.5A



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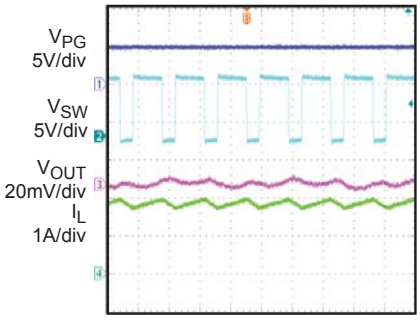
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C1=C2=4.7µF, C3=C4=10µF, C8=0.1µF, L=12µH, T_A=25ºC, unless otherwise noted

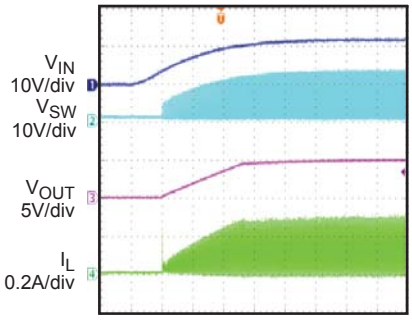
Steady State

V_{IN}=8V, V_{EN} put to V_{IN}
V_{OUT}=5V, I_{OUT}=1.8A, Electrical Load



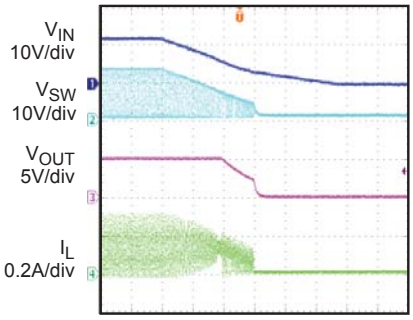
Power Ramp Up

V_{IN}=12V, V_{EN} put to V_{IN}
V_{OUT}=5V, I_{OUT}=130mA, Resistor Load



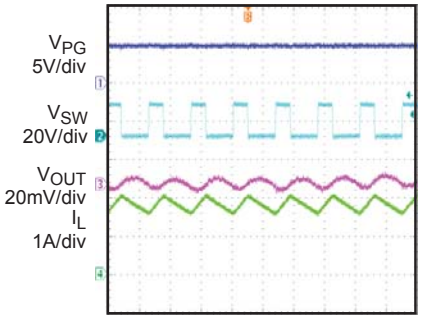
Power Ramp Down

V_{IN}=12V, V_{EN} put to V_{IN}
V_{OUT}=5V, I_{OUT}=130mA, Resistor Load



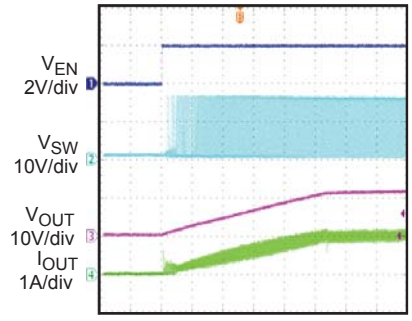
Steady State

V_{IN}=16V, V_{EN} put to V_{IN}
V_{OUT}=5V, I_{OUT}=1.8A, Electrical Load



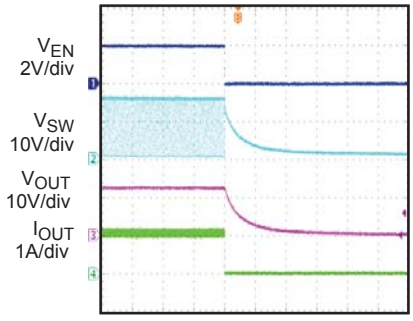
Enable Up

V_{IN}=15V, V_{EN} put to V_{IN}
V_{OUT}=12V, I_{OUT}=1A, Resistor Load



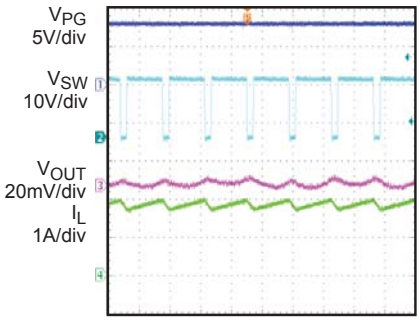
Enable Down

V_{IN}=15V, V_{EN} put to V_{IN}
V_{OUT}=12V, I_{OUT}=1A, Resistor Load



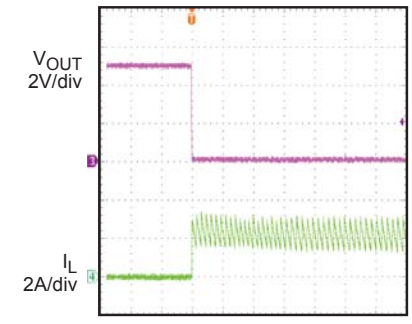
Steady State

V_{IN}=15V, V_{EN} put to V_{IN}
V_{OUT}=12V, I_{OUT}=1.8A, Electrical Load



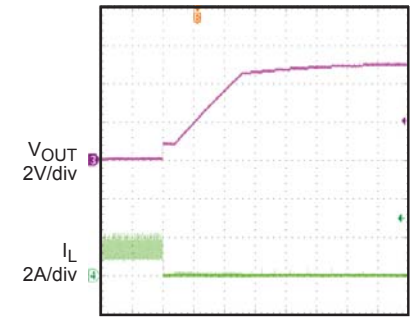
Short Circuit

V_{IN}=12V, V_{EN} put to V_{IN}
V_{OUT}=5V



Short Circuit Recovery

V_{IN}=12V, V_{EN} put to V_{IN}
V_{OUT}=5V



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OPERATION

Main Control Loop

The MP2490 is a current mode buck regulator. That is, the error amplifier (EA) output voltage is proportional to the peak inductor current.

At the beginning of a cycle, the integrated high side power switch M1 (Fig.1) is off; the EA output voltage is higher than the current sense amplifier output; and the current comparator's output is low. The rising edge of the 700kHz clock signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is added to Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and the MP2490 reverts to its initial M1 off state.

If the Current Sense Amplifier plus Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.8V bandgap reference. The polarity is such that a FB pin voltage lower than 0.8V increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage increases current delivered to the output. An external Schottky Diode (D1) carries the inductor current when M1 is off.

Load Current Limiting Loop

The output current information is sensed via the ISP and ISN pins. The regulation threshold is set at 100mV. If V_{SENSE}, the difference of V_{ISP} and V_{ISN}, is less than 100mV, the output voltage of the power supply will be set by the FB pin. If V_{SENSE} reaches 100mV, the current limit loop will pull down SS and regulate the output at a constant current determined by the external sense resistor. The external capacitor on SS pin is the dominant compensation capacitor for load current regulation loop. The capacitor has normal value of 100nF, which will put the bandwidth of load current regulation loop to be less than 1 kHz. When V_{SENSE} is higher than 100mV, SS will not drop down to the final regulation level immediately. It will cause the load current to be higher than the programmed level for a short period. A fast comparator is added to shut down power switch when the average load current is higher than 120% of the programmed current limit level.

An inductor DC resistance (DCR) or accurate sense resistor can be used for load current sensing.

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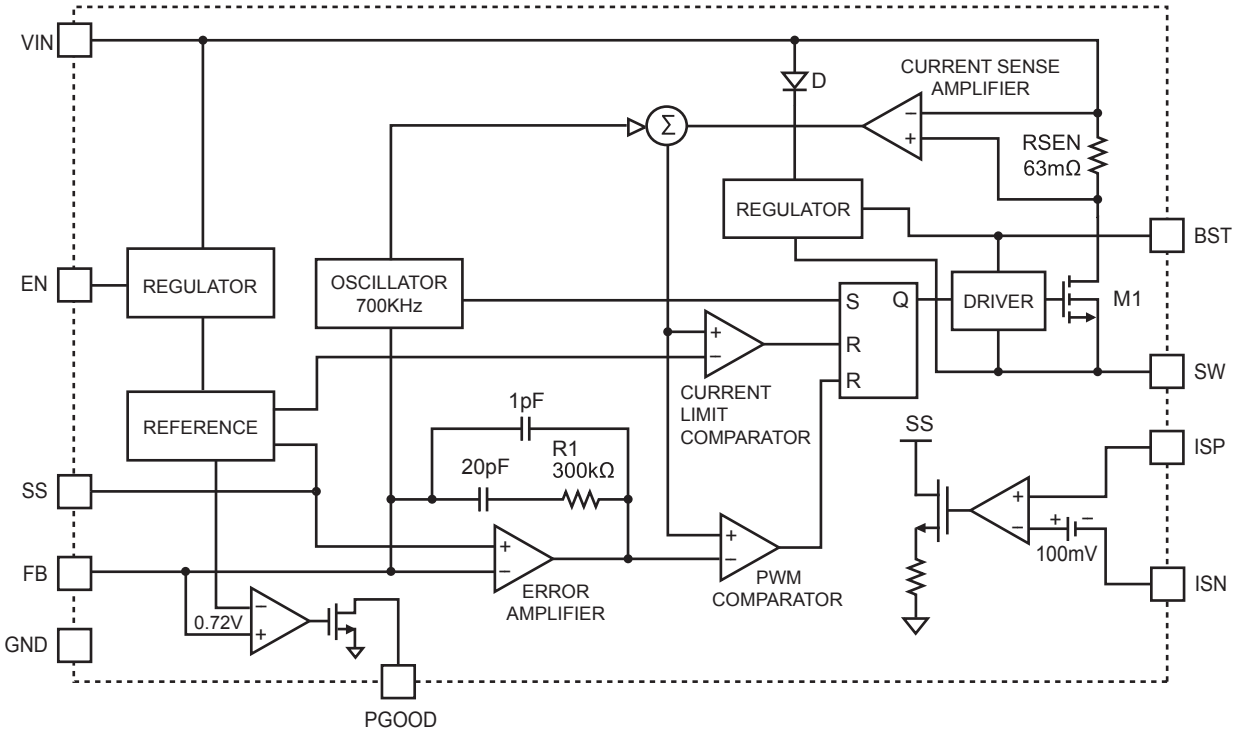

Figure 1—Functional Block Diagram

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). Choose R1 to be around 300kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	300 (1%)	240 (1%)
2.5	300 (1%)	141.1 (1%)
3.3	300 (1%)	96 (1%)
5	300 (1%)	57.1 (1%)

Selecting the Inductor

A 1μH to 15μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 200mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current ripple to be approximately 30% of the maximum load current,. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and also the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from pass to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps output voltage small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended.

PC Board Layout

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network. ISN, ISP are sensitive nodes. Put the sensing components as close to the device as possible and keep them away from the high current and noisy paths such as GND, IN, SW). Match the trace and components on ISN, ISP paths as good as possible.

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Output Current Sensing

The output current can be sensed through the DC resistance (DCR) of the inductor, as shown in Figure 2a.

In Figure 2a, the output current limit is set as:

$$I_{OUT} = \frac{100mV}{DCR} \times \frac{R_a + R_b}{R_b}$$

Where DCR is the DC resistance of the inductor winding.

In Figure 2a, it is desirable to keep

$$\frac{R_a \cdot R_b}{R_a + R_b} \times C_S = \frac{L1}{DCR}$$

If, there is no Rb:

$$R_a \times C_s = \frac{L1}{DCR}$$

For more accurate sensing, use a more accurate sense resistor, as in Figure 2b, where the output current limit is set as:

$$I_{OUT} = \frac{100mV}{R_{SENSE}}$$

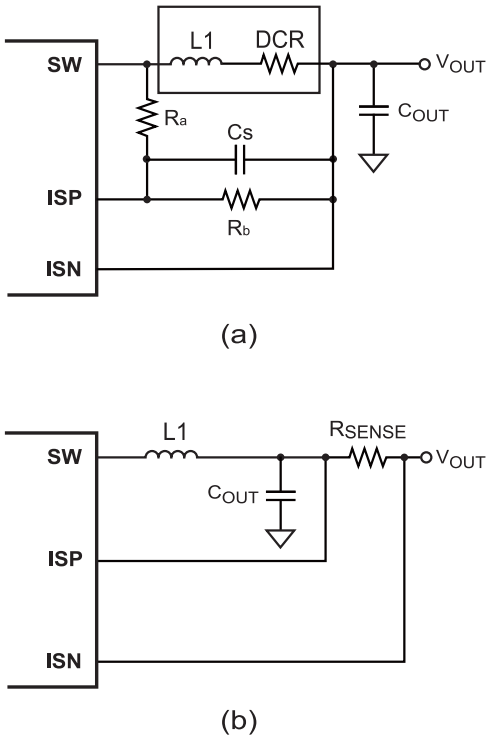

Figure 2—Current Sensing Methods

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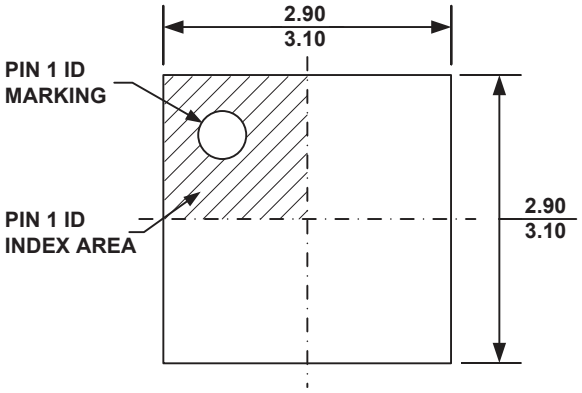
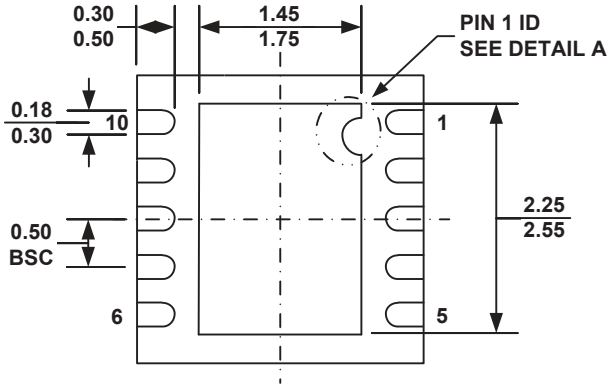
PACKAGE INFORMATION

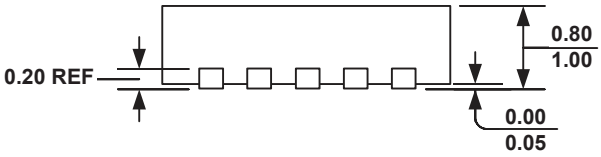
QFN10 (3mm x 3mm)



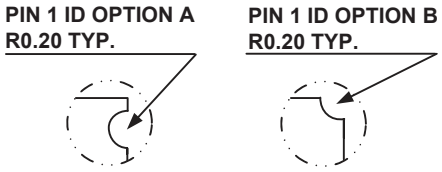
TOP VIEW



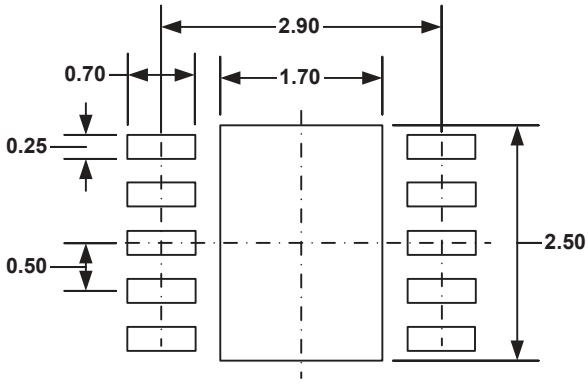
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

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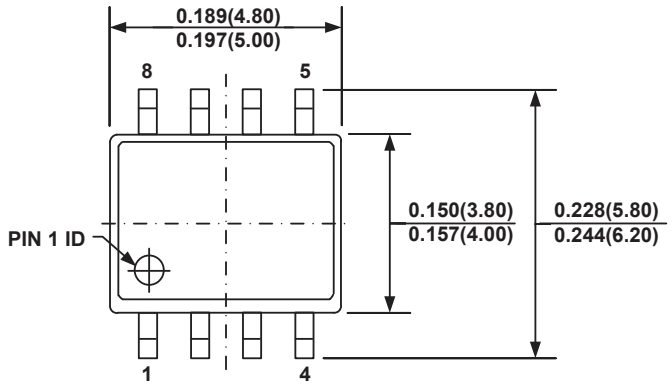
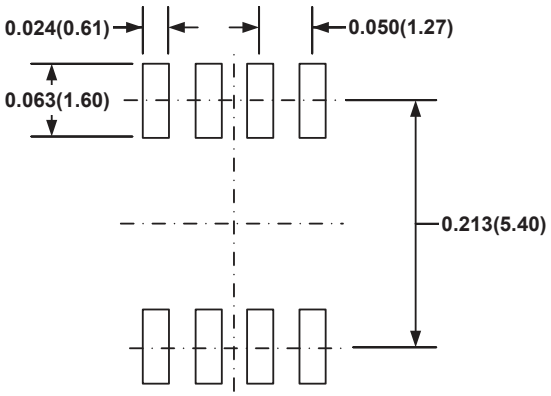
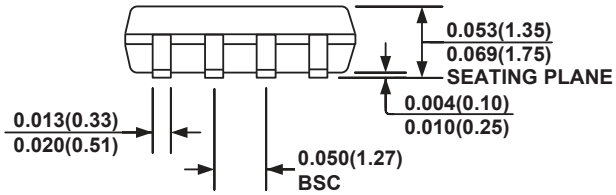
SOIC8



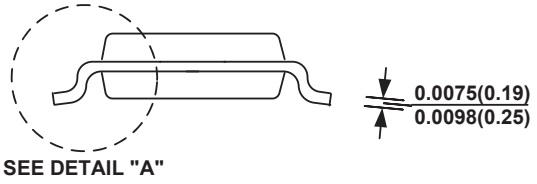
TOP VIEW



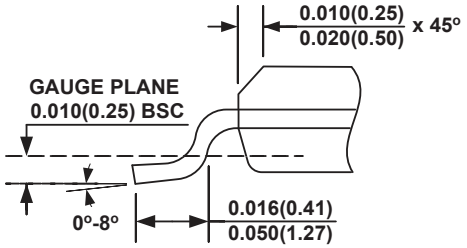
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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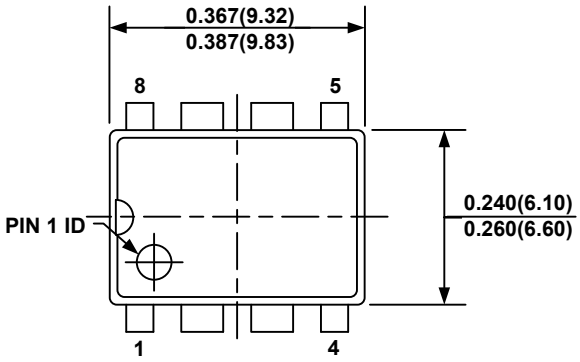
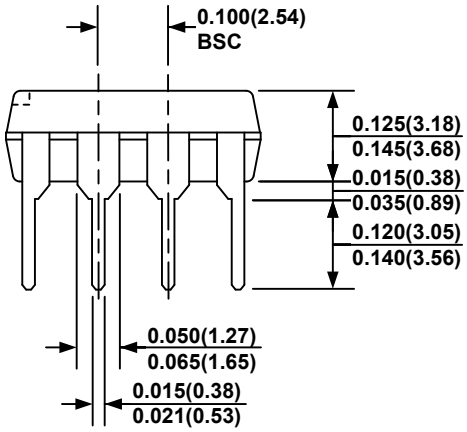
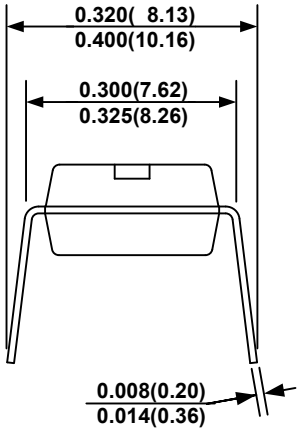
PDIP8



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH, OR PROTRUSIONS.
3) DRAWING CONFORMS TO JEDEC MS-001, VARIATION BA.
4) DRAWING IS NOT TO SCALE.

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