MP5921

16V, 50A, 1mΩ $R_{DS(ON)}$, Hot-Swap Intelli-Fuse Solution

The Future of Analog IC Technology

DESCRIPTION

The MP5921 is a monolithic, integrated controller and switch that contains a high-side MOSFET and other circuitries that enable it to work in standalone operation or to be controlled by a hot-swap controller. The MP5921 drives up to 50A of continuous current per device at room temperature. With air flow, the continuous current can reach 60A.

The MP5921 limits the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop. The MP5921 limits the internal MOSFET current by controlling the gate voltage through the current limit reference input and soft-start ramp.

The MP5921 offers many features to simplify system design. It provides an integrated current mirror to monitor the output current and on-die temperature sensing, eliminating the need for an external current-sense power resistor, power MOSFET, and thermal sense device.

The MP5921 detects the power FET gate, source, and drain short conditions and can feedback to the hot-swap controller via the fault reporting output (GOK). The MP5921 can be paralleled for higher current applications. All devices in parallel share current actively during soft start.

The MP5921 is available in a QFN-28 (4mmx5mm) package.

FEATURES

- 4V to 16V Operating Input Range
- Maximum 50A Output Current
- Supports 60A of Output Current with Air Flow
- Integrated Switch with 1mΩ $R_{DS(ON)}$
- Built-In MOSFET Driver
- 3.0V LDO Output
- Integrated Current Sensing with Sense Output
- Separate Current Sensing Output Used to Program Over-Current Value
- Built-In Insertion Delay
- Adjustable Soft Start (SS)
- Output Short-Circuit Protection (SCP)
- Over-Temperature Protection (OTP)
- Built-In Fuse Health Reporting
- Fault Signal Output
- Parallel Operation for High-Current Applications
- Integrated Intelli-Fuse Temperature Sense
- Output Voltage Power-Down Control
- Available in a FCQFN-28 (4mmx5mm) Package

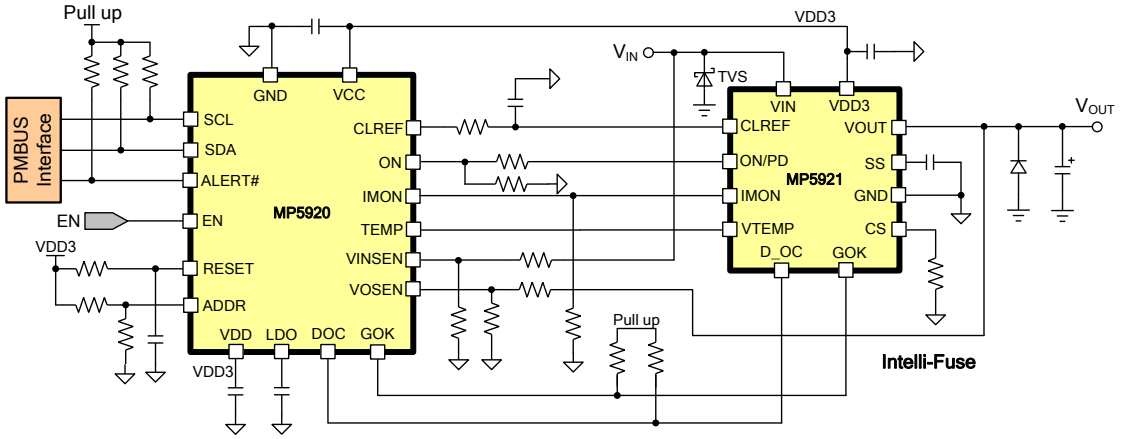
APPLICATIONS

- Hot Swap
- PC Cards
- Disk Drives
- Servers
- Networking

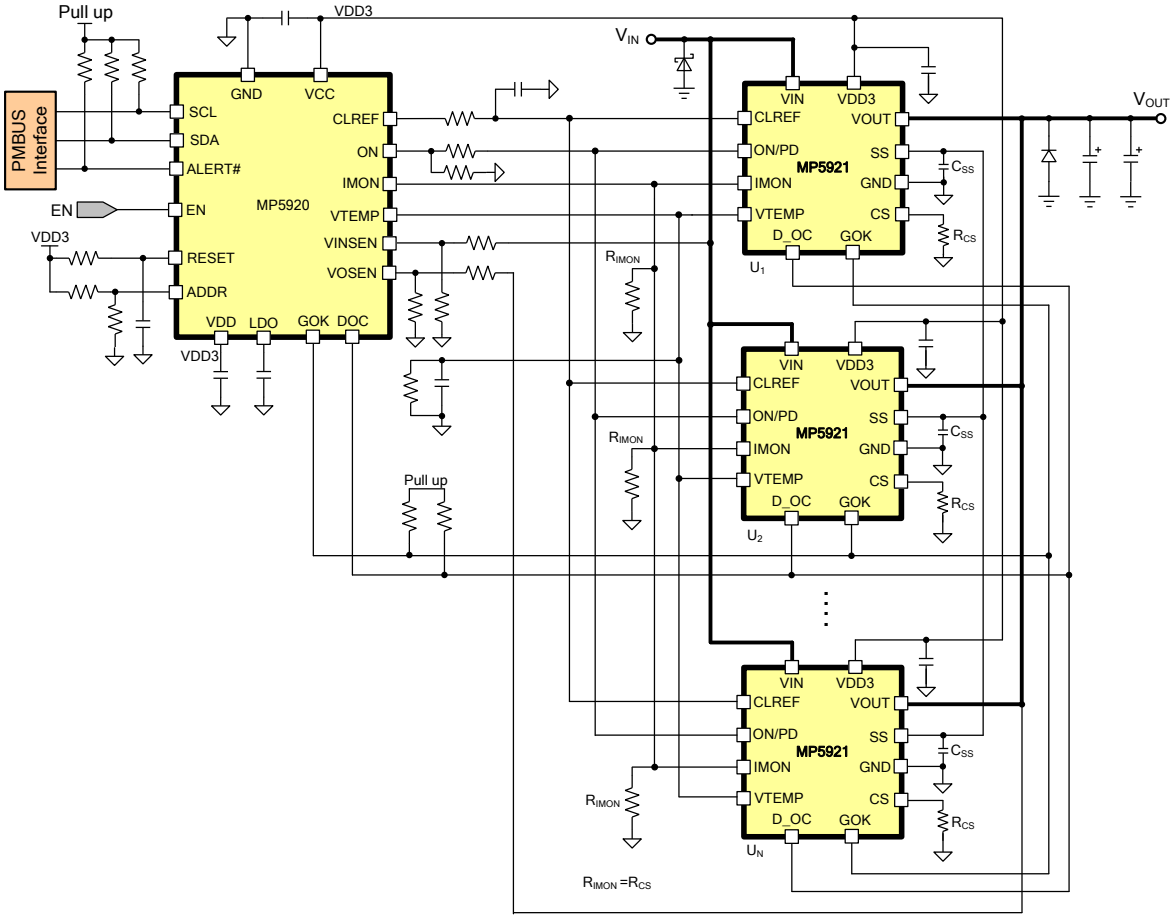
All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are registered trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION



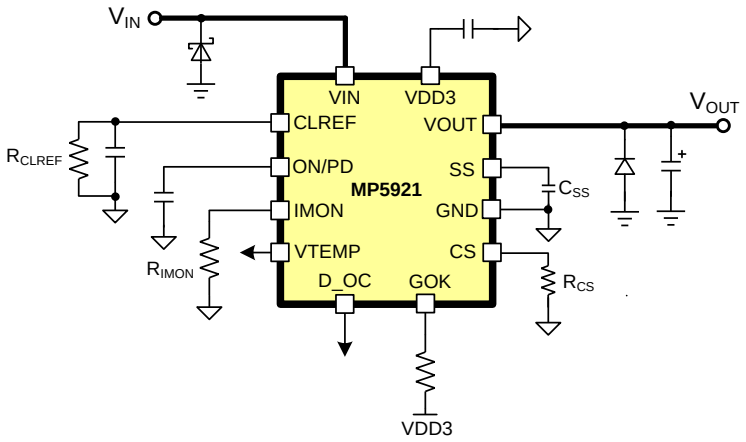
MP5921 Controlled by Hot-Swap Controller



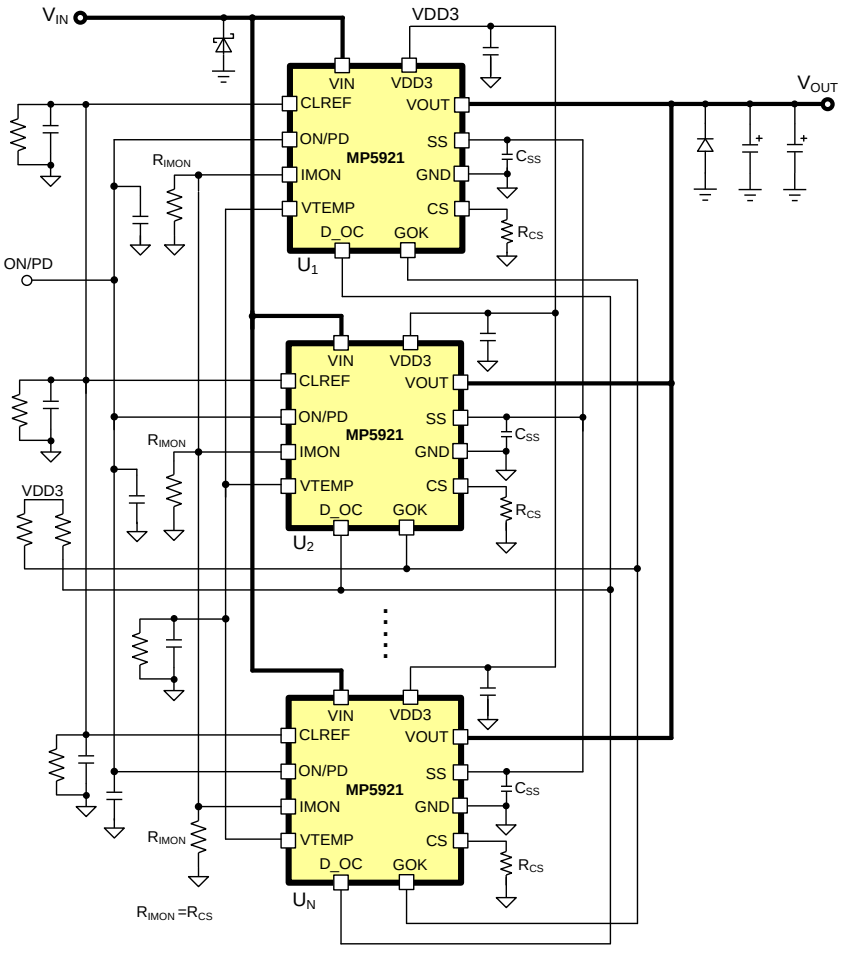
MP5921 Controlled by Hot-Swap Controller in Parallel Application

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION *(CONTINUED)*



MP5921 Standalone Operation (Set $R_{IMON} \geq R_{CS}$)



MP5921 Standalone Parallel Operation

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5921GV	QFN-28 (4mmx5mm)	*See Below*

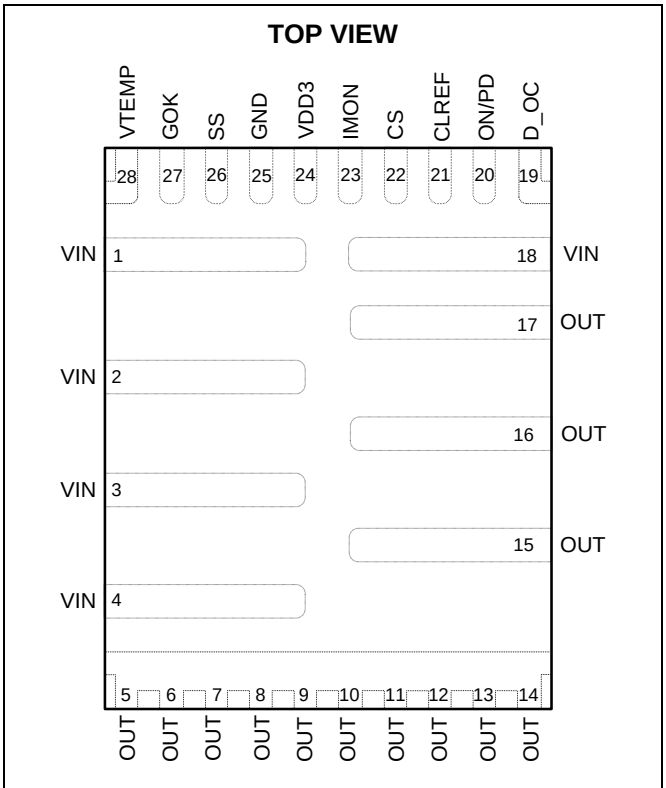
* FOR TAPE & REEL, ADD SUFFIX –Z (E.G. MP5921GV–Z)

TOP MARKING

MPSYWW
MP5921
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP5921: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-28 (4mmx5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

VIN (DC) .....-0.3V to +20V
VIN (1µs)..... +24V
VIN (25ns)..... +29V
OUT .....-0.3V to +20V
All other pins .....-0.3V to +4.2V
Continuous power dissipation (T_A = 25°C) (2) 3.29W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +155°C

Recommended Operating Conditions (3)

Input voltage operating range .....4V to 16V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
FCQFN-28 (4mmx5mm)	38	8	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

VIN = 12V, R_{CS} = 2kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_Q	Intelli-Fuse on, no load		1.8	2.7	mA
		Fault latch off		1.5	2.4	mA
		Intelli-Fuse off, VIN = 16V		1.6	2.5	mA
VDD3 Regulator and Under-Voltage Lockout (UVLO)						
VDD3 regulator output voltage	VDD3	I_{VDD3} = 0mA	2.855	3.05	3.245	V
VDD3 regulator load capability	I_{VDD3}	VOL = VDD3 - 40mV	14	15	16	mA
VDD3 under-voltage lockout threshold rising	VDD_{VTH}		2.28	2.41	2.54	V
VDD33 under voltage lockout threshold falling	VDD_{VTL}		1.9	2.04	2.18	V
VDD3 under-voltage lockout threshold hysteresis	VDD_{HYS}			370		mV
VIN Under-/Over-Voltage Protection (UVP, OVP)						
VIN under-voltage lockout threshold rising	VIN_{VTHR}		2.74	2.91	3.08	V
VIN under-voltage lockout threshold falling	VIN_{VTHF}		2.38	2.58	2.78	V
VIN over-voltage protection	VIN_{OVP}		17	18.5	20	V
Power MOSFET						
On resistance	$R_{DS(ON)}$	T_J = 25°C		1	1.25	mΩ
		T_J = 125°C (5)		1.35	1.625	
Off-state leakage current	I_{OFF}	VIN = 16V, power FET off			1	μA
Short-Circuit Current Limit						
Short-circuit current limit (5)	$I_{LimitSC}$		80	100	120	A
Short-circuit protection response time (5)	t_{SC}			200		ns
Current Limit Reference (CLREF)						
Internal CLREF current	I_{CLREF}		8.5	10	11.5	μA
CLREF internal max current limit clamp	V_{CLREF_CLAMP}	V_{BE} at V_{OUT} < 80%VIN, T_J = 25°C	570	635	699	mV
		V_{BE} at V_{OUT} < 80 VIN, T_J = 125°C (5)	370	440	510	mV
		V_{OUT} ≥ 80%VIN	1.44	1.6	1.76	V
CLREF over-current regulation time	t_{CL_REG}	V_{OUT} ≥ 90%VIN, CLREF ≥ 0.3V	120	180	265	μs
Short-circuit start-up protection timer	t_{SC_TIMER}	V_{OUT} < 1/8VIN, power FET current is regulated by V_{BE}		2.1	3.2	ms
Current Sense Output (CS)						
CS sense gain		I_{OUT} > 5A	9.7	10	10.3	μA/A
CS sense gain offset		I_{OUT} > 5A	-2.5		2.5	μA
Over-current D_OC high to low threshold	V_{DOC_TH}	V_{OUT} ≥ 90%VIN, 0.3V ≤ CLREF ≤ 1.6V	0.8	0.85	0.9	V_{CLREF}

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

VIN = 12V, R_{CS} = 2kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VTEMP						
VTEMP sense gain (5)		Sense range 0 - 140°C	8	8.7	9.4	mV/ °C
VTEMP sense output (5)		T_J = 25°C		370		mV
Soft Start (SS)						
SS pull-up current	I_{SS}	VIN = 12V, I_{SS} dependent VIN	13	15	17	µA
Current Monitor Output (IMON)						
IMON sense gain		I_{OUT} > 5A	9.7	10	10.3	µA/A
IMON sense gain offset		I_{OUT} > 5A	-2		2	µA
ON/PD						
Internal ON/PD current	I_{ON_PD}		3.2	4.2	5.2	µA
FET on insertion delay time	T_{DLY_ON}	VIN and VDD3 > UVLO		1.3	1.8	ms
FET on input rising threshold	V_{ON_vth}	ON/PD rising	1.26	1.4	1.54	V
FT on hysteresis	V_{ON_hys}			200		mV
FET on to PD mode threshold	$V_{PD_vth_fall}$	ON/PD falling	1.08	1.2	1.32	V
PD mode to off mode threshold	$V_{OFF_vth_fall}$	ON/PD falling	0.68	0.76	0.84	V
PD mode pull-down resistor	R_{PD}		250	500	750	Ω
PD mode pull-down delay time	t_{PD_DLY}			2.1	3.2	ms
Thermal Shutdown						
Over-temperature shutdown and GOK fault flag	t_{STD}			143		°C
GOK Output						
Output low voltage	V_{OL_GOK}	Sink current 1mA			0.2	V
GOK bar off-state leakage current	I_{GOK_LKG}	V_{GOK} = 3.3V			1	µA
D_OC Output						
Output low voltage	V_{OL_DOC}	Sink current 1mA			0.2	V
D_OC bar off-state leakage current	I_{DOC_LKG}	V_{D_OC} = 3.3V			1	µA
FET Short Detection						
GOK fault flag for FET drain-to-source short	V_{OUT_DSTH}	Measured at V_{OUT} during start-up	85%	90%	95%	VIN
GOK release high flag when drain-to-source short is removed	V_{OUT_GOKH}			70%	74%	VIN
Maximum soft-start time	T_{SS_MAX}	After ON_PD goes high, if V_{OUT} < 90%VIN within 270ms, indication of fuse is not fully on	200	270	340	ms

NOTE:

5) Guaranteed by design.

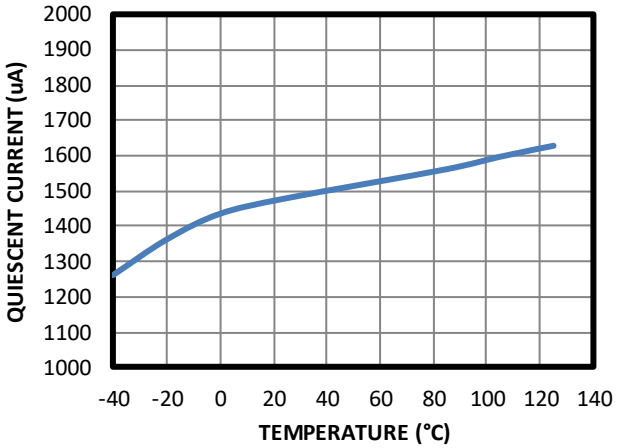
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

VIN = 12V, R_{CS} = R_{IMON} = 2kΩ, T_A =+ 25°C, unless otherwise noted.

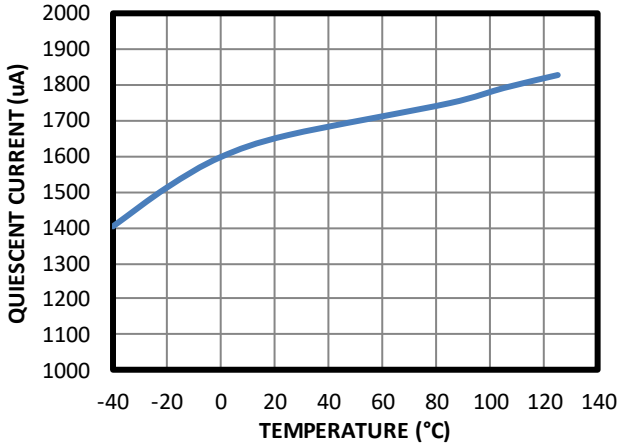
Quiescent Current vs. Temperature

ON/PD = LOW, VIN = 16V

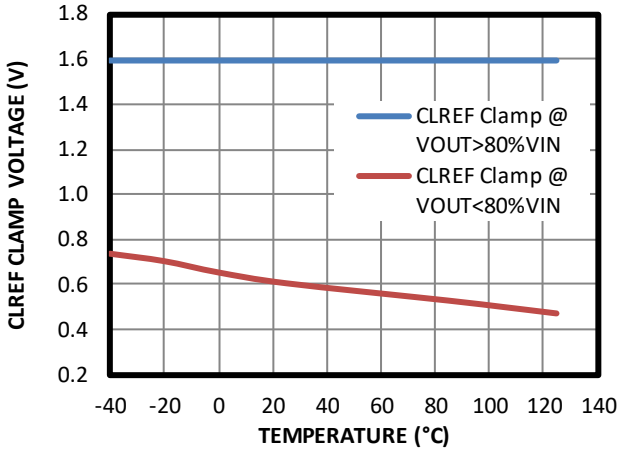


Quiescent Current vs. Temperature

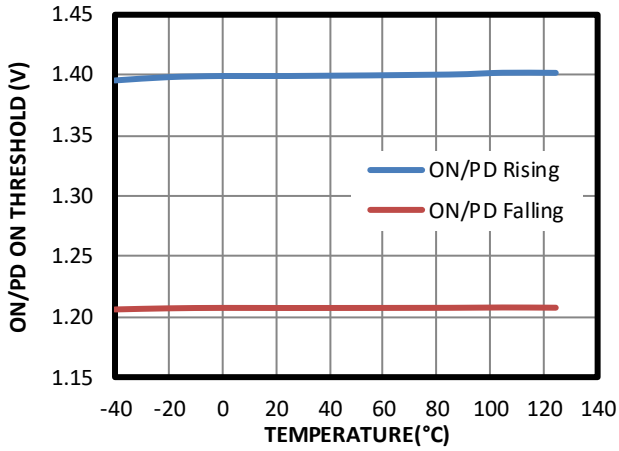
ON/PD = High



CLREF Clamp Voltage vs. Temperature

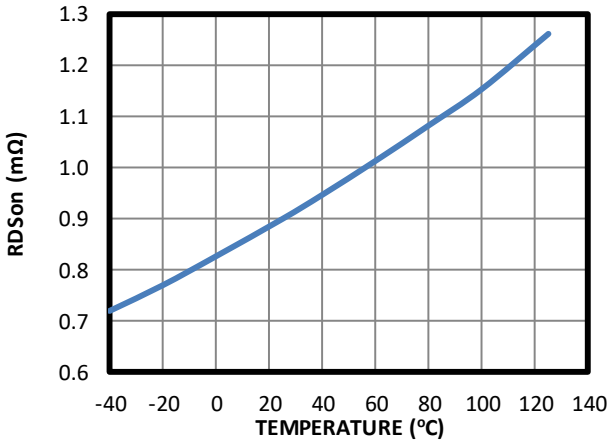


ON/PD FET On/Off Threshold vs. Temperature

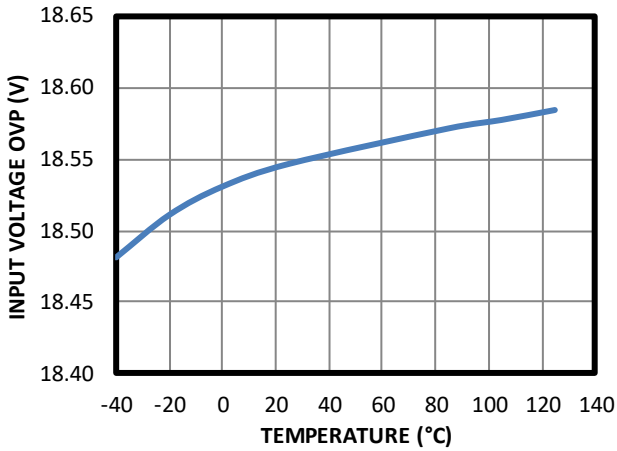


$R_{DS(ON)}$ vs. Temperature

I_{OUT} = 2A



VIN OVP vs. Temperature

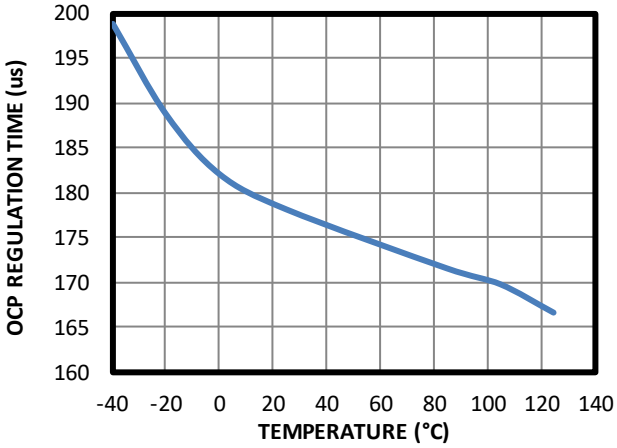


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

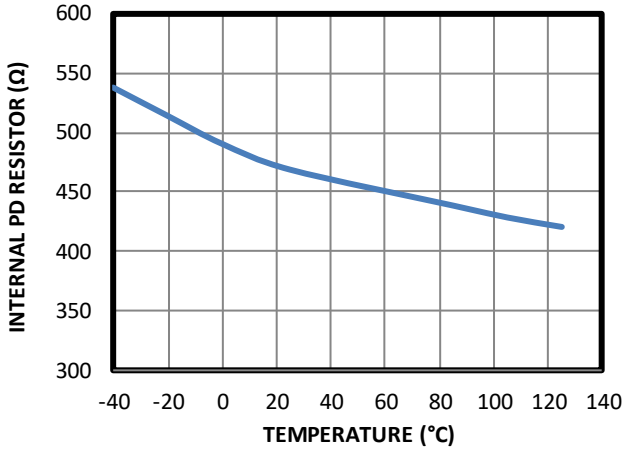
TYPICAL CHARACTERISTICS *(continued)*

VIN = 12V, R_{CS} = R_{IMON} = 2kΩ, T_A = +25°C, unless otherwise noted.

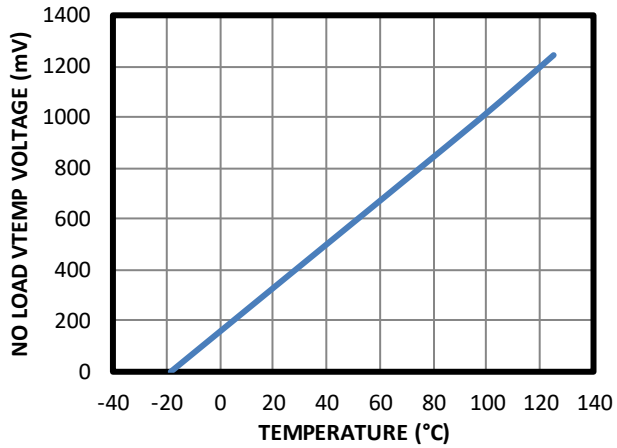
OCP Regulation Time vs. Temperature



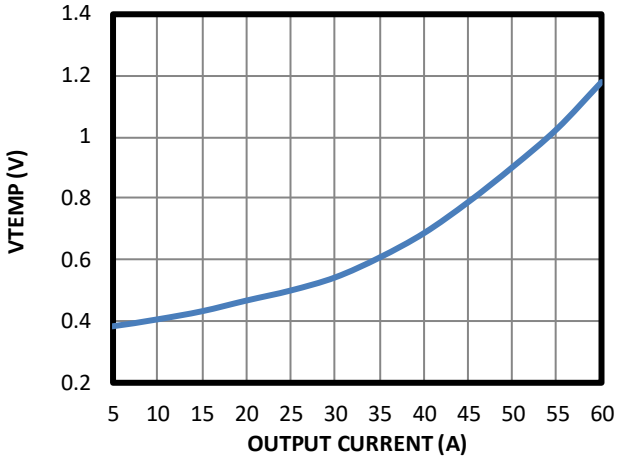
Internal PD Resistor vs. Temperature



No Load V_{TEMP} Voltage vs. Temperature

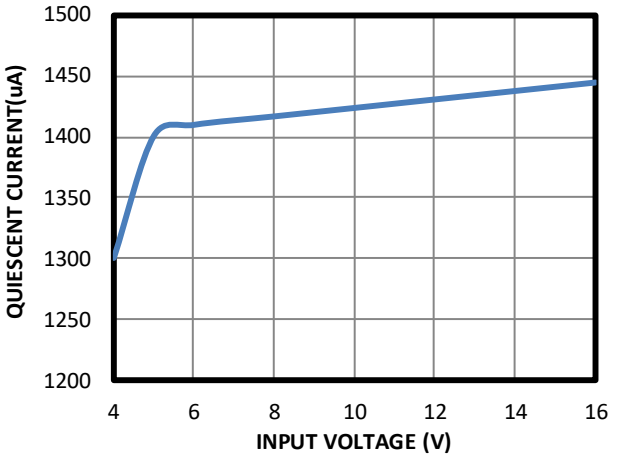


V_{TEMP} Voltage vs. Output Current



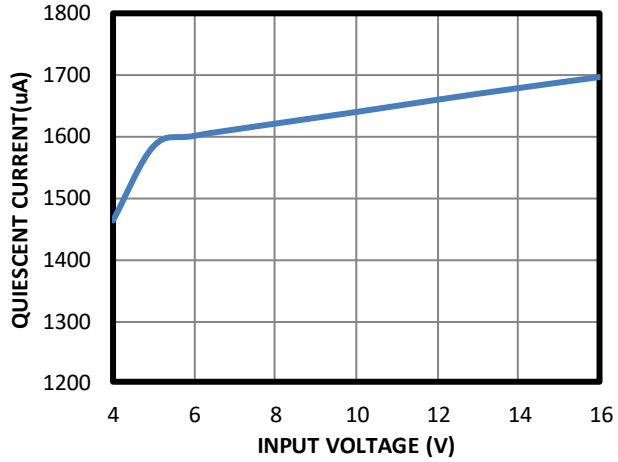
Supply Current vs. Input Voltage

ON/PD = Low



Supply Current vs. Input Voltage

ON/PD = High

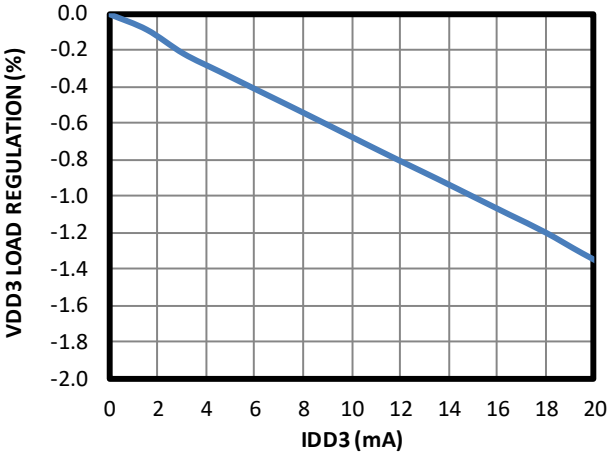


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

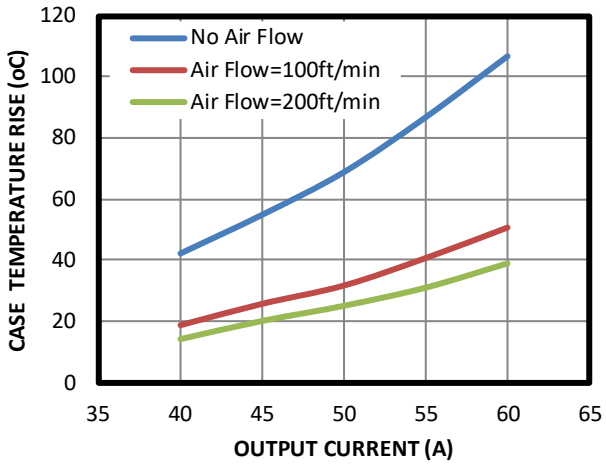
TYPICAL CHARACTERISTICS *(continued)*

VIN = 12V, R_{CS} = R_{IMON} = 2kΩ, T_A = +25°C, unless otherwise noted.

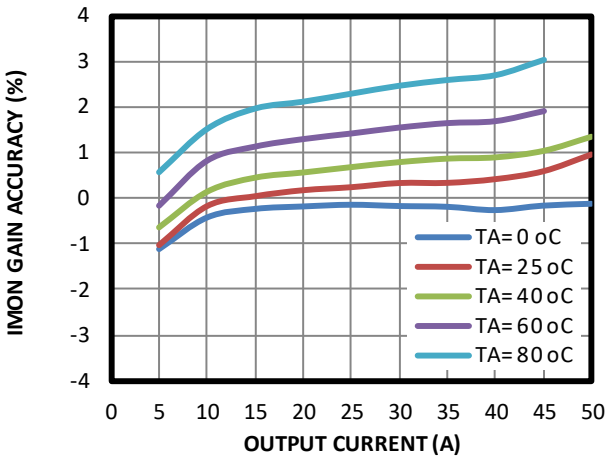
VDD3 Load Regulation



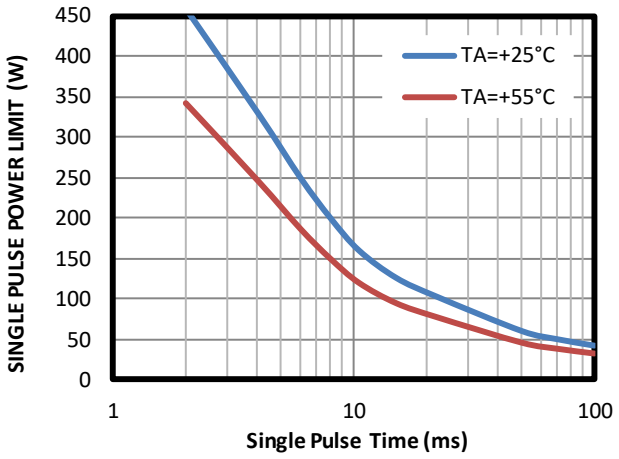
Case Temperature Rise



I_{MON} Gain Accuracy vs. Output Current and Temperature



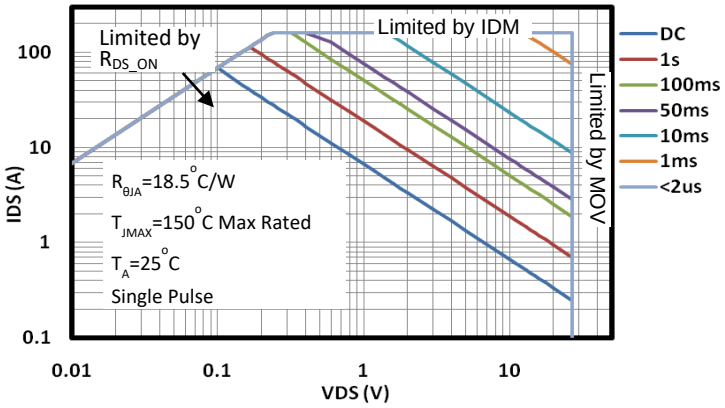
Single Pulse Power Limit before OTP



Safe Operating Area

Tested on EV5921-V-00A

4-Layers, 2oZ each layer, 11cmx12.07cm



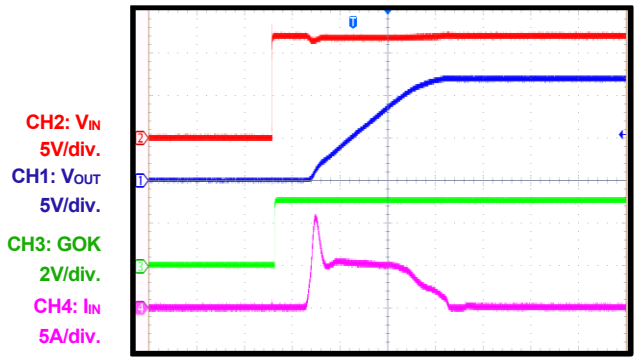
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, C_{OUT} = 4700µF, C_{SS} = 100nF, R_{CS} = R_{IMON} = 2kΩ, R_{CLREF} = 110kΩ, GOK is pulled up to VDD3, T_A = +25°C, unless otherwise noted.

VIN Hot Plug

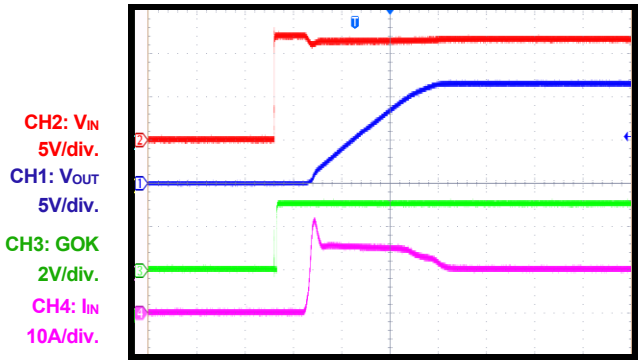
I_{OUT} = 0A



4ms/div.

VIN Hot Plug

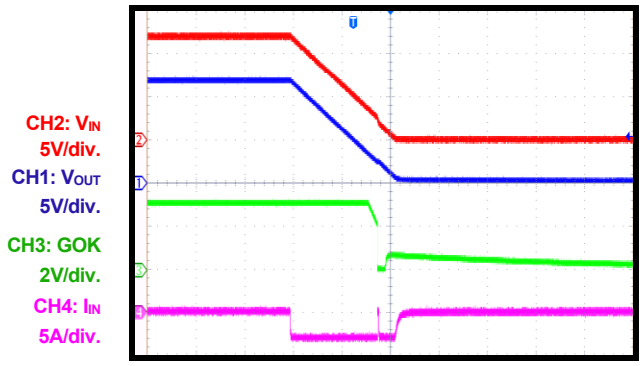
I_{OUT} = 10A



4ms/div.

Shutdown through VIN

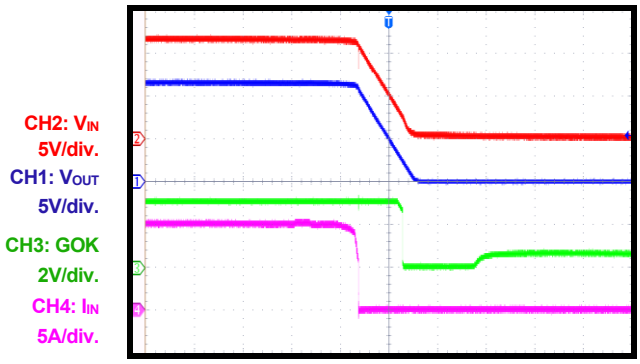
I_{OUT} = 0A



40ms/div.

Shutdown through VIN

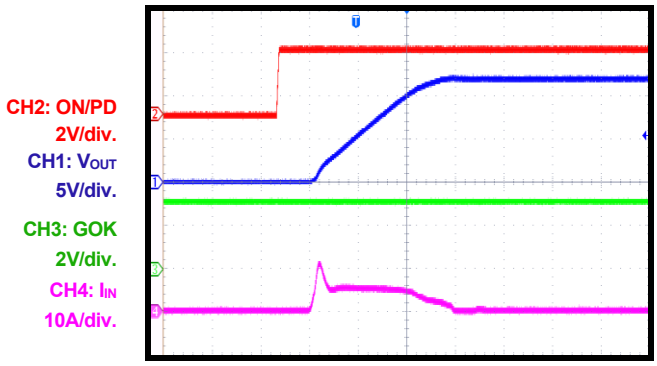
I_{OUT} = 15A



4ms/div.

Start-Up through ON/PD

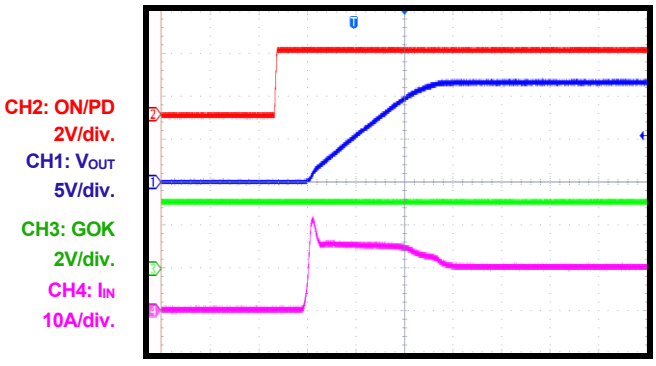
I_{OUT} = 0A



4ms/div.

Start-Up through ON/PD

I_{OUT} = 10A



4ms/div.

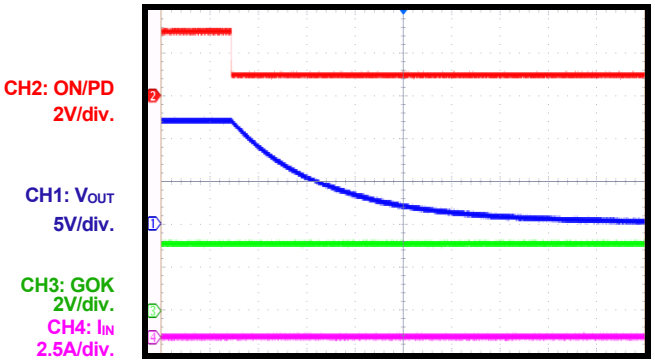
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, C_{OUT} = 4700µF, C_{SS} = 100nF, R_{CS} = R_{IMON} = 2kΩ, R_{CLREF} = 110kΩ, GOK is pulled up to VDD3, T_A = +25°C, unless otherwise noted.

Shutdown through ON/PD

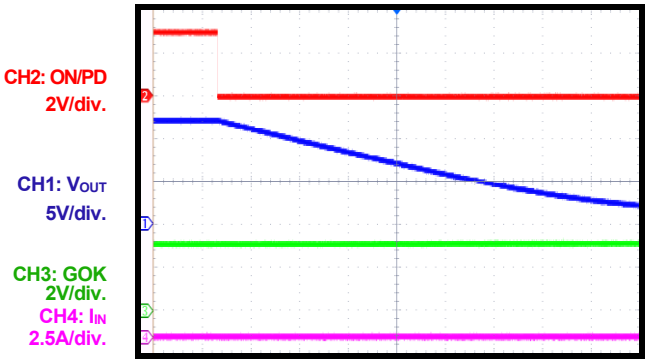
I_{OUT} = 0A, C_{OUT} = 4700µF, w/ PD



1s/div.

Shutdown through ON/PD

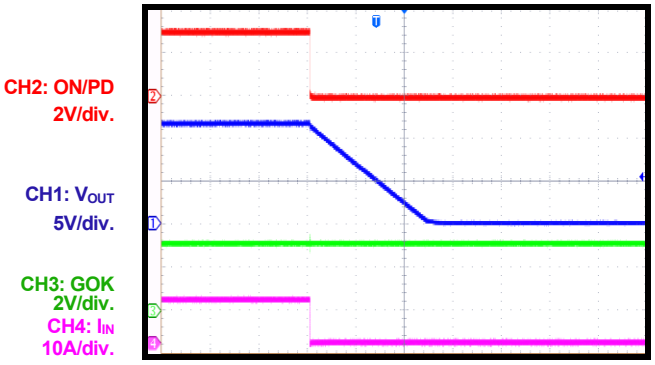
I_{OUT} = 0A, C_{OUT} = 4700µF, w/o PD



4s/div.

Shutdown through ON/PD

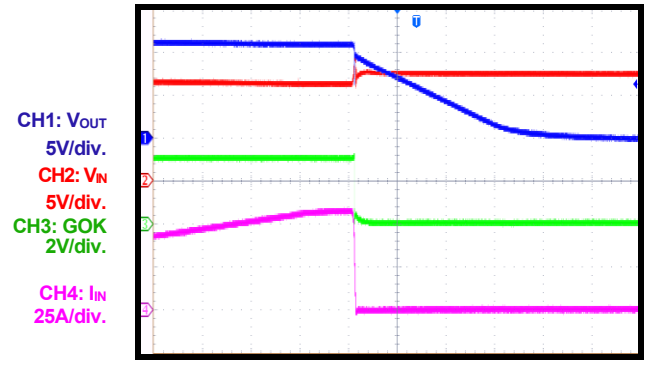
I_{OUT} = 10A, w/o PD



2ms/div.

OCP

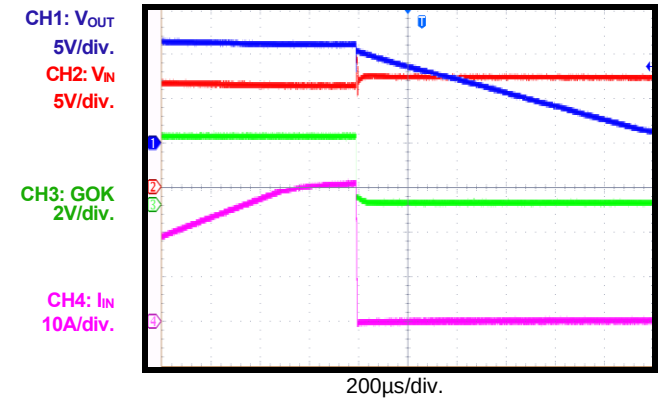
CLREF = 1.1V, I_{LIMIT} = 55A



200µs/div.

OCP

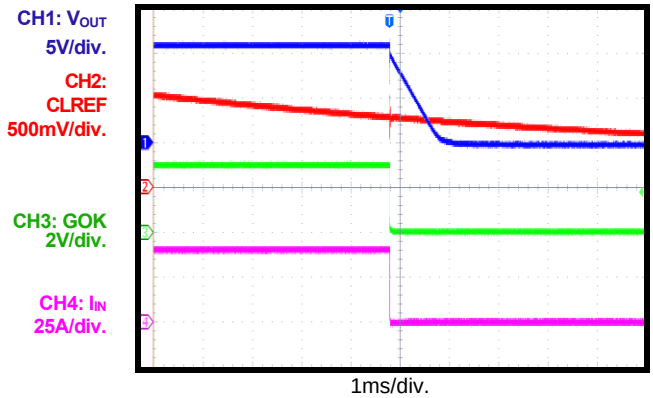
CLREF = 0.6V, I_{LIMIT} = 30A



200µs/div.

OCP

I_{OUT} = 40A, Decrease CLREF from 1.1V to 0V



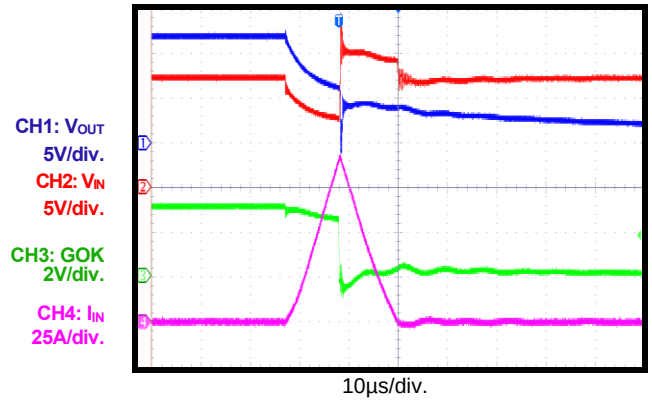
1ms/div.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

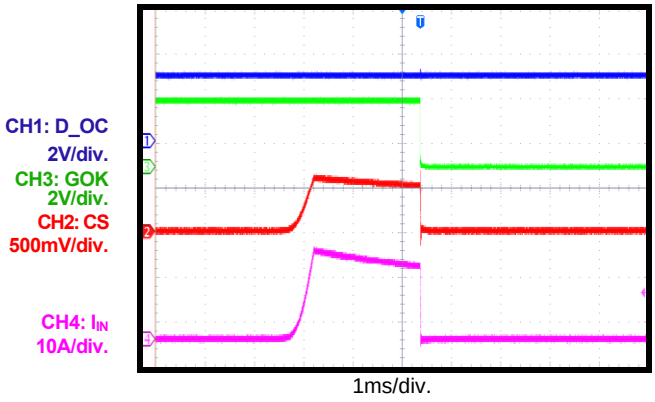
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, C_{OUT} = 4700µF, C_{SS} = 100nF, R_{CS} = R_{IMON} = 2kΩ, R_{CLREF} = 110kΩ, GOK is pulled up to VDD3, T_A = +25°C, unless otherwise noted.

SCP Entry

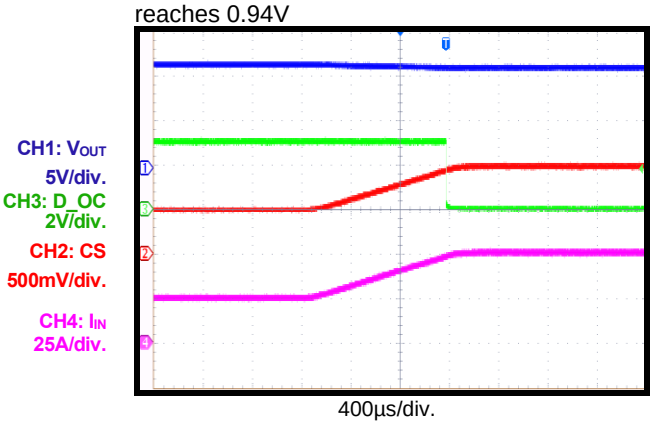


Short-Circuit Start-Up



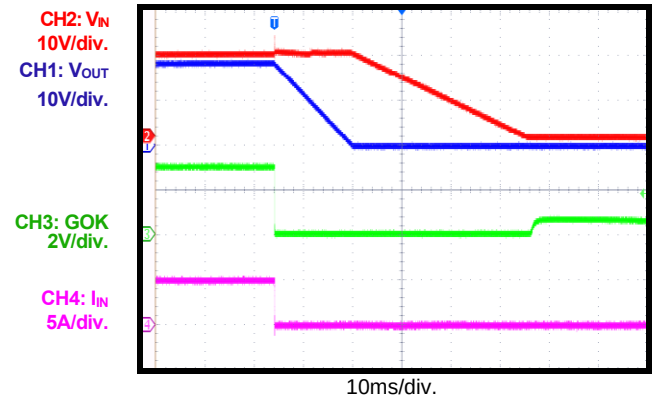
D_OC Status at Normal Operation

Increase Load, D_OC is pulled down when CS reaches 0.94V



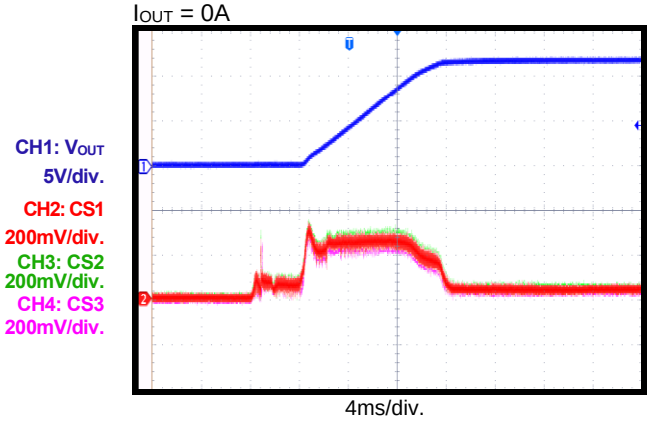
VIN OVP

I_{OUT} = 5A, apply 18.5V on VIN, then turn off VIN



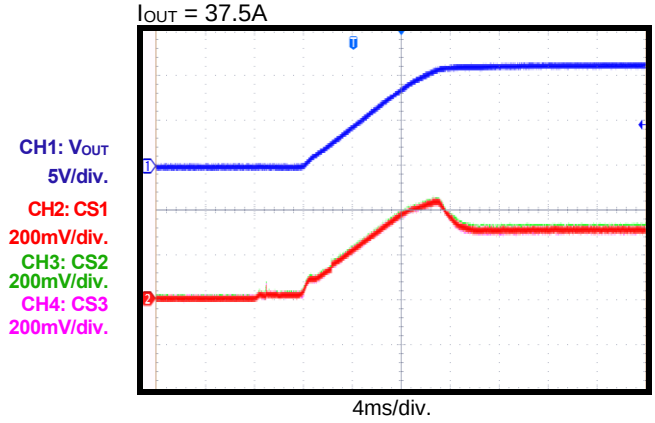
Current Balance During Start-Up at Paralleling

3-MP5921 parallel, R_{IMON} = RCS per MP5921, I_{OUT} = 0A



Current Balance During Start-Up at Paralleling

3-MP5921 parallel, R_{IMON} = RCS per MP5921, I_{OUT} = 37.5A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1 - 4, 18	VIN	**System input power supply.** The MP5921 operates from a 4V to 16V input rail.
5 - 17	OUT	**Output voltage controlled by the IC.** OUT is connected to the source of the integrated MOSFET.
19	D_OC	**Digital output of the over-current indication.** D_OC is an open-drain output. When the CS voltage (V_{CS}) is higher than 85% of CLREF, the D_OC logic is pulled low.
20	ON/PD	**Power FET on/off control or OUT voltage pull-down mode control.** Drive ON/PD above 1.4V to turn on the power FET. Drive ON/PD low to turn off the power FET. Force the ON/PD voltage to around 1V to pull down V_{OUT} with an integrated 500Ω resistor after a 2.1ms delay. Connect a 10kΩ resistor from ON/PD to the hot-swap controller when the MP5921 is controlled by the controller. Do not float ON/PD.
21	CLREF	**Current-limit reference voltage input.**
22	CS	**Current sense output.** CS requires an external resistor. The CS voltage (V_{CS}) is compared with CLREF to determine the current limit.
23	IMON	**Current monitor output.** The output current is proportional to the current flowing through the power device.
24	VDD3	**Internal 3.0V LDO output.** VDD3 can be driven with an external 3.3V to reduce loss from VIN. Place a 1µF decoupling capacitor close to VDD3 and GND.
25	GND	**Signal ground.**
26	SS	**Soft-start set.** An external capacitor connected to SS sets the soft-start time of the output voltage. The internal circuit controls the slew rate of the output voltage during turn-on.
27	GOK	**Intelli-Fuse fault reporting output.** GOK asserts low and latches after a fault occurs. The faults that can trigger GOK include over-current fault (during normal operation), short-circuit fault, over-temperature fault, and FET health fault. GOK is an open-drain output pin.
28	VTEMP	**Junction temperature sense output.**

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

BLOCK DIAGRAM

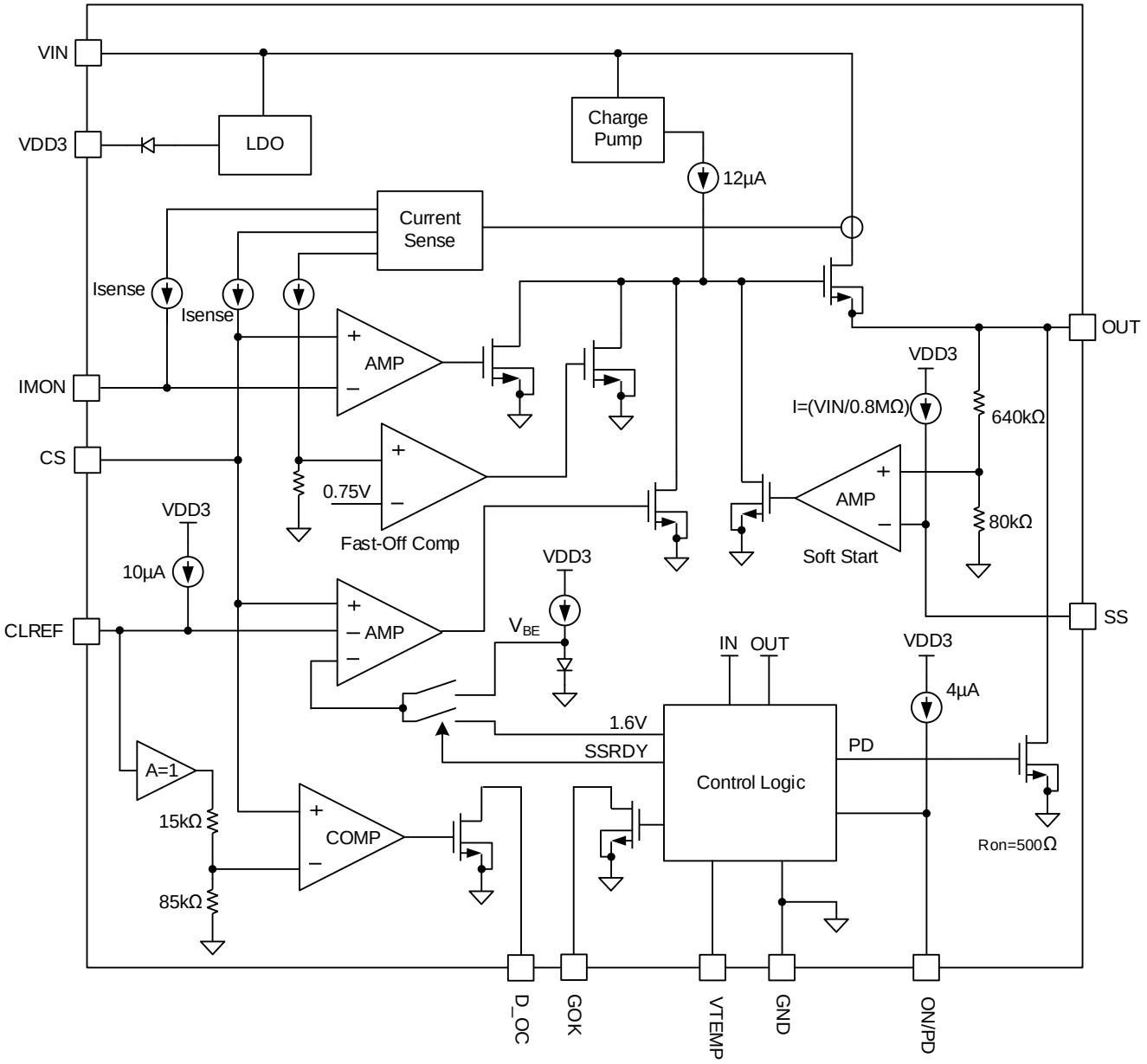


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

OPERATION

The MP5921 is a monolithic, high-side MOSFET with 1mΩ $R_{DS(ON)}$ ideally suited for multi-fuse hot-swap applications. The MP5921 can work in standalone operation or can be controlled by a hot-swap controller for multi-fuse operation. The MP5921 drives up to 50A of continuous current per device at room temperature and can reach 60A with air flow.

The MP5921 limits inrush current to the load when a circuit card is inserted into a live backplane power source, limiting the backplane's voltage drop. The MP5921 provides an integrated solution to monitor the output current and die temperature, eliminating the need for an external current-sense power resistor, power MOSFET, and thermal sense device. It also provides monitored current and temperature information feedback to the processor or controller. The MP5921 limits the internal MOSFET current by controlling the gate voltage through the current-limit reference input and soft-start ramp.

Current Limit at Start-Up

The MP5921 load current is limited by the current limit reference input and the CS external resistor. The CS voltage (V_{SC}) is compared with the current limit reference through an amplifier to regulate the power FET gate voltage. This prevents the Intelli-Fuse current from exceeding the current-limit reference-defined current limit. The current-limit reference voltage is set through CLREF and clamped low internally during soft start to allow a controlled and gradual ramp up of V_{OUT}. Once V_{OUT} is ramped close to VIN, the current limit reference can be raised to the full current limit level set by the CLREF voltage. The power FET gate is fully enhanced, and the e-fuse is ready to deliver full power from the input.

To protect the MP5921 from overheating during start-up, the current limit reference signal has an internal maximum clamp that depends on VIN and V_{OUT} (see Figure 2). When V_{OUT} < 80%VIN, the current limit reference is clamped to V_{BE} (around 635mV with a negative temperature coefficient). When V_{OUT} ≥ 80%VIN, the maximum current limit reference voltage is clamped to 1.6V.

If the external CLREF voltage is lower than the clamp voltage (V_{CLREF_CLAMP}), the actual current limit reference voltage is determined by the CLREF voltage.

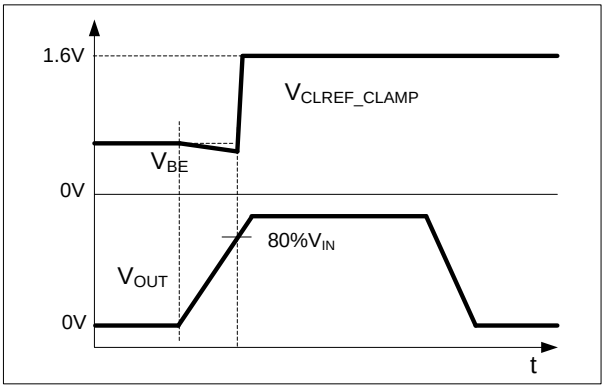


Figure 2: CLREF Clamp According to V_{OUT}

The desired start-up current limit (I_{LIMIT_SS}) is a function of the CS resistor (R_{CS}), start-up current sense gain, and CLREF voltage (V_{CLREF_SS}). The value of the current sense gain at start-up is slightly higher than when the power FET is fully on.

The V_{OUT} power-up ramp time can be estimated approximately with Equation (1):

$$t_{RAMP} = \frac{V_{IN}}{(I_{LIMIT_SS} - I_{LOAD})} \cdot C_{OUT} \quad (1)$$

The V_{OUT} ramp time varies with the load condition and the output capacitor (C_{OUT}) while adopting the CLREF current limit during start-up.

During start-up, once V_{CS} exceeds V_{CLREF_SS}, the power FET gate voltage is regulated to hold the FET current constant. If the power FET remains on while V_{OUT} remains lower than 90%VIN within the 270ms maximum soft-start time, the power FET is shut down when the 270ms time ends. If the value of V_{CLREF_SS} is higher, the power FET start-up instantaneous loss would be huge, triggering the thermal shutdown threshold (143°C) before the 270ms time ends and driving GOK low (see Figure 3).

During start-up, if V_{OUT} is lower than 1/8*VIN and the power FET current is regulated by V_{BE} for 2.1ms, the power FET is turned off as a faulty latched condition, and GOK is pulled low.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

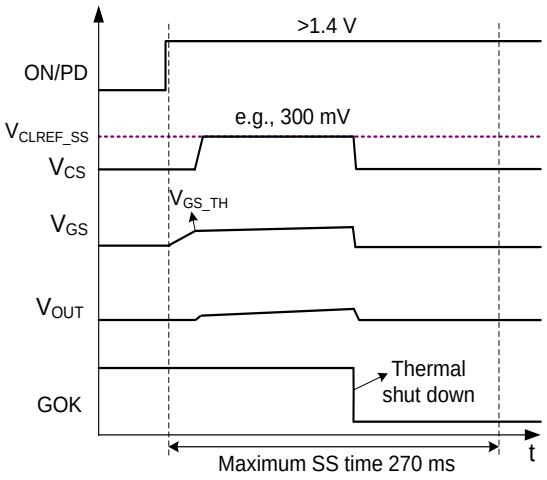


Figure 3: Failed Start-Up within 270ms

Current Limit at Normal Operation

When the output voltage has ramped up close to VIN, and V_{OUT} is higher than 80%VIN, the internal current limit reference clamp voltage is released to 1.6V, and the power FET gate voltage is close to the internal charge pump voltage. Once the MP5921 detects that the start-up has finished, the part works in normal operation.

During normal operation, once V_{CS} (which is programmed by an external resistor) exceeds the normal CLREF threshold, the internal circuit regulates the gate voltage to hold the power FET constant. To limit the current, the gate to the source voltage needs to be regulated from 3.3V to around 1V. The typical response time is about 14µs. The output current may have a small overshoot during this time period.

When the current limit is triggered, the internal fault timer starts. If the output current falls below the current limit threshold before the end of the 180µs fault time-out period, the MP5921 resumes normal operation. Otherwise, if the current limit duration exceeds the fault time-out period, the power FET is latched off and GOK is pulled low.

The desired current limit at normal operation is a function of the CS external resistor (R_{CS}).

The MP5921 current limit value can be higher than the normal maximum load current, allowing tolerances in the current sense value. The current limit can be set using Equation (2):

$$I_{LIMIT} = \frac{V_{CLREF_NORM}}{g_{CS} \cdot R_{CS}} \quad (2)$$

Where V_{CLREF_NORM} is the CLREF voltage in normal operation, and g_{CS} is 10µA/A, which is the current sense gain when the power FET is fully on. The FET works in the linear region.

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold significantly before the hot-swap control loop can respond. If the Intelli-Fuse current reaches 100A, a fast turn-off circuit in the Intelli-Fuse is activated to turn off the power FET. The total short-circuit response time is about 200ns. The GOK signal is pulled low when the power FET current reaches 100A current limit and asserts low.

Power-Up Sequence

For hot-swap applications, while the input voltage rises immediately, the power FET gate voltage should always be pulled low during the VIN plug-in with high dV/dt.

There are two operation modes for the MP5921: controlled by a hot-swap controller or standalone.

If MP5921 is controlled by a hot-swap controller, the power FET remains off until the ON/PD signal is pulled high. When the ON/PD signal becomes high and the insertion delay time ends, the power FET is charged up by the internal 12µA charge pump. Once the MP5921 power FET voltage (V_{GS}) reaches its threshold (V_{GSTH}), the output voltage rises (see Figure 4). The maximum V_{CS} is clamped to V_{CLREF_SS} if the load current is high.

If the ON/PD signal stays high from the hot-swap controller, the MP5921 can also be turned on or off through the input voltage.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

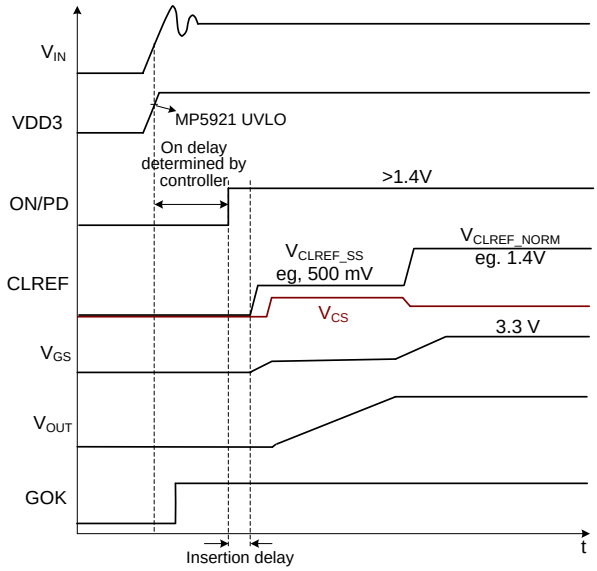


Figure 4: Start-Up when MP5921 is Controlled by Hot-Swap Controller

If the MP5921 works in standalone mode, an external capacitor (C_{ON}) can be connected from ON/PD to ground for an automatic start-up (see Figure 5). The internal 4.2μA current source charges the capacitor when VDD3 is higher than the UVLO. ON/PD can also be pulled up externally to the VDD3 voltage. A 10μA CLREF current source determines the current limit level through a resistor to ground.

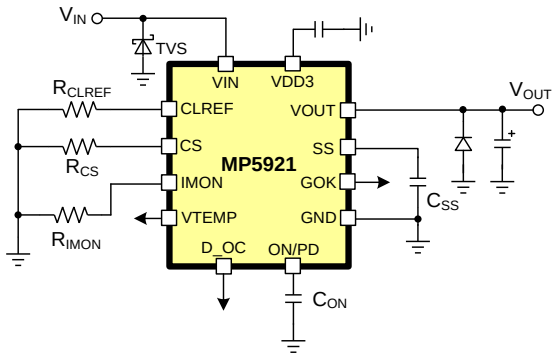


Figure 5: MP5921 Schematic when Operating in Standalone Mode

Once the ON/PD voltage exceeds 1.4V and the insertion delay time ends, the power FET is charged up by the internal 12μA charge pump. The power FET is turned on when V_{GS} reaches V_{GSTH}, and then the output voltage rises. The current-limit reference voltage is clamped internally to different voltage levels according to V_{OUT}. The external CLREF voltage is higher than the internal V_{BE} clamp (see Figure 6).

If the external CLREF voltage is lower than the clamp voltage, the actual current limit reference is determined by the CLREF voltage.

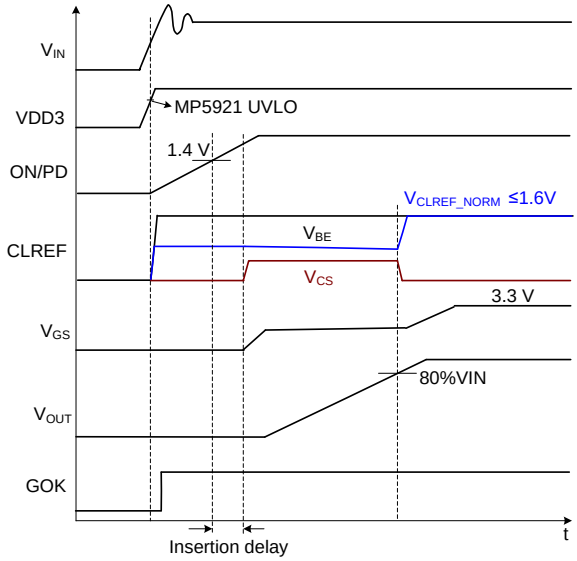


Figure 6: Start-Up when MP5921 Operates in Standalone Mode

Soft Start (SS)

A capacitor connected to SS determines the soft-start time. When ON/PD is pulled high and the insertion delay time ends, a constant current source proportional to the input voltage charges up the SS voltage. The output voltage rises at a similar slew rate to the SS voltage.

The SS capacitor value can be calculated by Equation (3):

$$C_{SS} = \frac{9 \cdot t_{SS}}{R_{SS}} \quad (3)$$

Where t_{SS} is the soft start time (ms), C_{SS} is the soft-start capacitor (nF), and R_{SS} is 0.8MΩ.

For example, a 100nF capacitor provides a soft-start time of 8.9ms. If the load capacitance is extremely large, the current required to maintain the preset soft-start time exceeds the start-up current limit. In this case, the rise time is controlled by the load capacitor and the start-up current limit. Float SS to generate a fast ramp-up voltage. A 12μA current source pulls up the gate of the power FET. The gate charge current controls the output voltage rise time.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

The approximate soft-start time is then 1.5ms, which is the minimum output voltage soft-start time.

ON/PD Control

ON/PD can be used for on/off control of the power FET and the pull-down mode of the output voltage. When ON/PD is used for on/off control, the power FET is turned on if the ON/PD voltage is higher than 1.4V. Once the ON/PD voltage is lower than 1.2V, the power FET is turned off. If ON/PD is used for V_{OUT} pull-down mode, the ON/PD voltage must be clamped at around 1V for more than 80µs. The MP5921 recognizes 0.8V < ON/PD < 1.2V as a special state that requires V_{OUT} to be pulled down.

If ON/PD is used to turn on the power FET, there is a fixed 1.3ms insertion delay after VDD3 and VIN pass the UVLO threshold. All fault functionality is operative during the insertion delay, so the GOK signal is pulled high if no fault is detected or remains low if a fault is detected. The power FET remains off until the insertion delay time ends. At the end of the insertion delay, ON/PD behaves normally to turn on the power FET if no fault occurs. The detail logic is shown in Figure 7 when GOK is pulled up to the VDD3 voltage.

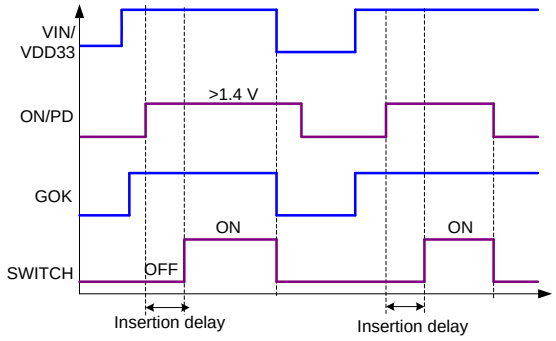


Figure 7: Power FET On/Off Control when No Fault Occurs

Once the ON/PD voltage is pulled above 1.4V and the insertion delay ends, the internal 12µA current source charges the power FET's gate. Once the gate voltage reaches its threshold (V_{GSTH}), the output voltage rises. The output voltage rises following the CLREF-controlled current limit or SS slew rate and output capacitor.

If the MP5921 works in standalone mode, a capacitor on ON/PD can be used for automatic start-up by the internal 4.2µA pull-up current source. Once the ON/PD voltage reaches its turn-on threshold, the power FET gate is charged by the internal 12µA charge pump.

When the ON/PD voltage is set to around 1V, the MP5921 works in pull-down mode (see Figure 8). In pull-down mode, when the power FET is turned off, an integrated 500Ω pull-down resistor attached to the output discharges the output voltage after a fixed delay time (2.1ms). If the ON/PD signal is pulled low directly, pull-down mode is disabled, and the Intelli-Fuse output voltage is discharged through the external load.

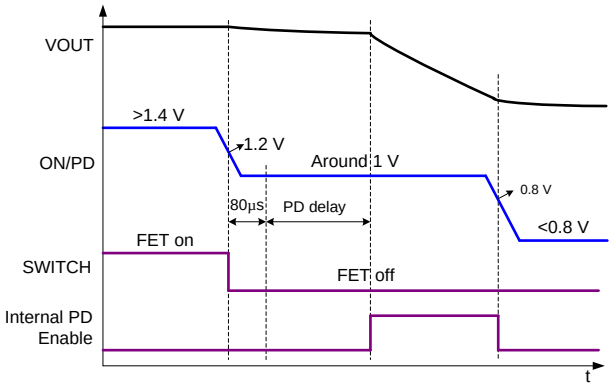


Figure 8: V_{OUT} PD Mode

If the MP5921 is controlled by the hot-swap controller, to achieve power FET on/off control and V_{OUT} PD mode control, the ON/PD can be connected as shown in Figure 9. Pull ON/PD up to VDD3 through a resistor divider (R_{PD} and R_{ON}) from the controller. If ON/PD is set to around 1V when the hot-swap controller outputs low to turn off the power FET. R_{PD} can be calculated with Equation (4):

$$R_{PD} = \frac{2 \cdot R_{ON}(\Omega)}{1 - 4.2\mu \cdot N \cdot R_{ON}(\Omega)} \quad (4)$$

Where N is the active parallel number. Choose R_{ON} to be 10kΩ. For example, if N is 2, then R_{PD} can be set to around 22kΩ.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

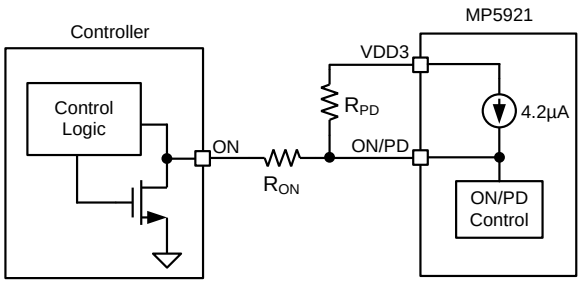


Figure 9: ON/PD Connection for PD Mode

If the ON/PD is controlled by the hot-swap controller and PD mode is unnecessary, remove R_{PD} and connect ON/PD to the hot-swap controller with a 10kΩ resistor.

GOK Report

GOK is an open-drain, active-low signal that reports the fault of the Intelli-Fuse. When a fault occurs, GOK is pulled low. Pull GOK up to the VDD3 voltage through a 100kΩ resistor. During VDD3 power-up, the GOK output is driven low. Before the power FET is turned on, the GOK fault condition is detected when VDD3 and VIN have passed the UVLO threshold. ON/PD is higher than 1.4V, so the GOK signal is pulled high if no fault is detected or is pulled low if a fault is detected.

There are four fault latch protections for the MP5921.

1. Over-current protection: When V_{CS} exceeds the CLREF threshold during normal operation, the GOK signal is pulled low after a 180µs gate regulation time.
2. Short-circuit protection: When the Intelli-Fuse load current reaches 100A rapidly, GOK is pulled low immediately.
3. Over-temperature protection: Once the junction temperature (T_J) is higher than 143°C, GOK is pulled down.
4. Power FET not fully on indication: After the FET is enabled and V_{OUT} begins ramping, if V_{OUT} < 90%VIN for the maximum soft-start time (270ms), GOK is driven low. If V_{OUT} < 1/8VIN, and the FET current is regulated by V_{BE} for 2.1ms, GOK is driven low.

When a latch fault occurs, GOK is pulled low. The GOK fault latch can be released by recycling VIN.

The MP5921 can detect a power FET drain-to-source short before the FET is turned on. If a short is detected, GOK is driven low. Once the short is removed, GOK is released high again.

Figure 10 shows the power FET on/off control with the GOK timing diagram when the MP5921 is controlled by the hot-swap controller.

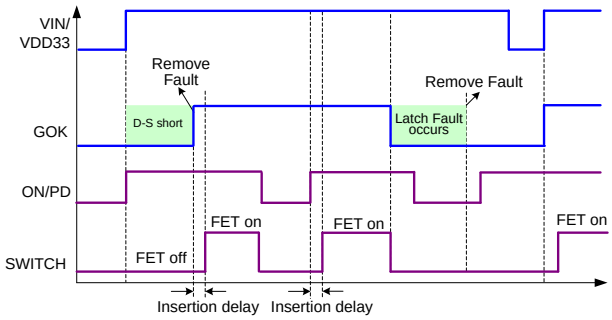


Figure 10: Power FET On/Off Control when a Fault Occurs

Damaged Intelli-Fuse MOSFET Detection

The MP5921 can detect a shorted pass FET during power-up. Once VDD3 is higher than the UVLO rising threshold, and ON/PD is higher than the 1.4V FET on threshold, the MP5921 detects a shorted pass FET by treating an output voltage that exceeds 90%VIN before the FET turns on as a short on the MOSFET. The GOK signal remains low when the MP5921 detects V_{OUT} > 90%*VIN during start-up. Once the short is removed, and the MP5921 detects that V_{OUT} < 70%*VIN, the GOK signal is released high again, and the MP5921 prepares for normal start-up.

D_OC Report

D_OC is an open-drain, active-low output that reports the over-current warning when V_{OUT} ≥ 90%VIN. Once V_{CS} is higher than 85% of the CLREF voltage, D_OC is driven low. When V_{CS} drops below the threshold, D_OC is released high again. Pull D_OC up to the VDD3 voltage through a 100kΩ resistor.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Input and Output Transient Protection

The hot-swap system experiences positive transients on the input during a hot plug or rapid turn-off with high current due to parasitic inductance in the input circuit. For input transient protection, a transient voltage suppressor (TVS) diode may be required on the input to limit transient voltages below the absolute maximum ratings.

The output may experience negative transients during rapid turn off with high current due to inductance in the output circuit. If a transient makes OUT more negative, the power FET may not turn off properly.

An output voltage clamp diode is required on the output to limit negative transients. Select a Schottky diode with a low forward voltage.

Current Sense Output (CS)

CS provides a current proportional to the output current (the current through the power device). The gain of the current sense is 10μA/A when the power FET is fully on. There is a resistor (R_{CS}) connected on CS to form an external voltage. Determine a proper reference voltage with Equation (5) and Equation (6):

$$I_{CS} = I_{OUT}*10\mu A/A \quad (5)$$

$$V_{CS} = I_{CS}*R_{CS} \quad (6)$$

Once V_{CS} reaches the CLREF current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant.

Current Monitor Output (IMON)

The gain of the current monitor is 10μA/A. There is a resistor (R_{IMON}) connected from IMON to ground. The IMON voltage range of 0V to 1.6V is required to keep IMON's output current linearly proportional to the output current. Determine a proper reference voltage with Equation (7) and Equation (8):

$$I_{MON} = I_{OUT}*10\mu A/A \quad (7)$$

$$V_{IMON} = I_{MON}*R_{IMON} \quad (8)$$

The MP5921 current monitor output can be used by the controller to accurately monitor the output current. Place a 100nF capacitor from IMON to GND to smooth the indicator voltage.

Connect a 2kΩ resistor (R_{IMON}) to ground to set the gain of the output, which is about 20mV per ampere. For the best accuracy, use resistors within 1%.

Current Balance for Parallel Operation

Multiple MP5921 devices can be used in parallel for higher current applications. The current balance loop in the MP5921 is used to balance the start-up current per active channel. All IMON pins must be connected together.

The sensed current from each active MP5921 IMON is summed together and divided by the number of active channels. The resulting average load current provides a measure of the total load current. The MP5921 current balance is achieved by comparing the sensed current of CS in each MP5921 to the average current to make an appropriate adjustment to the power FET gate voltage of each Intelli-Fuse during start-up. The equivalent average IMON resistor can be calculated by R_{CS}/N, where N is the number of active MP5921 devices.

Start-up current balance is essential in achieving the thermal advantage of paralleling operation. With good current balance, the power loss is dissipated equally over multiple devices and a greater area.

Temperature Sense Output (VTEMP)

VTEMP reports the junction temperature when there is no thermal gradient on the IC. VTEMP is a voltage output proportional to the junction temperature whenever VDD3 is higher than its UVLO threshold and the MP5921 is in active mode. The VTEMP output voltage is 8.7 mV/°C with a 152.5mV offset and can be calculated with Equation (9):

$$V_{TEMP} = T_{JUNCTION}*8.7mV+152.5mV \quad (9)$$

For example, if the junction temperature is 100°C, the VTEMP voltage is about 1.022V. If VTEMP is 0V, the junction temperature is about -18°C. The total temperature sense range is -18°C to 140°C. When the junction temperature is below -18°C, VTEMP remains at 0V.

In multi-fuse operation, the VTEMP pins of each Intelli-Fuse can be connected to the temperature monitor pin of the controller (see Figure 11).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

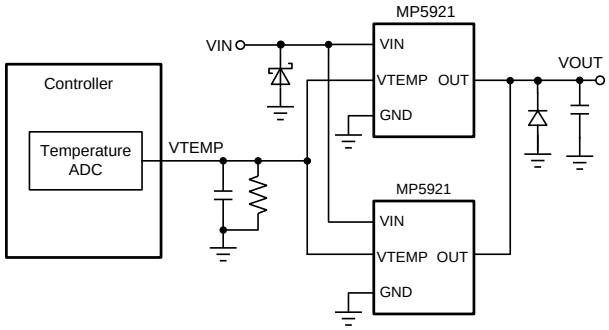


Figure 11: Multi-Fuse Temperature Sense Utilization in Paralleling

Thermal Protection

The Intelli-Fuse temperature is sensed by internally monitoring the junction temperature of the IC. The temperature information can be read from VTEMP.

The Intelli-Fuse has thermal protection. When the junction temperature exceeds the threshold (143°C), the power FET is turned off, and GOK is pulled low.

VDD3 Sub-Regulator

The MP5921 has an internal 3.0V linear sub-regulator that steps down the input voltage to generate a 3.0V power supply. VDD3 can be driven with an external 3.3V to reduce sub-regulator loss from VIN.

Under-Voltage Lockout (UVLO) Protection

The MP5921 has two under-voltage lockout (UVLO) protections: a 2.41V VDD3 UVLO and a 2.91V VIN UVLO. The MP5921 can start up only when both VDD3 and VIN exceed their respective UVLO thresholds. The MP5921 shuts down when either the VDD3 voltage is lower than the UVLO falling threshold voltage (typically 2.04V) or VIN is lower than the VIN falling threshold (2.58V). Both UVLO protections are non-latch off.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

APPLICATION INFORMATION

Current Limit Resistor (R_{CS})

The MP5921's normal current limit value should be higher than the normal maximum load current, allowing the tolerances in the current sense value. The current limit can be set with Equation (10):

$$I_{LIMIT} = \frac{V_{CLREF_NORM}}{R_{CS}} \times 10^5 (A) \quad (10)$$

Where V_{CLREF_NORM} is the CLREF voltage when the power FET works in linear mode, and R_{CS} is the resistor from CS to ground (Ω).

If R_{CS} is set to 3kΩ, and V_{CLREF_NORM} is 1.2V, the desired current limit is around 40A. When V_{CLREF_NORM} is 0.3V, the desired current limit is about 10A.

Note that the maximum CS resistor (R_{CS}) should be set no higher than 3.6kΩ.

CLREF

CLREF is used to set the current-limit reference voltage, which can be determined by the hot-swap controller or a resistor to ground in standalone operation. A CLREF 10μA current source sets the pin voltage. Place a 1nF capacitor from CLREF to ground to smooth the indicator voltage if the MP5921 is in standalone mode.

For the current limit at normal operation, the CLREF voltage can be set from 0.3V to 1.6V to program the current limit low or high while a fixed R_{CS} resistor is used.

Current Monitor Set (IMON)

The MP5921 provides a power MOSFET current monitoring function. Place a resistor to ground to set the gain of the output current.

In a single MP5921 application, the IMON resistor should be set no lower than the CS resistor. When the MP5921 is used in a multi-fuse parallel application, achieve start-up current balance per device by connecting IMON and CS (see Figure 12). The equivalent average IMON resistor (R_{IMON_AVG}) can be calculated by R_{CS}/N, where N is the active parallel number.

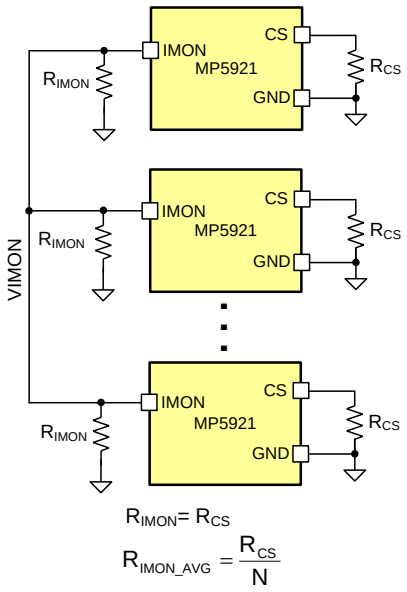


Figure 12: Multi-MP5921 IMON and CS Connection in Parallel Application

Maximum Output Current

The MP5921 drives up to 50A of continuous current per device at room temperature and can reach 60A with air flow. The case temperature rise vs. the output current at different air conditions is shown in Figure 13.

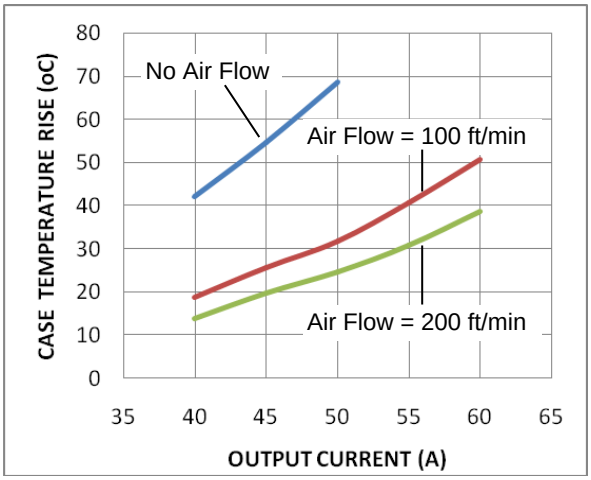


Figure 13: Output Current De-Rating Curve

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PCB Layout Guidelines

Efficient PCB layout is critical for optimum IC performance. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 14 and follow the guidelines below.

1. Place the MP5921 close to the board's input connector to minimize trace inductance.
2. Place a small capacitor (C_{IN}, 100nF) close to the MP5921's VIN and GND to minimize transients, which may occur on the input supply line.
   Transients of several volts can occur easily when the load current is shut off.
3. Place a 1µF capacitor as close to VDD3 as possible.
4. Keep the high-current path from the board's input to the load (and the return path) close to each other and in parallel to minimize loop inductance.
5. An analog signal ground (AGND) plane is used locally in the MP5921 and connected to the PCB power ground planes at a single point.
6. Connect the reference ground of all signal pins to the reference ground of the controller if the MP5921 cooperates with the hot-swap controller.

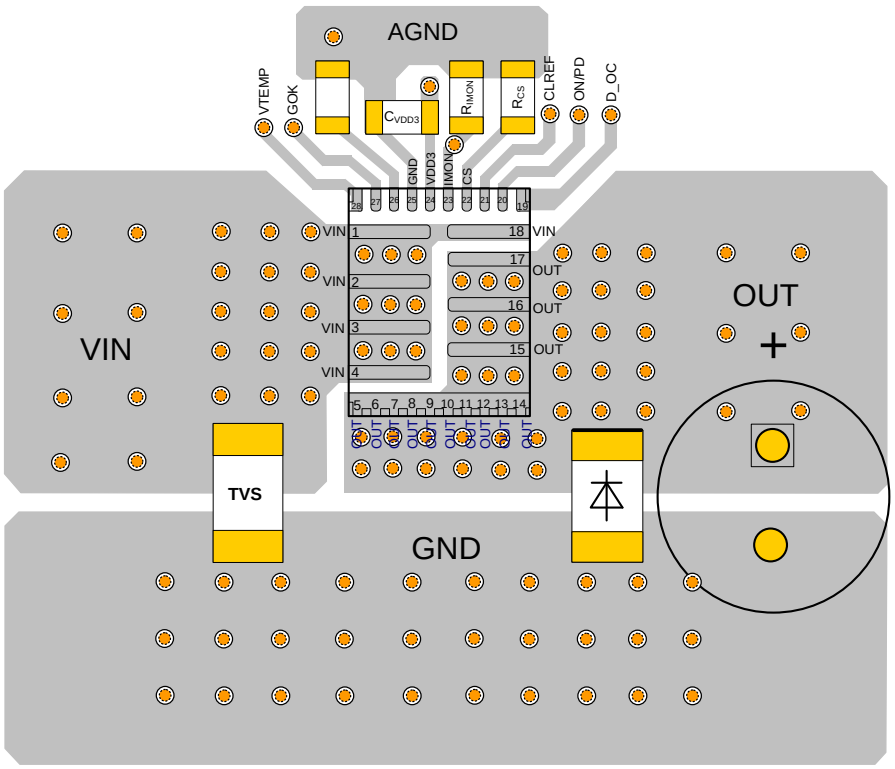
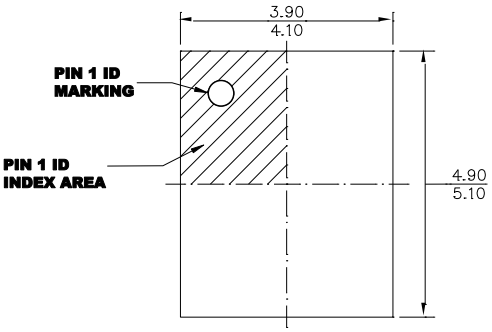


Figure 14: Example of PCB Layout (Placement & Top Layer PCB)
VIN TVS: SMDJ12A
VOUT DIODE: MBRA340T3G for Single MP5921, MBRS540T3G for Paralleling Operation

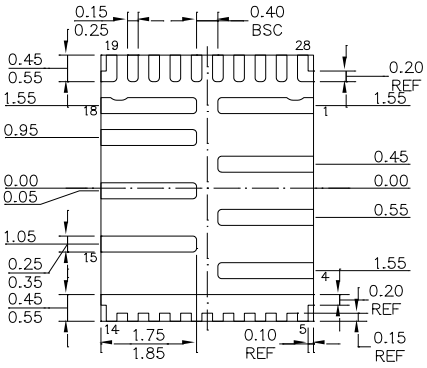
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PACKAGE INFORMATION

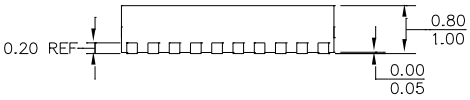
FCQFN-28 (4mmx5mm)



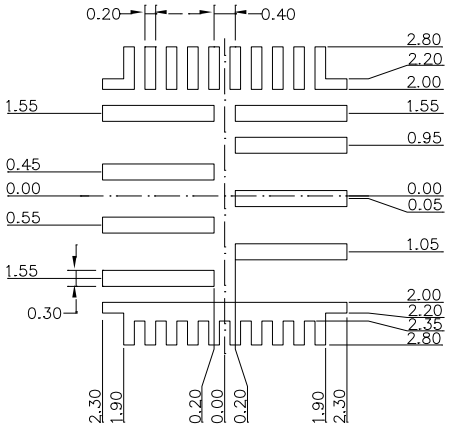
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1~4 AND PIN15-18 HAVE THE SAME SHAPE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/7/2017	Initial Release	-
1.01	10/30/2017	Updated Current-Sense Output from “-2 to 2” to “-2.5 to 2.5”	6
		Updated TPC Safe Operating Area test conditions	10
1.1	5/17/2022	Minor formatting updates	All
		Updated Quality Assurance notice	1
		Updated CLREF over-current regulation time max value from “240μs” to “265μs”	6
		Updated the R_{SS} value in Figure 1 from “0.923MΩ” to “0.8MΩ”	15
		Updated the R_{SS} value in the Soft Start (SS) section from “0.923MΩ” to “0.8MΩ”	18

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.