**S40FC008**

# 8GB, 3.3 V, e.MMC Flash

## Features

- **e.MMC 5.1 Specification Compatible**
  - Backward compatible with previous e.MMC specifications
- **Operating Voltage**
  - $V_{CCQ}$: 1.7V - 1.95V
  - $V_{CC}$: 2.7V - 3.6V
- **Density: 4 / 8 / 16 GB of Data Storage**
- **Data Bus Width:**
  - SDR Mode: 1 bit, 4 bit, 8 bit
  - DDR Mode: 4 bit, 8 bit
  - HS200 Mode: 4 bit, 8 bit
  - HS400 Mode: 8 bit
- **Clock Frequency: 52 MHz, 200 MHz**
  - SDR Mode: up to 52 MHz
  - DDR Mode: up to 52 MHz
  - HS200 Mode: up to 200 MHz
  - HS400 Mode: up to 200 MHz
- **BGA Packages**
  - 153-ball VFBGA — 11.5 mm x 13 mm x 0.8 mm
- **Operating Temperature Range**
  - Industrial (–40°C to + 85°C)
  - Industrial Extended (–40°C to + 105°C)
  - Automotive (–40°C to + 85°C)
  - Automotive Extended (–40°C to + 105°C)

## Key Supported Features

- **HS400, HS200**
- **Boot Feature/ Boot Partition**
- **Partitioning, RPMB, RPMB Throughput Improve**
- **HPI, BKOPS, BKOP Operation Control**
- **Sanitize, Discard, Trim, Erase**
- **Lock/Unlock**
- **High Priority Interrupt**
- **Secure Removal Type**
- **Configurable Drive Strength**
- **Write protect, Secure Write Protection**
- **Cache, Cache Barrier, Cache Flushing Report**
- **Reliable Write**
- **Hardware/ Software Reset**
- **Health Monitoring**
- **Field Firmware Update**
- **PON, Sleep/Awake**
- **Packed CMD, CMD Queuing**
- **Data Strobe Pin, Enhanced Data Strobe**
- **Production State Awareness**

# Performance and Power Consumption (Temperature = 25°C)

### Table 1 MLC Partition Sequential Performance

| Condition [1] | Typ. Values (MB/s) |
|---|---|
| | 8GB |
| Write | 68 |
| Read | 278 |

Note:
*1. Bus in x8 I/O, HS400 mode. Sequential Access of 1MB chunk*

### Table 2 MLC Partition Random Performance

| Condition [2] | Typ. Values (IOPS) | |
|---|---|---|
| | 8GB | |
| | Burst | Sustained |
| Write (Cache On) | 17588 | 16280 |
| Write (Cache Off) | 2284 | 2145 |
| Read | N/A | 6290 |

Note:
*2: Bus in x8 I/O, HS400 mode. Random Access of 4KB chunk over 1GB span*

### Table 3 Power Consumption

| eMMC | | | | RMS | | Idle | | Sleep | |
|---|---|---|---|---|---|---|---|---|---|
| Density | Speed | VCC/VCCQ | Operation | ICC(mA) | ICCQ(mA) | ICC(uA) | ICCQ(uA) | ICC(uA) | ICCQ(uA) |
| 8GB | SDR52 | 3.6/1.95 | Read | 24 | 95 | 110 | 470 | 100 | 450 |
| | | | Write | 32 | 76 | | | | |
| | DDR52 | 3.6/1.95 | Read | 42 | 123 | | | | |
| | | | Write | 45 | 74 | | | | |
| | HS200 | 3.6/1.95 | Read | 80 | 121 | | | | |
| | | | Write | 59 | 84 | | | | |
| | HS400 | 3.6/1.95 | Read | 111 | 144 | | | | |
| | | | Write | 59 | 82 | | | | |

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# 1. General Description

SkyHigh e.MMC is a managed NAND memory solution designed for embedded applications. SkyHigh e.MMC includes a flash controller and a standard MLC NAND flash memory, and is compatible with the JEDEC JESD84-B51 with backwards compatibility to previous e.MMC specifications.

Designed for faster throughput and large data transfer, SkyHigh e.MMC offers high performance, great reliability, and minimal latency. In addition to higher performance, SkyHigh's e.MMC offers optimum power management features resulting in reduced power consumption, making it an ideal solution for mobile applications.

In addition, highly optimized SkyHigh firmware fully utilizes the MLC NAND capabilities leveraging wear-leveling, defect management, garbage collection, and ECC to enhance product life.

The SkyHigh e.MMC product family offers a vast array of the JEDEC e.MMC features including HS200, HS400, high priority interrupt
(HPI), boot partitions, RPMB partitions, background operations, hardware reset, and power off notification.

Combined with an advanced e.MMC feature set and SkyHigh's commitment to quality, SkyHigh e.MMC is ideal for industrial applications as well as set top boxes, gaming consoles, and consumer electronic devices.

# 2. SkyHigh Product Offering

The SkyHigh e.MMC product offering includes: 4/8/16 GB in 153-FBGA (11.5 mm x 13 mm) packages.

- 8 GB: S40FC008
  - 153 VFBGA (11.5 x 13 x 0.8, 0.5 mm ball pitch)

# 3. Package Configurations

**Figure 3.1** FBGA 153 (Top View, Balls Down)

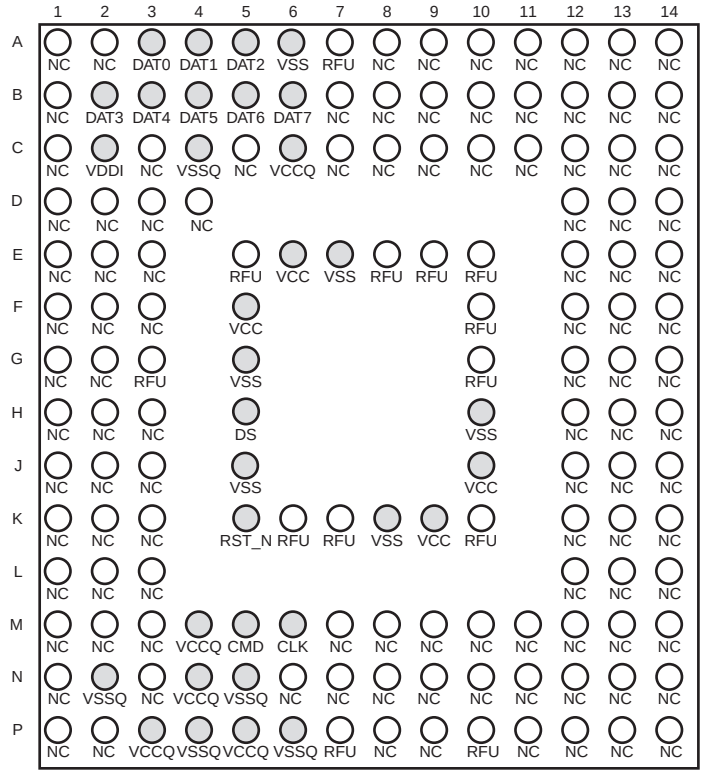


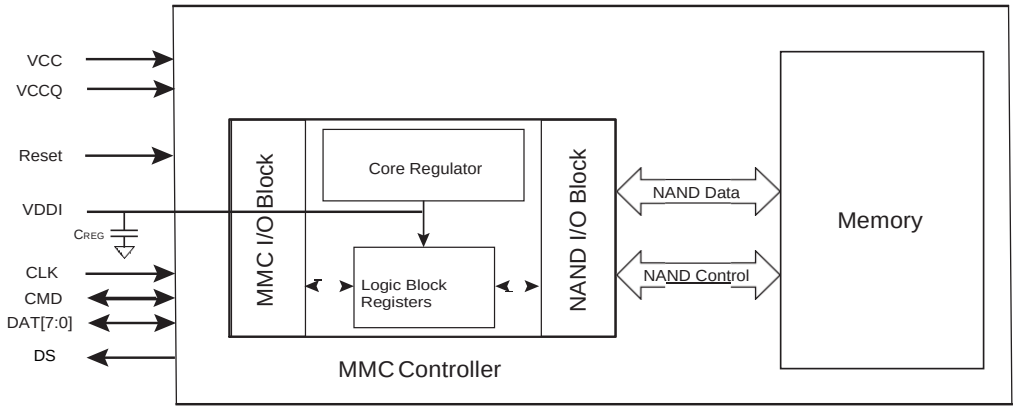
**Table 3.1 Pin Description**

| Pin Name | Type | Description |
|---|---|---|
| DAT0 - DAT7 | I/O | Bidirectional data channels used for data transfers. |
| CMD | I/O | Bidirectional command channel used for device initialization and command transfers. |
| CLK | Input | Clock input. |
| RST_N | Input | Hardware reset. |
| VCC | Power | Supply voltage for the flash memory. |
| VCCQ | Power | Supply voltage for the memory controller and MMC interface. |
| VDDI | Power | Internal power node. Connect capacitor to ground. |
| VSS | Power | Ground pin for the flash memory. |
| VSSQ | Power | Ground pin for the memory controller and MMC interface. |
| DS | Output | Data strobe. |
| NC | — | Not connected. |
| RFU | — | Reserved for future use. Do not connect. |

# 4. Architecture

SkyHigh e.MMC is an embedded non-volatile storage solution with a MultiMediaCard (MMC) interface, a high performance memory controller, and state of the art flash memory all supported by SkyHigh optimized flash management software. Based on the JEDEC industry-standard MMC System Specification v5.1, the SkyHigh e.MMC product family is offered in standard JEDEC BGA packages. Figure 4.1 represents the basic block diagram of the SkyHigh e.MMC.

**Figure 4.1** SkyHigh e.MMC Architecture




# 5. Key Supported e.MMC Features

SkyHigh e.MMC supports the JEDEC JESD84-B51 specification.

## 5.1 Boot Operation

SkyHigh e.MMC supports boot mode as well as alternate boot mode. Boot operations can be performed at high speed and dual data rate timings.

**Figure 5.1** MultiMediaCard State Diagram (Boot Mode)

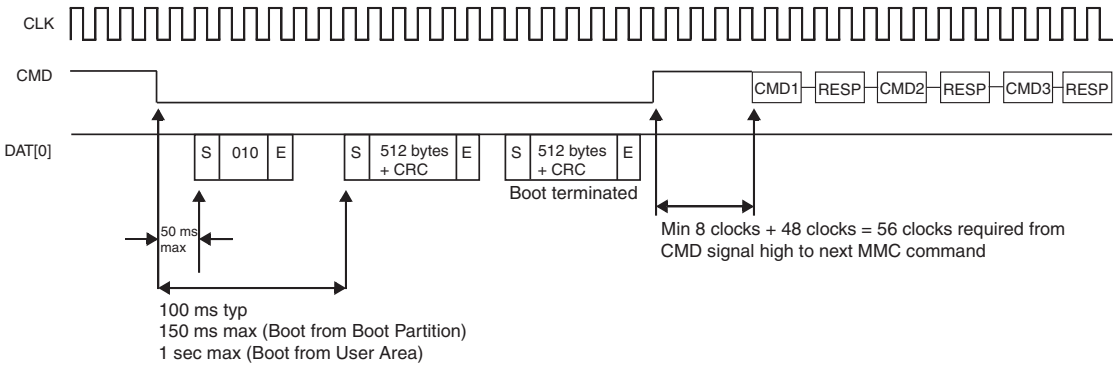
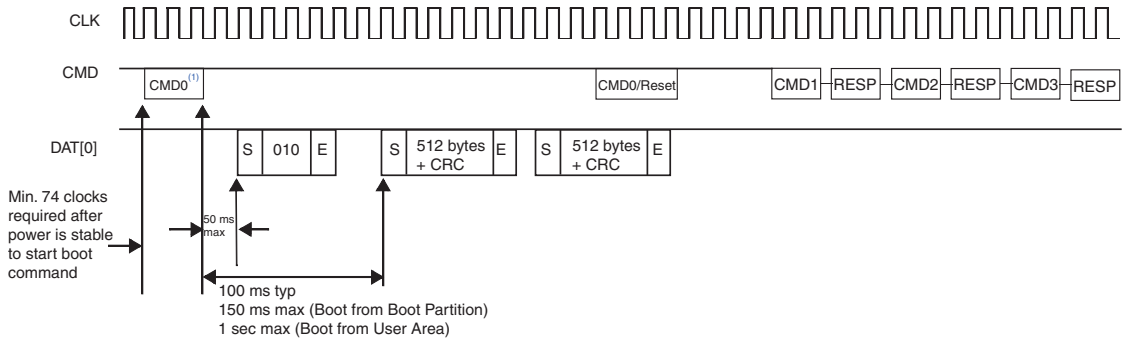


**Figure 5.2** MultiMediaCard State Diagram (Alternative Boot Mode)




***Note:***
*1. CMD0 with argument 0xFFFFFFFA.*

## 5.2 Partition Management

e.MMC specifications allow for the device to have the following partitions: a User Data Area for general purpose storage, two boot partitions for storing boot images, and the Replay Protected Memory Block (RPMB) for data management in a replay protected and authenticated manner.

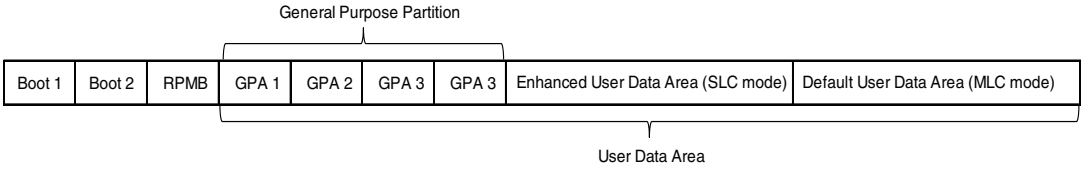
The SkyHigh e.MMC device can be configured as below:

- Factory configuration supplies two boot partitions size of 4 MB each and one RPMB partition size of 4 MB. These partitions are configured in Enhanced (SLC) mode for higher reliability.
- The host can create up to four General Purpose Partitions within the User Data Area. These partitions can be configured in Enhanced (SLC) mode or Default (MLC) mode. The host will also need to configure the size of each partition. These attributes can be programmed by the host only once in the device life-cycle (one-time programmable).
- In addition to the General Purpose Partitions the host can also configure a segment of the User Data Area to be accessed in Enhanced (SLC) mode. The host will need to specify the starting location and size. These attributes can be programmed by the host only once in the device life-cycle (one-time programmable).

**Table 5.1 Partition Type**

| Partition | | NAND Mode |
|---|---|---|
| Boot Area 1 | | SLC Mode |
| Boot Area 2 | | SLC Mode |
| RPMB Area | | SLC Mode |
| User Data Area | General Purpose Partition | MLC or SLC Mode |
| | Enhanced | SLC Mode |
| | Default | MLC Mode |

**Figure 5.3** Partitions



## 5.3 Sleep (CMD5)

Sleep/Awake (CMD5) is used to switch the device between Sleep and Standby mode. During the Sleep state, $V_{CC}$ can be switched off for maximum power savings. While a device is in Sleep mode it can only respond to the Reset (CMD0) and Sleep/Awake (CMD5) commands.

## 5.4 High Priority Interrupt (HPI)

High Priority Interrupt (HPI) is intended to suspend an ongoing operation while allowing for a high priority read operation to be performed.

## 5.5 Background Operations

e.MMC devices are equipped with a Background Operations feature. When enabled, BackgroundOperations allow the e.MMC device to perform a number of routine data maintenance operations such as wear leveling, garbage collection, erase, and compaction while the host CPU is not being serviced.

## 5.6 Auto Background Operations

Auto Background Operations is a feature that allows the e.MMC device to fully manage background operations without any requirements from the Host. The e.MMC device will check if background operations are required at specified intervals and initiate background operations if needed. This frees the host from having to develop software to manage these maintenance tasks and ensure that the e.MMC device is operating at the optimum performance levels. Issuing any command while auto background operations are occurring will stop the current background operation activities. There will be a maximum latency of 40 ms if auto background operations are interrupted by any read or write command from the host.

## 5.7 Trim

Similar to the Erase operation, the Trim function performs a targeted erase on specific write blocks. Data that is no longer needed, designated by the host, will be erased during background erase events.

## 5.8 Sanitize

Sanitize is intended for applications with high security requirements that can afford the performance impact.This command is used in conjunction with standard Erase or Trim operations and requires the device to physically remove data from the unmapped user address space. The busy line will be asserted once the Sanitize operations begin and will remain busy until the operation has been completed or interrupted.

## 5.9 Hardware Reset

Used by the host to reset the device, hardware reset moves the device into a pre-idle state and disables the power-on period write protection on blocks that were set at power-on as write protected.

## 5.10 Health Monitoring

Health Monitoring is a proprietary feature of the SkyHigh e.MMC product that provides useful information about the life span of the NAND flash component. The host can query for the device's health by using the CMD60 command to get information such as the number of bad blocks and the number of erase cycles for each block. EXT_CSD registers [269:254] also contain valuable device health information. A separate application note is available with the full details of the CMD60 command and EXT_CSD registers [269:254]. A non-disclosure agreement (NDA) is required to view this application note. Contact your nearest SkyHigh sales office for more information.

## 5.11 Field Firmware Update

Field Firmware Update is a feature that allows the host to upload a new version of the firmware to the e.MMC. This can be done by setting the device into FFU mode and performing writes with the arguments defined in the FFU_ARG register. A separate application note is available with the full details of this feature. A non-disclosure agreement (NDA) is required to view this application note. Contact your nearest SkyHigh sales office for more information.

# 6. Register Values

## 6.1 OCR Register

Operation Conditions Register (OCR) stores the e.MMC voltage profile. In addition, it contains the status bit (31) which is set when the device power up has been completed.

**Table 6.1 OCR Register**

| Field Description | OCR Slice | Value |
|---|---|---|
| Reserved | [6:0] | 00 00000b |
| $V_{CCQ}$: 1.7 - 1.95 range | [7] | Dual Voltage: 1b |
| $V_{CCQ}$: 2.0 - 2.6 range | [14:8] | 000 0000b |
| $V_{CCQ}$: 2.7 - 3.6 range | [23:15] | 1 1111 1111b |
| Reserved | [28:24] | 0 0000b |
| Access Mode | [30:29] | Sector Mode: 10b |
| e.MMC power up status bit (busy) (1) | [31] | — |

***Notes:***

1. *Bit 31 is set to LOW if device is not finished with the power up routine.*
2. *The voltage for internal flash memory ($V_{CC}$) should be 2.7V - 3.6V regardless of OCR Register value.*

## 6.2 CID Register

The Card Identification Register (CID) contains the card identification information used during the card identification phase.

**Table 6.2 CID Register**

| Field Name | Field ID | Width | CID slice | CID Value |
|---|---|---|---|---|
| Manufacturer ID | MID | 8 | [127:120] | 01h |
| Card BGA | CBX | 2 | [113:112] | 01b |
| OEM/Application ID | OID | 8 | [111:104] | 00h |
| Product Name | PNM | 48 | [103:56] | See product table |
| Product Revision | PRV | 8 | [55:48] | (Note3) |
| Product Serial Number | PSN | 32 | [47:16] | 32-bit unsigned binary integer assigned at random |
| Manufacturing Date | MDT | 8 | [15:8] | (Note 1) |
| CRC7 Checksum | CRC | 7 | [7:1] | (Note 2) |
| Not Used | — | 1 | [0] | Always 1 |

***Notes:***

*1. Descriptions follow JEDEC e.MMC Standard Specifications.*
*2. The CRC7 checksum (7 bits). This is the checksum of the CID contents computed according to 0.*
*3. Product Revision is a combination of Controller and Firmware Revisions.*

## 6.3 Product Table

**Table 6.3 Product Table**

| SkyHigh Part Number | Density | Product Name in CID Register (PNM) |
|---|---|---|
| S40FC008 | 8 GB | “S40008” – 533430303038h |

## 6.4 Card Specific Data Register

Card Specific Data (CSD) Register contains the e.MMC access information. It includes data format, error correction, transfer speeds, and access times. It also includes information as to whether the DSR register can be accessed.

**Table 6. CSD Register**

| Field Name | Field ID | Size (Bits) | Cell Type | CSD Slice | CSD Value |
|---|---|---|---|---|---|
| CSD Structure | CSD_STRUCTURE | 2 | R | [127:126] | 3h |
| System Specification Version | SPEC_VERS | 4 | R | [125:122] | 4h |
| Reserved[1] | — | 2 | R | [121:120] | — |
| Data Read Access Time 1 | TAAC | 8 | R | [119:112] | 27h |
| Data Read Access Time 2 in CLK cycles (NSAC*100) | NSAC | 8 | R | [111:104] | 01h |
| Maximum Bus Clock Frequency | TRAN_SPEED | 8 | R | [103:96] | 32h |
| Device Command Classes | CCC | 12 | R | [95:84] | 0F5h |
| Maximum Read Block Length | READ_BL_LEN | 4 | R | [83:80] | 9h |
| Partial Blocks For Read Allowed | READ_BL_PARTIAL | 1 | R | [79:79] | 0h |
| Write Block Misalignment | WRITE_BLK_MISALIGN | 1 | R | [78:78] | 0h |
| Read Block Misalignment | READ_BLK_MISALIGN | 1 | R | [77:77] | 0h |
| DSR Implemented | DSR_IMP | 1 | R | [76:76] | 0h |
| Reserved[1] | — | 2 | R | [75:74] | — |
| Device Size | *C_SIZE | 12 | R | [73:62] | FFFh |
| Maximum Read Current at $V_{DD}$ min | VDD_R_CURR_MIN | 3 | R | [61:59] | 7h |
| Maximum Read Current at $V_{DD}$ max | VDD_R_CURR_MAX | 3 | R | [58:56] | 7h |
| Maximum Write Current at $V_{DD}$ min | VDD_W_CURR_MIN | 3 | R | [55:53] | 7h |
| Maximum Write Current at $V_{DD}$ max | VDD_W_CURR_MAX | 3 | R | [52:50] | 7h |
| Device Size Multiplier | C_SIZE_MULT | 3 | R | [49:47] | 7h |
| Erase Group Size | ERASE_GRP_SIZE | 5 | R | [46:42] | 1Fh |
| Erase Group Size Multiplier | ERASE_GRP_MULT | 5 | R | [41:37] | 1Fh |
| Write Protect Group Size | WP_GRP_SIZE | 5 | R | [36:32] | 0Fh |
| Write Protect Group Enable | WP_GRP_ENABLE | 1 | R | [31:31] | 1h |
| Manufacturer Default | DEFAULT_ECC | 2 | R | [30:29] | 0h |
| Write Speed Factor | R2W_FACTOR | 3 | R | [28:26] | 2h |
| Maximum Write Data Block Length | WRITE_BL_LEN | 4 | R | [25:22] | 9h |
| Partial Blocks For Write Allowed | WRITE_BL_PARTIAL | 1 | R | [21:21] | 0h |
| Reserved[1] | — | 4 | R | [20:17] | — |
| Content Protection Application | CONTENT_PROT_APP | 1 | R | [16:16] | 0h |
| File Format Group | FILE_FORMAT_GRP | 1 | R/W | [15:15] | 0h |
| Copy Flag (OTP) | COPY | 1 | R/W | [14:14] | 1h |
| Permanent Write Protection | PERM_WRITE_PROTECT | 1 | R/W | [13:13] | 0h |

**Notes**

1. Reserved bits should be read at '0'.
2. R = Read only. R/W = One time programmable and readable. R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
3. $V_{DD}$ represents the total consumed current for $V_{CC}$ and $V_{CCQ}$.

**Table 6. CSD Register** (Continued)

| Field Name | Field ID | Size (Bits) | Cell Type | CSD Slice | CSD Value |
|---|---|---|---|---|---|
| Temporary Write Protection | TMP_WRITE_PROTECT | 1 | R/W/E | [12:12] | 0h |
| File Format | FILE_FORMAT | 2 | R/W | [11:10] | 0h |
| ECC Code | ECC | 2 | R/W/E | [9:8] | 0h |
| Calculated CRC | CRC | 7 | R/W/E | [7:1] | NOTE 4 |
| Not Used | — | 1 | — | [0] | Always 1 |

**Notes**
1. Reserved bits should be read at '0'.
2. R = Read only. R/W = One time programmable and readable. R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
3. $V_{DD}$ represents the total consumed current for $V_{CC}$ and $V_{CCQ}$.
4. The CRC field carries the check sum for the CSD contents. It is computed according to 0. The checksum has to be recalculated by the host for any CSD modification. The default corresponds to the initial CSD contents.

## 6.5 Extended CSD Register (EXT_CSD)

The Extended CSD Register defines the e.MMC selected modes and properties. It is 512 bytes long. The most significant 320 bytes, also know as Properties segment, define the e.MMC capabilities and cannot be modified by the host. The remaining 192 bytes define e.MMC operating modes and can be modified by the host via a Switch command.

**Table 7. Extended CSD Register (EXT_CSD)**

| Field Name | Field ID | Size (Bytes) | Cell Type | EXT_CSD Slice | Value |
|---|---|---|---|---|---|
| Reserved[5] | — | 6 | — | [511:506] | — |
| Extended Security Commands Error | EXT_SECURITY_ERR | 1 | R | [505] | 00h |
| Supported Command Sets | S_CMD_SET | 1 | R | [504] | 01h |
| HPI Features | HPI_FEATURES | 1 | R | [503] | 01h |
| Background Operations Support | BKOPS_SUPPORT | 1 | R | [502] | 01h |
| Max Packed Read Commands | MAX_PACKED_READS | 1 | R | [501] | 20h |
| Max Packed Write Commands | MAX_PACKED_WRITES | 1 | R | [500] | 20h |
| Data Tag Support | DATA_TAG_SUPPORT | 1 | R | [499] | 01h |
| Tag Unit Size | TAG_UNIT_SIZE | 1 | R | [498] | 00h |
| Tag Resources Size | TAG_RES_SIZE | 1 | R | [497] | 00h |
| Context Management Capabilities | CONTEXT_CAPABILITIES | 1 | R | [496] | 78h |
| Large Unit Size | LARGE_UNIT_SIZE_M1 | 1 | R | [495] | 01h |
| Extended Partitions Attribute Support | EXT_SUPPORT | 1 | R | [494] | 03h |
| Supported Modes | SUPPORTED_MODES | 1 | R | [493] | 01h |
| FFU Features | FFU_FEATURES | 1 | R | [492] | 00h |
| Operation Codes Timeout | OPERATION_CODE_TIMEOUT | 1 | R | [491] | 17h |

**Notes**
5. Reserved bits should be read at 0, unless otherwise specified.
6. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
7. Set to 0 after power up and can be changed via a Switch command.
8. R = Read only.
   R/W = One time programmable and readable.
   R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
   R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
   W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
9. Value depends on state of the device.
10. Value depends on the firmware that the device is loaded with.

**Table 7. Extended CSD Register (EXT_CSD)** (Continued)

| Field Name | Field ID | Size (Bytes) | Cell Type | EXT_CSD Slice | Value |
|---|---|---|---|---|---|
| FFU Argument | FFU_ARG | 4 | R | [490:487] | FFFAFFF0h |
| Barrier support | BARRIER_ SUPPORT | 1 | R | 486 | 1h |
| Reserved[5] | | 181 | — | [485:309] | — |
| CMD Queuing Support | CMDQ_ SUPPORT | 1 | R | 308 | 1h |
| CMD Queuing Depth | CMDQ_ DEPTH | 1 | R | 307 | 1Fh |
| Reserved[5] | | 1 | — | 306 | — |
| Number of FW Sectors Correctly Programmed | NUMBER_OF_FW_SECTORS_ CORRECTLY_PROGRAMMED | 4 | R | [305:302] | 0000h |
| Vendor proprietary health report[11] | VENDOR_PROPRIETARY_HEALTH_ REPORT | 32 | R | [301:270] | N/A |
| Device Life Time Estimation Type B | DEVICE_LIFE_TIME_EST_TYP_B | 1 | R | [269] | 01h |
| Device Life Time Estimation Type A | DEVICE_LIFE_TIME_EST_TYP_A | 1 | R | [268] | 01h |
| Pre-EOL Information[9] | PRE_EOL_INFO | 1 | R | [267] | 01h |
| Optimal Read Size | OPTIMAL_READ_SIZE | 1 | R | [266] | 40h |
| Optimal Write Size | OPTIMAL_WRITE_SIZE | 1 | R | [265] | 40h |
| Optimal Trim Unit Size | OPTIMAL_TRIM_UNIT_SIZE | 1 | R | [264] | 07h |
| Device Version | DEVICE_VERSION | 2 | R | [263:262] | 3805h |
| Firmware Version[10] | FIRMWARE_VERSION | 8 | R | [261:254] | — |
| Power class for 200MHz, DDR at VCC= 3.6V | PWR_CL_DDR_200_360 | 1 | R | [253] | 00h |
| Cache Size | CACHE_SIZE | 4 | R | [252:249] | 0400h |
| Generic CMD6 Timeout | GENERIC_CMD6_TIME | 1 | R | [248] | 05h |
| Power Off Notification (Long) Timeout | POWER_OFF_LONG_TIME | 1 | R | [247] | 64h |
| Background Operations Status | BKOPS_STATUS | 1 | R | [246] | 00h |
| Number Of Correctly Programmed Sectors | CORRECTLY_PRG_SECTORS_NU M | 4 | R | [245:242] | 0000h |
| 1st Initialization Time after Partitioning | INI_TIMEOUT_PA | 1 | R | [241] | 0Ah |
| Cache Flushing Policy | CACHE_FLUSH_POLICY | 1 | R | [240] | 01h |
| Power Class for 52 MHz, DDR at 3.6 V | PWR_CL_DDR_52_360 | 1 | R | [239] | 00h |
| Power Class for 52 MHz, DDR at 1.95 V | PWR_CL_DDR_52_195 | 1 | R | [238] | 00h |
| Power Class for 200 MHz at 1.95 V | PWR_CL_200_195 | 1 | R | [237] | 00h |
| Power Class for 200 MHz at 1.30 V | PWR_CL_200_130 | 1 | R | [236] | 00h |
| Minimum Write Performance for 8-bit at 52 MHz in DDR mode | MIN_PERF_DDR_W_8_52 | 1 | R | [235] | 00h |
| Minimum Read Performance for 8-bit at 52 MHz in DDR mode | MIN_PERF_DDR_R_8_52 | 1 | R | [234] | 00h |
| Reserved[5] | — | 1 | — | [233] | — |

**Notes**

5. Reserved bits should be read at 0, unless otherwise specified.
6. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1,the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
7. Set to 0 after power up and can be changed via a Switch command.
8. R = Read only.
   R/W = One time programmable and readable.
   R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
   R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
   W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
9. Value depends on state of the device.
10. Value depends on the firmware that the device is loaded with. ExtCSD[254] = PRV value in CID register Others are zero
11. This Fields reserved for vendor proprietary health report.

**Table 7. Extended CSD Register (EXT_CSD)** (Continued)

| Field Name | Field ID | Size (Bytes) | Cell Type | EXT_CSD Slice | Value |
|---|---|---|---|---|---|
| Trim Multiplier | TRIM_MULT | 1 | R | [232] | 02h |
| Secure Feature Support | SEC_FEATURE_SUPPORT | 1 | R | [231] | 55h |
| Secure Erase Multiplier | SEC_ERASE_MULT | 1 | R | [230] | 19h |
| Secure TRIM Multiplier | SEC_TRIM_MULT | 1 | R | [229] | 0Ah |
| Boot Information | BOOT_INFO | 1 | R | [228] | 07h |
| Reserved[5] | — | 1 | — | [227] | — |
| Boot Partition Size | BOOT_SIZE_MULTI | 1 | R | [226] | 20h |
| Access Size | ACC_SIZE | 1 | R | [225] | 06h |
| High Capacity Erase Unit Size | HC_ERASE_GRP_SIZE | 1 | R | [224] | 01h |
| High Capacity Erase Time Out | ERASE_TIMEOUT_MULT | 1 | R | [223] | 02h |
| Reliable Write Sector Count | REL_WR_SEC_C | 1 | R | [222] | 01h |
| High Capacity Write Protect Group Size | HC_WP_GRP_SIZE | 1 | R | [221] | 10h |
| Sleep Current [$V_{CC}$] | S_C_VCC | 1 | R | [220] | 07h |
| Sleep Current [$V_{CCQ}$] | S_C_VCCQ | 1 | R | [219] | 07h |
| Production State Awareness Timeout | PRODUCTION_STATE_AWARENESS_TIMEOUT | 1 | R | [218] | 17h |
| Sleep/awake Time Out | S_A_TIMEOUT | 1 | R | [217] | 12h |
| Sleep Notification Timeout | SLLEP_NOTIFICATION_TIME | 1 | R | [216] | 0Ch |
| Sector Count | SEC_COUNT | 4 | R | [215:212] | 00E90000h |
| Secure Write Protect Information | SECURE_WP_INFO | 1 | R | [211] | 01h |
| Minimum Write Performance for 8-bit at 52 MHz | MIN_PERF_W_8_52 | 1 | R | [210] | 0h |
| Minimum Read Performance for 8-bit at 52 MHz | MIN_PERF_R_8_52 | 1 | R | [209] | 0h |
| Minimum Write Performance for 4-bit at 52 MHz or 8-bit at 26 MHz | MIN_PERF_W_8_26_4_52 | 1 | R | [208] | 0h |
| Minimum Read Performance for 4-bit at 52 MHz or 8-bit at 26 MHz | MIN_PERF_R_8_26_4_52 | 1 | R | [207] | 0h |
| Minimum Write Performance for 4-bit at 26 MHz | MIN_PERF_W_4_26 | 1 | R | [206] | 0h |

**Notes**

5. Reserved bits should be read at 0, unless otherwise specified.
6. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
7. Set to 0 after power up and can be changed via a Switch command.
8. R = Read only.
   R/W = One time programmable and readable.
   R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
   R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
   W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
9. Value depends on state of the device.
10. Value depends on the firmware that the device is loaded with.

**Table 7. Extended CSD Register (EXT_CSD)** (Continued)

| Field Name | Field ID | Size (Bytes) | Cell Type | EXT_CSD Slice | Value |
|---|---|---|---|---|---|
| Minimum Read Performance for 4-bit at 26 MHz | MIN_PERF_R_4_26 | 1 | R | [205] | 0h |
| Reserved[5] | — | 1 | — | [204] | — |
| Power Class for 26 MHz at 3.6 V | PWR_CL_26_360 | 1 | R | [203] | 0h |
| Power Class for 52 MHz at 3.6 V | PWR_CL_52_360 | 1 | R | [202] | 0h |
| Power Class for 26 MHz at 1.95 V | PWR_CL_26_195 | 1 | R | [201] | 0h |
| Power Class for 52 MHz at 1.95 V | PWR_CL_52_195 | 1 | R | [200] | 0h |
| Partition Switching Timing | PARTITION_SWITCH_TIME | 1 | R | [199] | 04h |
| Out-of-Interrupt Busy Timing | OUT_OF_INTERRUPT_TIME | 1 | R | [198] | 0Ah |
| I/O Driver Strength | DRIVER_STRENGTH | 1 | R | [197] | 1Fh |
| Device Type | CARD_TYPE | 1 | R | [196] | 57h |
| Reserved[5] | — | 1 | — | [195] | — |
| CSD Structure Version | CSD_STRUCTURE | 1 | R | [194] | 2h |
| Reserved[5] | — | 1 | — | [193] | — |
| Extended CSD Revision | EXT_CSD_REV | 1 | R | [192] | 8h |
| Command Set | CMD_SET | 1 | R/W/E_P | [191] | 0h |
| Reserved[5] | — | 1 | — | [190] | — |
| Command Set Revision | CMD_SET_REV | 1 | R | [189] | 0h |
| Reserved[5] | — | 1 | — | [188] | — |
| Power Class | POWER_CLASS | 1 | R/W/E_P | [187] | 0h |
| Reserved[5] | — | 1 | — | [186] | — |
| High Speed Interface Timing[6] | HS_TIMING | 1 | R/W/E_P | [185] | 0h |
| Strobe Support | STROBE_SUPPORT | 1 | R | [184] | 1h |
| Bus Width Mode[7] | BUS_WIDTH | 1 | W/E_P | [183] | 0h |
| Reserved[5] | — | 1 | — | [182] | — |
| Erased Memory Content | ERASED_MEM_CONT | 1 | R | [181] | 0h |
| Reserved[5] | — | 1 | — | [180] | — |
| Partition Configuration | PARTITION_CONFIG | 1 | R/W/E, R/W/E_P | [179] | 0h |
| Boot Config Protection | BOOT_CONFIG_PROT | 1 | R/W, R/W/C_P | [178] | 0h |
| Boot Bus Conditions | BOOT_BUS_WIDTH | 1 | R/W/E | [177] | 0h |
| Reserved[5] | — | 1 | — | [176] | — |
| High-Density Erase Group Definition | ERASE_GROUP_DEF | 1 | R/W/E_P | [175] | 0h |

**Notes**
5. Reserved bits should be read at 0, unless otherwise specified.
6. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
7. Set to 0 after power up and can be changed via a Switch command.
8. R = Read only.
   R/W = One time programmable and readable.
   R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
   R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
   W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
9. Value depends on state of the device.
10. Value depends on the firmware that the device is loaded with.

**Table 7. Extended CSD Register (EXT_CSD)** (Continued)

| Field Name | Field ID | Size (Bytes) | Cell Type | EXT_CSD Slice | Value |
|---|---|---|---|---|---|
| Boot Write Protection Status Register | BOOT_WP_STATUS | 1 | R | [174] | 0h |
| Boot Area Write Protect Register | BOOT_WP | 1 | R/W, R/W/C_P | [173] | 0h |
| Reserved[5] | — | 1 | — | [172] | — |
| User Area Write Protect Register | USER_WP | 1 | R/W, R/W/C_P, R/W/E_P | [171] | 0h |
| Reserved[5] | — | 1 | — | [170] | — |
| FW Configuration | FW_CONFIG | 1 | R/W | [169] | 0h |
| RPMB Size | RPMB_SIZE_MULT | 1 | R | [168] | 20h |
| Write Reliability Setting Register | WR_REL_SET | 1 | R/W | [167] | 1Fh |
| Write Reliability Parameter Register | WR_REL_PARAM | 1 | R | [166] | 15h |
| Start Sanitize Operation | SANITIZE_START | 1 | W/E_P | [165] | 00h |
| Manually Start Background Operations | BKOPS_START | 1 | W/E_P | [164] | 00h |
| Enable Background Operations Handshake | BKOPS_EN | 1 | R/W | [163] | 02h |
| Hardware Reset Function | RST_n_FUNCTION | 1 | R/W | [162] | 00h |
| HPI Management | HPI_MGMT | 1 | R/W/E_P | [161] | 00h |
| Partitioning Support | PARTITIONING_SUPPORT | 1 | R | [160] | 07h |
| Max Enhanced Area Size | MAX_ENH_SIZE_MULT | 3 | R | [159:157] | 0001D2h |
| Partitions Attribute | PARTITIONS_ATTRIBUTE | 1 | R/W | [156] | 00h |
| Partitioning Setting | PARTITION_SETTING_COMPLETED | 1 | R/W | [155] | 00h |
| General Purpose Partition Size | GP_SIZE_MULT | 12 | R/W | [154:143] | 00...00h |
| Enhanced User Data Area Size | ENH_SIZE_MULT | 3 | R/W | [142:140] | 000h |
| Enhanced User Data Start Address | ENH_START_ADDR | 4 | R/W | [139:136] | 0000h |
| Reserved[5] | — | 1 | — | [135] | — |
| Secure Bad Block Management | SEC_BAD_BLK_MGMNT | 1 | R/W | [134] | 00h |
| Production State Awareness | PRODUCTION_STATE_AWARENESS | 1 | R/W/E | [133] | 00h |
| Package Case Temperature is Controlled | TCASE_SUPPORT | 1 | W/E_P | [132] | 00h |
| Periodic Wakeup | PERIODIC_WAKEUP | 1 | R/W/E | [131] | 00h |
| Program CID/CSD in DDR Mode Support | PROGRAM_CID_CSD_DDR_SUPPORT | 1 | R | [130] | 01h |
| Reserved[5] | — | 2 | — | [129:128] | — |

**Notes**
5. Reserved bits should be read at 0, unless otherwise specified.
6. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
7. Set to 0 after power up and can be changed via a Switch command.
8. R = Read only.
   R/W = One time programmable and readable.
   R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
   R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
   W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
9. Value depends on state of the device.
10. Value depends on the firmware that the device is loaded with.

**Table 7. Extended CSD Register (EXT_CSD)** (Continued)

| Field Name | Field ID | Size (Bytes) | Cell Type | EXT_CSD Slice | Value |
|---|---|---|---|---|---|
| Vendor Specific Fields [12] | VENDOR_SPECIFIC_FIELD | 64 | <vendor specific> | [127:64] | N/A |
| Native Sector Size | NATIVE_SECTOR_SIZE | 1 | R | [63] | 1h |
| Sector Size Emulation | USE_NATIVE_SECTOR | 1 | R/W | [62] | 0h |
| Sector Size | DATA_SECTOR_SIZE | 1 | R | [61] | 0h |
| 1st Initialization After Disabling Sector Size Emulation | INI_TIMEOUT_EMU | 1 | R | [60] | 0Ah |
| Class 6 Command Control | CLASS_6_CTRL | 1 | R/W/E_P | [59] | 0h |
| Number Of Address Group To Be Released | DYNCAP_NEEDED | 1 | R | [58] | 0h |
| Exception Events Control | EXCEPTION_EVENTS_CTRL | 2 | R/W/E_P | [57:56] | 00h |
| Exception Events Status | EXCEPTION_EVENTS_STATUS | 2 | R | [55:54] | 00h |
| Extended Partitions Attribute | EXT_PARTITIONS_ATTRIBUTE | 2 | R/W | [53:52] | 00h |
| Context Configuration | CONTEXT_CONF | 15 | R/W/E_P | [51:37] | 00...00h |
| Packed Command Status | PACKED_COMMAND_STATUS | 1 | R | [36] | 0h |
| Packed Command Failure Index | PACKED_FAILURE_INDEX | 1 | R | [35] | 0h |
| Power Off Notification | POWER_OFF_NOTIFICATION | 1 | R/W/E_P | [34] | 0h |
| Control to Turn the Cache On/Off | CACHE_CTRL | 1 | R/W/E_P | [33] | 0h |
| Flushing of the Cache | FLUSH_CACHE | 1 | W/E_P | [32] | 0h |
| Control to turn the Barrier ON/OFF | BARRIEIR_CNTL | 1 | R/W | [31] | 0h |
| Mode Config | MODE_CONFIG | 1 | R/W/E_P | [30] | 0h |
| Mode Operation Codes | MODE_OPERATION_CODES | 1 | W/E_P | [29] | 0h |
| Reserved[5] | | 2 | — | [28:27] | — |
| FFU Status | FFU_STATUS | 1 | R | [26] | 0h |
| Pre Loading Data Size | PRE_LOADING_DATA_SIZE | 4 | R/W/E_P | [25:22] | 0000h |
| Max Pre Loading Data Size | MAX_PRE_LOADING_DATA_SIZE | 4 | R | [21:18] | 0x00E90000 |
| Production State Awareness Enablement | PRODUCT_STATE_AWARENESS_ENABLEMENT | 1 | R/W/E and R | [17] | 01h |
| Secure Removal Type | SECURE_REMOVAL_TYPE | 1 | R/W & R | [16] | 3Bh |
| Command Queue Mode Enable | CMDQ_MODE_EN | 1 | R/W/E_P | [15] | 0h |
| Reserved[5] | | 15 | — | [14:0] | — |

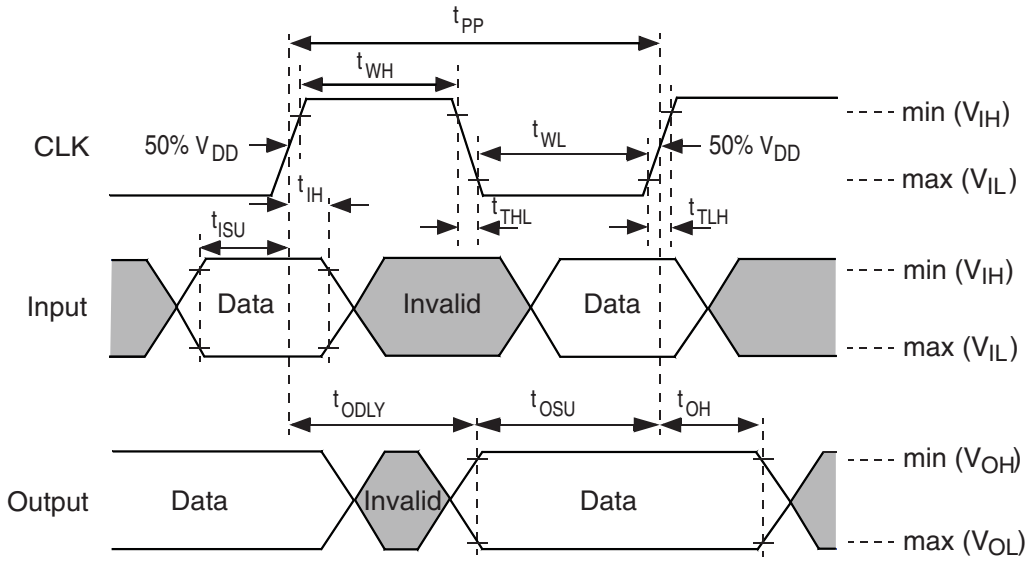
**Notes**

5. Reserved bits should be read at 0, unless otherwise specified.
6. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
7. Set to 0 after power up and can be changed via a Switch command.
8. R = Read only.
   R/W = One time programmable and readable.
   R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
   R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
   W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
9. Value depends on state of the device.
10. Value depends on the firmware that the device is loaded with.
12. These fields are reserved for definition by the device manufacturer

# 7. AC Parameter

## 7.1 Bus Timing

**Figure 7.1** Bus Timing Diagram




***Note:***
*1. Data must always be sampled on the rising edge of the clock.*

## 7.2 High Speed Timing

**Table 7.1 High Speed Timing**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK** | | | | | |
| Clock Frequency Data Transfer Mode | $f_{PP}$ | 0 | 52 | MHz | CL ≤ 30 pF<br>Tolerance: +100 kHz |
| Clock Frequency Identification Mode | $f_{OD}$ | 0 | 400 | kHz | Tolerance: +20 kHz |
| Clock Low Time | $t_{WL}$ | 6.5 | | ns | CL ≤ 30 pF |
| Clock High Time | $t_{WH}$ | 6.5 | | ns | CL ≤ 30 pF |
| Clock Rise Time | $t_{TLH}$ | | 3 | ns | CL ≤ 30 pF |
| Clock Fall Time | $t_{THL}$ | | 3 | ns | CL ≤ 30 pF |
| **Inputs CMD, DAT (referenced to CLK)** | | | | | |
| Input Set-up Time | $t_{ISU}$ | 3 | | ns | CL ≤ 30 pF |
| Input Hold Time | $t_{IH}$ | 3 | | ns | CL ≤ 30 pF |
| **Outputs CMD, DAT (referenced to CLK)** | | | | | |
| Output Delay Time During Data Transfer Mode | $t_{ODLY}$ | | 13.7 | ns | CL ≤ 30 pF |
| Output Hold Time | $t_{OH}$ | 2.5 | | | CL ≤ 30 pF |
| Signal Rise Time | $t_{RISE}$ | | 3 | ns | CL ≤ 30 pF |
| Signal Fall Time | $t_{FALL}$ | | 3 | ns | CL ≤ 30 pF |

## 7.3 Backward Compatible Timing

**Table 7.2 Backward Compatible Timing**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK** | | | | | |
| Clock Frequency Data Transfer Mode | $f_{PP}$ | 0 | 26 | MHz | CL ≤ 30 pF |
| Clock Frequency Identification Mode | $f_{OD}$ | 0 | 400 | kHz | |
| Clock Low Time | $t_{WL}$ | 10 | | ns | CL ≤ 30 pF |
| Clock High Time | $t_{WH}$ | 10 | | | |
| Clock Rise Time | $t_{TLH}$ | | 10 | ns | CL ≤ 30 pF |
| Clock Fall Time | $t_{THL}$ | | 10 | ns | CL ≤ 30 pF |
| **Inputs CMD, DAT (referenced to CLK)** | | | | | |
| Input Set-Up Time | $t_{ISU}$ | 3 | | ns | CL ≤ 30 pF |
| Input Hold Time | $t_{IH}$ | 3 | | ns | CL ≤ 30 pF |
| **Outputs CMD, DAT (referenced to CLK)** | | | | | |
| Output Hold Time | $t_{OH}$ | 8.3 | | ns | CL ≤ 30 pF |
| Output Set-up Time | $t_{OSU}$ | 11.7 | | ns | CL ≤ 30 pF |

## 7.4 DDR Interface Timing

**Figure 7.2** DDR Interface Timing

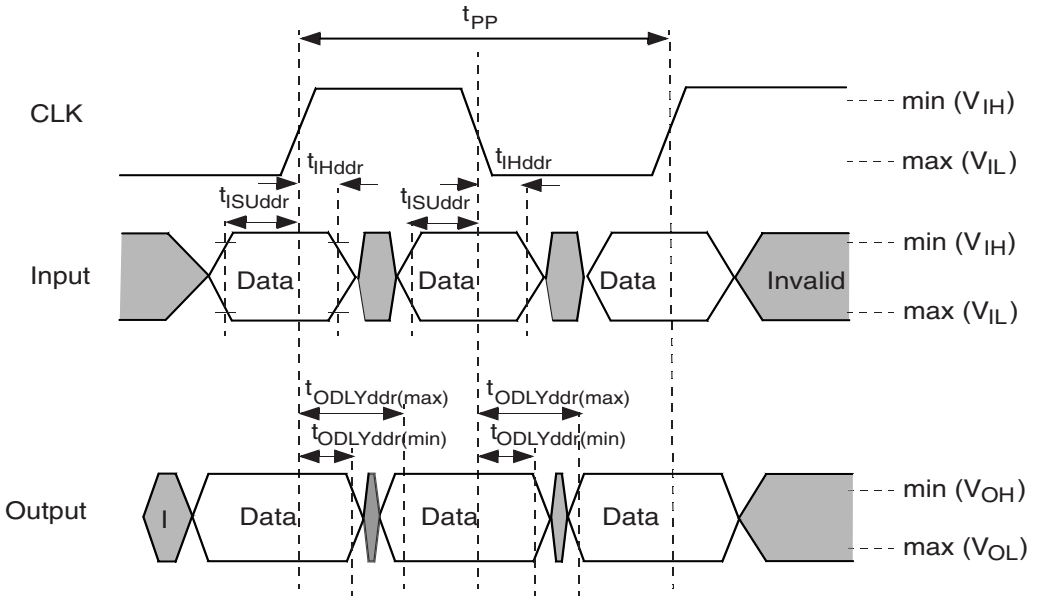



**Table 7.3 DDR Interface Timing**

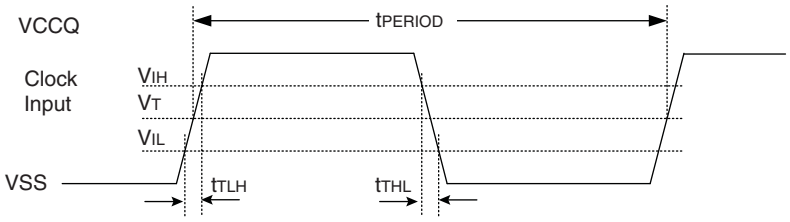
| Parameter | Symbol | Min | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Input CLK1** | | | | | |
| Clock Duty Cycle | | 45 | 55 | % | Includes jitter, phase noise |
| **Input DAT (referenced to CLK-DDR mode)** | | | | | |
| Input Set-up Time | $t_{ISUddr}$ | 2.5 | | ns | CL ≤ 20 pF |
| Input Hold Time | $t_{IHddr}$ | 2.5 | | ns | CL ≤ 20 pF |
| **Output DAT (referenced to CLK-DDR mode)** | | | | | |
| Output Delay Time During Data Transfer | $t_{ODLYddr}$ | 1.5 | 7 | ns | CL ≤ 20 pF |
| Signal Rise Time (All Signals) | $t_{RISE}$ | | 2 | ns | CL ≤ 20 pF |
| Signal Fall Time (All Signals) | $t_{FALL}$ | | 2 | ns | CL ≤ 20 pF |

## 7.5 Timing Specifications for HS200 Mode

### 7.5.1 HS200 Clock Timing

HS200 mode is available when $V_{CCQ}$ is 1.7V to 1.95V, and the clock timing should conform with the timing diagram shown in Figure 7.3. CLK input timings need to meet the clock timing across the entire range of operating environment. CLK timings must be measured while CMD and DAT signals are either high or low. HS200 supports clock frequencies of up to 200 MHz.

**Figure 7.3** HS200 Clock Signal Timing




***Notes:***

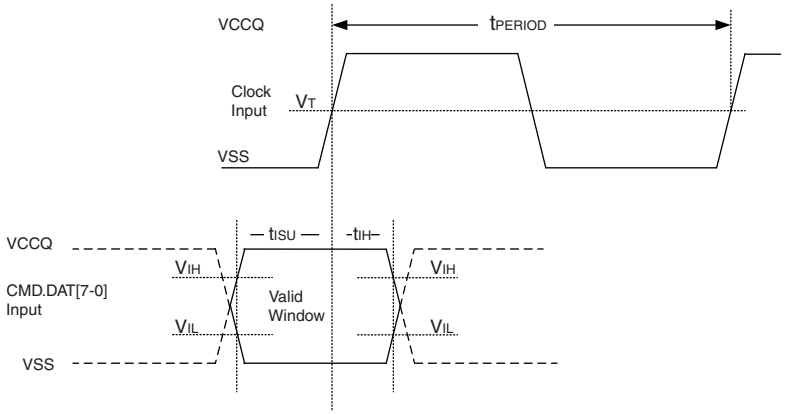
1. *$V_{IH}$ denotes $V_{IH(min.)}$, and $V_{IL}$ denotes $V_{IL(max.)}$.*
2. *$V_T$ = 0.975V, Clock Threshold ($V_{CCQ}$ = 1.8V); indicates reference points for timing measurements.*

**Table 7.4 HS200 Clock Signal Timing**

| Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|
| $t_{PERIOD}$ | 5 | — | ns | 200 MHz (max.) between rising edges. |
| $t_{TLH}$, $t_{THL}$ | — | 0.2 $t_{PERIOD}$ | ns | $t_{TLH}$, $t_{THL}$ < 1ns (max.) at 200 MHz, CBGA = 12 pF. The absolute max. value of $t_{TLH}$, $t_{TLH}$ is 10 ns regardless of clock frequency. |
| Duty Cycle | 30 | 70 | % | |

## 7.5.2 HS200 Input Timing

**Figure 7.4** HS200 Device Input Timing




***Notes:***

1. *$t_{ISU}$ and $t_{IH}$ are measured at $V_{IL(max.)}$ and $V_{IH(min.)}$.*
2. *$V_{IH}$ denotes $V_{IH(min.)}$, and $V_{IL}$ denotes $V_{IL(max.)}$.*

**Table 7.5 HS200 Device Input Timing**

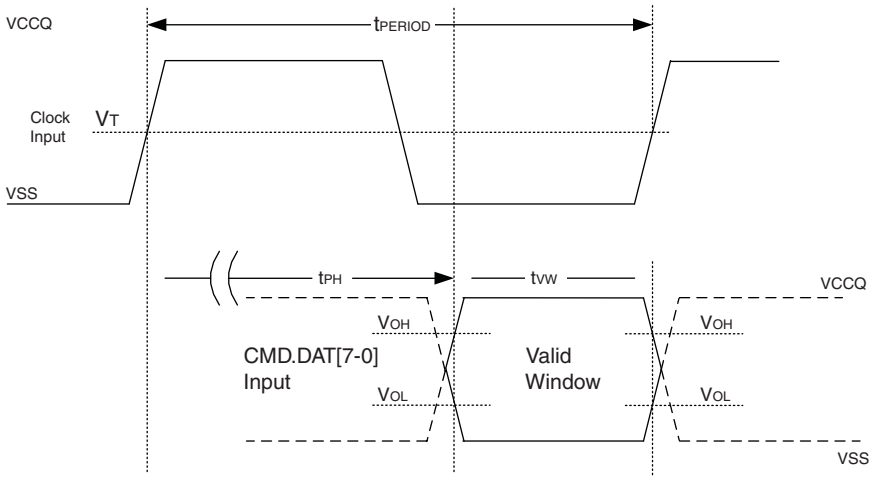
| Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|
| $t_{ISU}$ | 1.40 | — | ns | 5 pF ≤ CBGA ≤ 12 pF |
| $t_{IH}$ | 0.8 | — | ns | 5 pF ≤ CBGA ≤ 12 pF |

### 7.5.3 HS200 Output Timing

The $t_{PH}$ parameter is defined to allow device output delay to be longer than $t_{PERIOD}$. $t_{PH}$ may have random phase relation to the clock upon initialization. The Host is ultimately responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode.

The impact of a temperature drift ($\Delta_{TPH}$) has to be taken into account when setting the sampling point. Output valid data window ($t_{VW}$) is available regardless of the drift ($\Delta_{TPH}$) while the position of data window varies by the drift.

**Figure 7.5** HS200 Device Output Timing



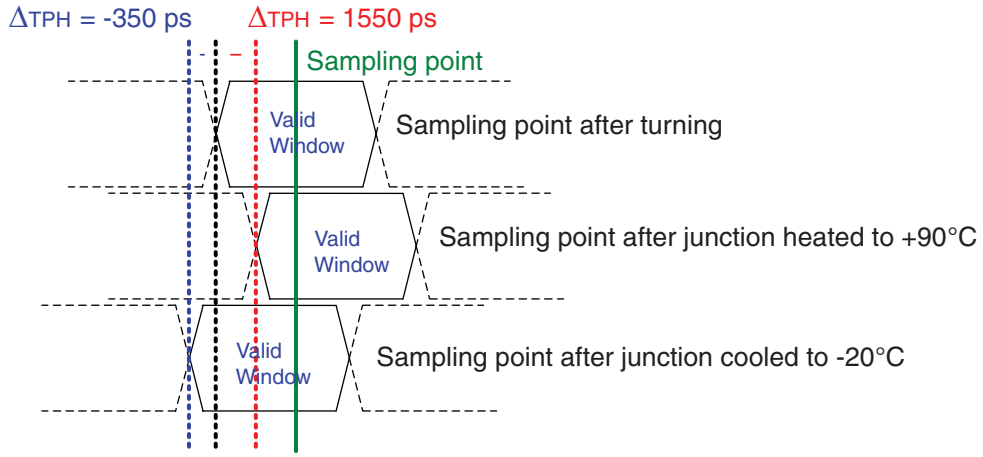

***Note:***
*1. $V_{OH}$ denotes $V_{OH(min.)}$, and $V_{OL}$ denotes $V_{OL(max.)}$.*

**Table 7.6 HS200 Device Output Timing**

| Symbol | Min. | Max. | Unit | Notes |
|---|---|---|---|---|
| $t_{PH}$ | 0 | 2 | UI | Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift. |
| $\Delta_{TPH}$ | -350 ($\Delta$T = -20°C) | +1550 ($\Delta$T = 90°C) | ps | Delay variation due to temperature change after tuning. Total allowable shift of output valid window ($t_{VW}$) from last system Tuning procedure. $\Delta_{TPH}$ is 2600 ps for $\Delta$T from -25°C to 125°C during operation. |
| $t_{VW}$ | 0.575 | — | UI | $t_{VW}$ = 2.88 ns at 200 MHz. Host path may add Signal Integrity induced noise, skews, etc. Expected $t_{VW}$ at Host input is larger than 0.475 UI. |

***Note:***
*1. Unit Interval (UI) is one-bit nominal time (i.e. UI = 5 ns at 200 MHz).*

**Figure 7.6** $\Delta_{TPH}$ Consideration




**Implementation Guide:**

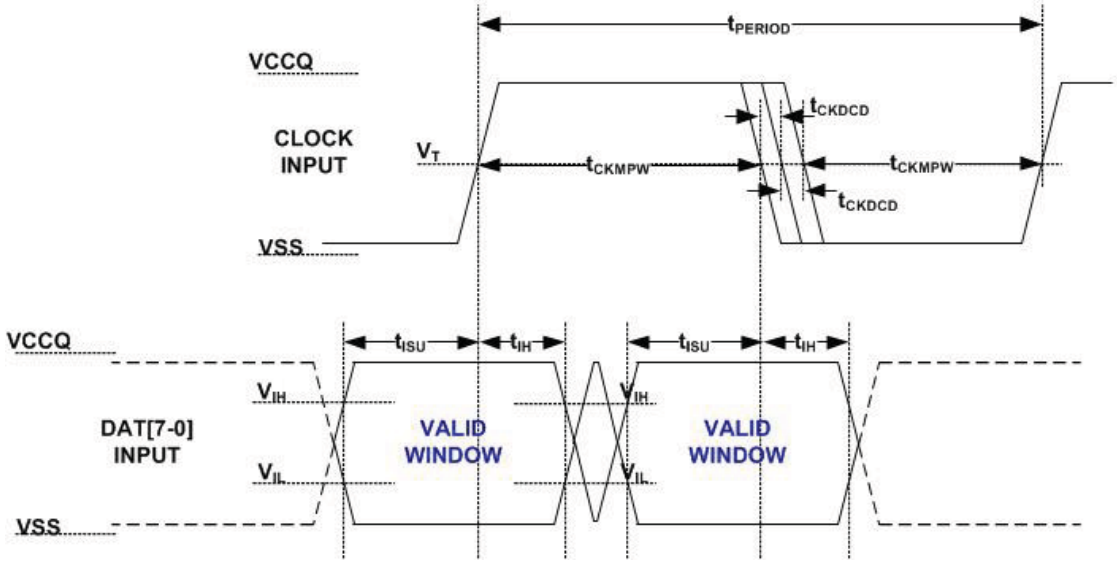
- The host should avoid sampling errors that are caused by the $\Delta_{TPH}$ drift.
- Tuning should be performed while the device wakes up after sleep.
- Reducing operating frequency can help overcome the $\Delta_{TPH}$ drift.

## 7.6 Bus Timing Specification in HS400 Mode

### 7.6.1 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.Figure 7.7 and Table 7.4 show Device input timing.

**Figure 7.7** HS400 Device Data Input Timing




***Note:***
*1. $V_T$ = 50% of $V_{CCQ}$, indicates clock reference point for timing measurements.*

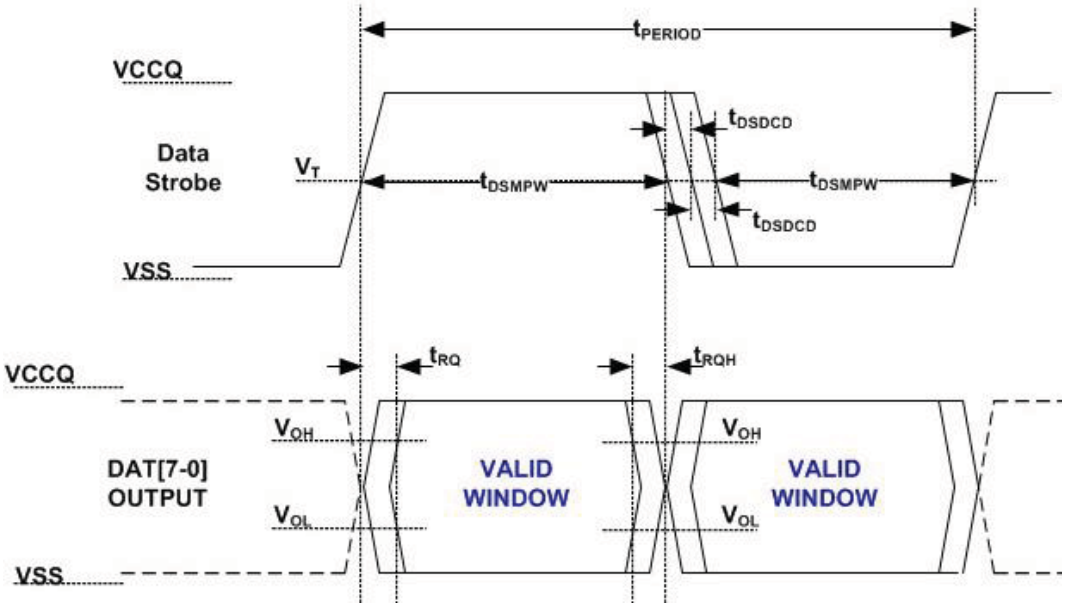
**Table 7.7** HS400 Device Input Timing

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Input CLK | | | | | |
| Cycle time data transfer mode | $t_{PERIOD}$ | 5 | | | 200 MHz (max), between rising edges With respect to $V_T$. |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{IH}/V_{IL}$. |
| Duty cycle distortion | $t_{CKDCD}$ | 0.0 | 0.3 | ns | Allowable deviation from an ideal 50% duty cycle.<br>With respect to $V_T$.<br>Includes jitter, phase noise |
| Minimum pulse width | $t_{CKMPW}$ | 2.2 | | ns | With respect to $V_T$. |
| Input DAT (referenced to CLK) | | | | | |
| Input set-up time | $t_{ISUddr}$ | 0.4 | | ns | $C_{Device} \leq 6$ pF<br>With respect to $V_{IH}/V_{IL}$. |
| Input hold time | $t_{IHddr}$ | 0.4 | | ns | $C_{Device} \leq 6$ pF<br>With respect to $V_{IH}/V_{IL}$. |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{IH}/V_{IL}$. |

## 7.6.2 HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

**Figure 7.8** HS400 Device Output Timing




***Note:***
*$V_T$ = 50% of $V_{CCQ}$, indicates clock reference point for timing measurements.*

**Table 7.8** HS400 Device Output Timing

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Data Strobe | | | | | |
| Cycle time data transfer mode | $t_{PERIOD}$ | 5 | | | 200 MHz (max), between rising edges With respect to $V_T$ |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load |
| Duty cycle distortion | $t_{DSDCD}$ | 0.0 | 0.2 | ns | Allowable deviation from the input CLKduty cycle distortion ($t_{CKDCD}$) With respect to $V_T$ Includes jitter, phase noise |
| Minimum pulse width | $t_{DSMPW}$ | 2.0 | | ns | With respect to $V_T$ |
| Read pre-amble | $t_{RPRE}$ | 0.4 | — | $t_{PERIOD}$ | Max value is specified by manufacturer. Value up to infinite is valid |
| Read post-amble | $t_{RPST}$ | 0.4 | — | $t_{PERIOD}$ | Max value is specified by manufacturer. Value up to infinite is valid |
| Output DAT (referenced to Data Strobe) | | | | | |
| Output skew | $t_{RQ}$ | | 0.4 | ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load |
| Output hold skew | $t_{RQH}$ | | 0.4 | ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load. |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load |

**Table 7.9** HS400 Capacitance and Resistors

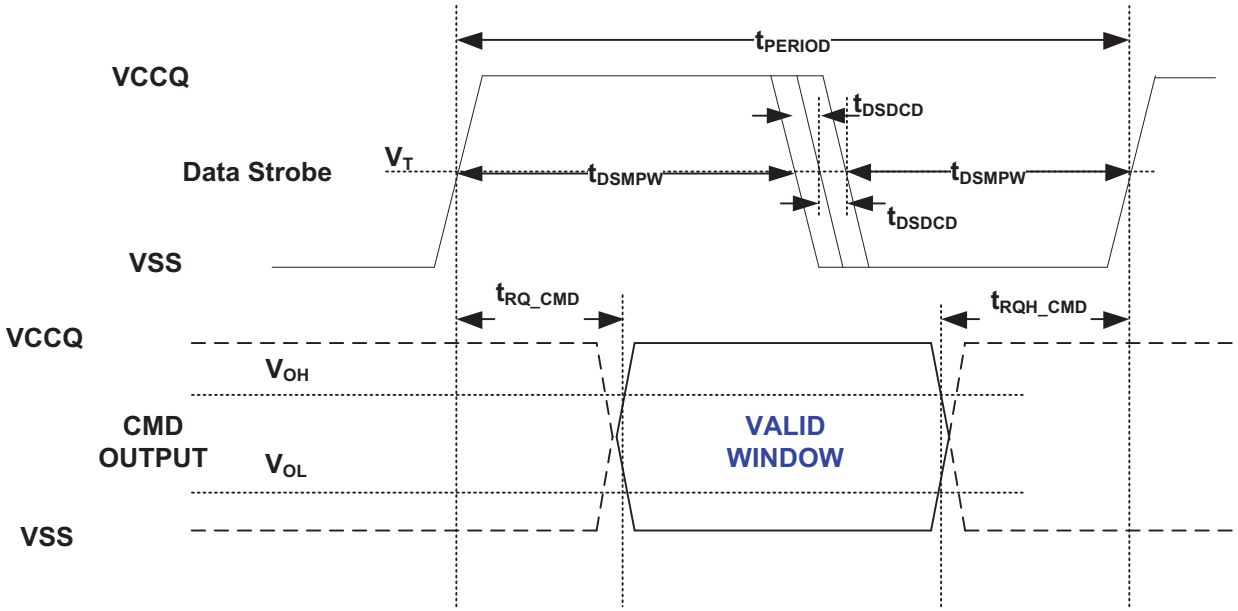
| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Pull-up resistance for CMD | $R_{CMD}$ | 4.7 | 100 | kΩ |
| Pull-up resistance for DAT0-7 | $R_{DAT}$ | 10 | 100 | kΩ |
| Pull-down resistance for Data Strobe | $R_{DS}$ | 10 | 100 | kΩ |
| Internal pull up resistance DAT1-DAT7 | $R_{int}$ | 10 | 150 | kΩ |
| Single Device capacitance | $C_{Device}$ | | 6 | pF |

***Note:***
*1. Recommended maximum value is 30 kΩ for 1.2V and 50 kΩ for 1.8V interface supply voltages.*

### 7.6.3 HS400 Device Command Output Timing

The Data Strobe is used to response of any command in HS400 mode.

**Figure 7.9** HS400 CMD Response Timing

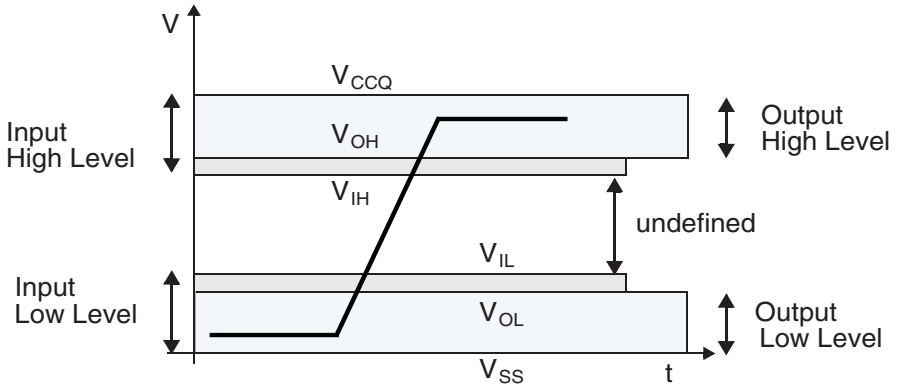



***Note:***
*$V_T$ = 50% of $V_{CCQ}$, indicates clock reference point for timing measurements.*

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Data Strobe | | | | | |
| Cycle time data transfer mode | $t_{PERIOD}$ | 5 | | | 200 MHz (max), between rising edges With respect to $V_T$ |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load |
| Duty cycle distortion | $t_{DSDCD}$ | 0.0 | 0.2 | ns | Allowable deviation from the input CLK duty cycle distortion ($t_{CKDCD}$) With respect to $V_T$ Includes jitter, phase noise |
| Minimum pulse width | $t_{DSMPW}$ | 2.0 | | ns | With respect to $V_T$ |
| Read pre-amble | $t_{RPRE}$ | 0.4 | - | tPERIOD | Max value is specified by manufacturer. Value up to infinite is valid |
| Read post-amble | $t_{RPST}$ | 0.4 | - | tPERIOD | Max value is specified by manufacturer. Value up to infinite is valid |
| CMD Response (referenced to Data Strobe) | | | | | |
| Output skew(CMD) | $t_{RQ_CMD}$ | | 0.4 | ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load |
| Output hold skew(CMD) | $t_{RQH_CMD}$ | | 0.4 | ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load |

## 7.7 Signal Levels

**Figure 7.10** Signal Levels




## 7.8 Open-Drain Mode Bus Signal Level

**Table 7.10 Open-Drain Mode Bus Signal Level**

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $V_{CCQ}$ -0.2 | | V | $I_{OH}$ = -100 µA |
| Output Low Voltage | $V_{OL}$ | | 0.3 | V | $I_{OLL}$ = 2 mA |

## 7.9 Push-Pull Mode Bus Signal Level — High Voltage e.MMC

**Table 7.11 Push-Pull Mode Bus Signal Level — High Voltage e.MMC**

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | 0.75 * $V_{CCQ}$ | | V | $I_{OH}$ = -100 µA at $V_{CCQ}$ min |
| Output Low Voltage | $V_{OL}$ | | 0.125 * $V_{CCQ}$ | V | $I_{OL}$ = 100 µA at $V_{CCQ}$ min |
| Input High Voltage | $V_{IH}$ | 0.625 * $V_{CCQ}$ | $V_{CCQ}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$ -0.3 | 0.25 * $V_{CCQ}$ | V | |

## 7.10 Push-Pull Bus Signal Level — Dual Voltage e.MMC

**Table 7.12 Push-Pull Bus Signal Level — Dual Voltage e.MMC**

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $V_{CCQ}$ -0.45V | | V | $I_{OH}$ = -2 mA |
| Output Low Voltage | $V_{OL}$ | | 0.45V | V | $I_{OL}$ = 2 mA |
| Input High Voltage | $V_{IH}$ | 0.65 * $V_{CCQ}$ | $V_{CCQ}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$ -0.3 | 0.35 * $V_{CCQ}$ | V | |

# 8. DC Parameter

## 8.1 Supply Voltage

**Table 8.1 Supply Voltage**

| Symbol | Min. | Max. | Unit |
|---|---|---|---|
| $V_{CC}$ | 2.7 | 3.6 | V |
| $V_{CCQ}$ | 1.7 | 1.95 | V |
| $V_{SS}$ | -0.5 | 0.5 | V |

## 8.2 Absolute Maximum Ratings

**Table 8.2 Absolute Maximum Ratings**

| Symbol | Min. | Max. | Unit |
|---|---|---|---|
| $V_{CC}$ | -0.3 | 4.0 | V |
| $V_{CCQ}$ | -0.3 | 4.0 | V |

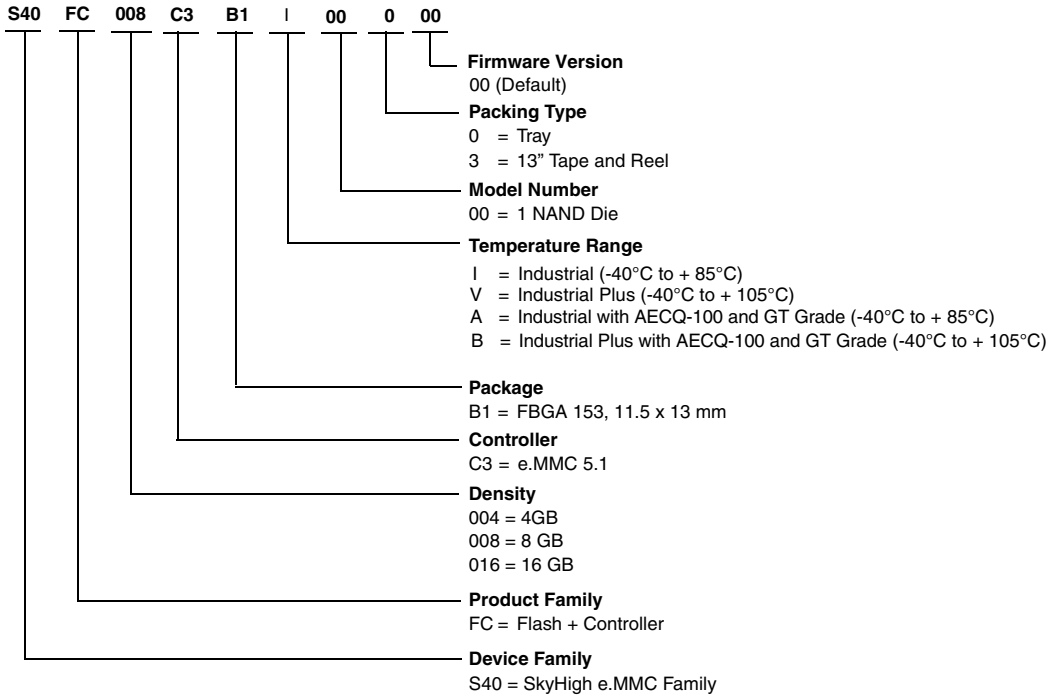
## 8.3 Bus Operating Condition

**Table 8.3 Bus Operating Condition**

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| Peak Voltage on all lines | -0.5 | $V_{CCQ}$ +0.5 | V |
| Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors) | -2 | 2 | µA |
| Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors) | -2 | 2 | µA |

# 9. Ordering Information

The ordering part number is formed by a valid combination of the following:



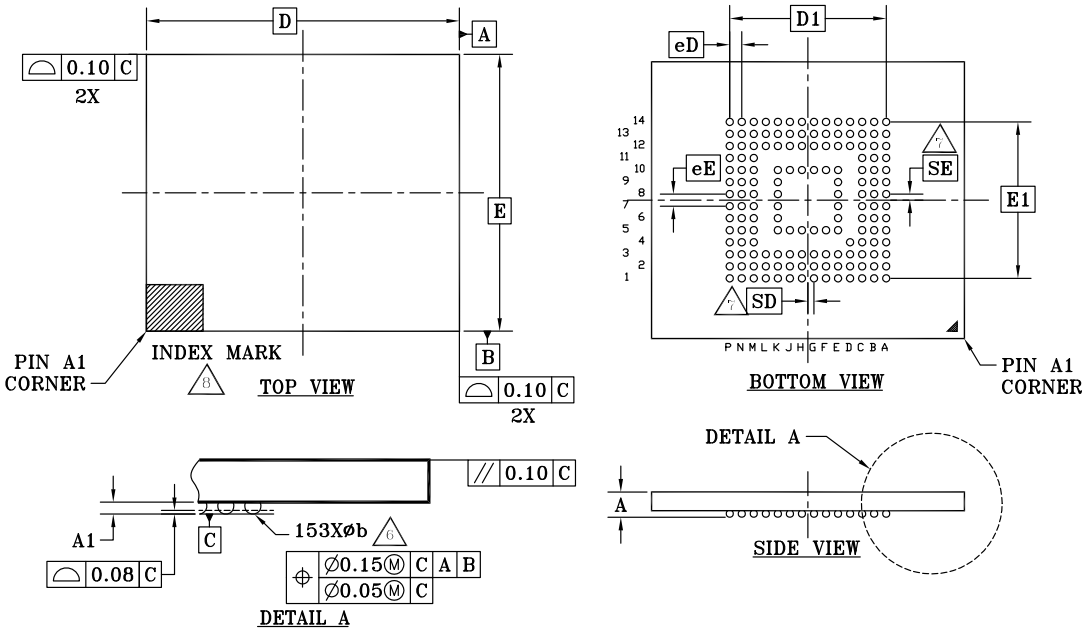

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| Valid Combinations | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Device Family** | **Product Family** | **Density** | **Controller** | **Package Type** | **Temperature Range** | **Model Number** | **Packing Type** | **Firmware Version** | **Package Description** |
| S40 | FC | 008 | C3 | B1 | I , V | 00 | 0, 3 | 00 | BGA |

# 10. Physical Diagram

## 10.1 VFBGA 153 — Package Dimensions 11.5 x 13 x 0.8 mm




| PACKAGE | TBD 153 | | | NOTE |
|---|---|---|---|---|
| JEDEC | MO-276 | | | |
| D X E | 13.00mm X 11.50mm PACKAGE | | | |
| SYMBOL | MIN. | NOM. | MAX. | |
| A | 0.70 | --- | 0.80 | PROFILE |
| A1 | 0.17 | --- | --- | BALL HEIGHT |
| D | | 13.00 BSC | | BODY SIZE |
| E | | 11.50 BSC | | BODY SIZE |
| D1 | | 6.50 BSC | | MATRIX FOOTPRINT |
| E1 | | 6.50 BSC | | MATRIX FOOTPRINT |
| MD | | 14 | | MATRIX SIZE D DIRECTION |
| ME | | 14 | | MATRIX SIZE E DIRECTION |
| n | | 153 | | BALL COUNT |
| Ø b | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| eE | | 0.50 BSC | | BALL PITCH |
| eD | | 0.50 BSC | | BALL PITCH |
| SD / SE | | 0.25 BSC | | SOLDER BALL PLACEMENT |
| | D5-D11,E11-K11,L4-L11,E4-K4 F6-F9,G6-G9,H6-H9,J6-J9 | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP 95, SECTION 4.6.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP 95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW D OR SE = 0.000. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = e/2
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
9. TEST PADS MAY BE PRESENT BUT ARE NOT SHOWN. THEY ARE FOR INTERNAL USE ONLY AND ARE NOT SOLDER BALLS.

TBD153-0.8/4.16.15

# 11. Document History Page

| Document Title: S40FC008<br>Document Number: 002-01117 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | | MNADA | 06/01/2022 | Initial release |
| A | | MNADA | 09/08/2022 | Removed Preliminary |
| B | | MNADA | 11/30/2022 | Add "V" option to the Valid Combinations section |
| C | | MNADA | 04/13/2023 | Removed VCCQ 2.7V-3.6V option |
| D | | MNADA | 01/02/2024 | Add Absolute Maximum Ratings |