2-Gb (DDP)/4-Gb (QDP), SEMPER™ Flash with Quad SPI

1.8 V, 3.0 V

Device overview

- Architecture
  - Infineon 45-nm MIRRORBIT™ technology that stores two data bits in each memory array cell
  - Multi-chip package (MCP)
    - 02GT Dual Die Package (DDP) 2 × 1 Gb die
    - 04GT Quad Die Package (QDP) 4 × 1 Gb die
  - Sector Architecture options
    - Uniform - Address space consists of all 256 KB Sectors
    - Hybrid
      Configuration 1: Address space consists of thirty-two 4 KB sectors grouped either on the top or the bottom while the remaining sectors are all 256 KB
      Configuration 2: Address space consists of thirty-two 4 KB sectors at the top and bottom while the remaining sectors are all 256 KB
  - Page Programming buffer of 256 or 512 bytes
  - OTP Secure Silicon array of 1024 bytes (32 × 32 bytes)

- Interface
  - Quad SPI
    - Supports 1S-1S-4S, 1S-4S-4S, 1S-4D-4D, 4S-4S-4S, 4S-4D-4D protocols
    - SDR option runs up to 83 MBps (166 MHz clock speed)
    - DDR option runs up to 102 MBps (102 MHz clock speed)
  - Dual SPI
    - Supports 1S-2S-2S protocol
    - SDR option runs up to 41.5 MBps (166 MHz clock speed)
  - SPI
    - Supports 1S-1S-1S protocol
    - SDR option runs up to 21 MBps (166 MHz clock speed)

- Highlights
  - Safety features
    - Functional Safety with the Industry's first ISO26262 ASIL B compliant and ASIL D ready NOR flash
    - EnduraFlex™ Architecture provides High-Endurance and Long Retention Partitions
    - Data Integrity CRC detects errors in memory array
    - SafeBoot reports device initialization failures, detects configuration corruption and provides recovery options
    - Built-in Error Correcting Code (ECC) corrects Single-bit Error and detects Double-bit Error (SECDED) on memory array data
    - Sector Erase Status indicator for power loss during erase
  - Protection features
    - Legacy Block Protection for memory array and device configuration
    - Advanced Sector Protection for individual memory array sector based protection
  - Hardware Reset through CS# Signaling method (JEDEC) / individual RESET# pin / DQ3_RESET# pin

Device overview

- Identification
  - Serial Flash Discoverable Parameters (SFDP) describing device functions and features
  - Device Identification, Manufacturer Identification, and Unique Identification

- Data Integrity
  - 02GT DDP, 04GT QDP devices
    - Minimum 2,560,000 Program-Erase cycles for the Main array
  - All devices
    - Minimum 300,000 Program-Erase cycles for the 4 KB Sectors
    - Minimum 25 Years Data Retention

- Supply voltage
  - 1.7 V to 2.0 V (HS-T)
  - 2.7 V to 3.6 V (HL-T)

- Grade / Temperature range
  - Industrial (–40°C to +85°C)
  - Industrial Plus (–40°C to +105°C)
  - Automotive AEC-Q100 Grade 3 (–40°C to +85°C)
  - Automotive AEC-Q100 Grade 2 (–40°C to +105°C)
  - Automotive AEC-Q100 Grade 1 (–40°C to +125°C)

- Packages
  - 02GT DDP, 04GT QDP devices:
    - 24-ball BGA 8 × 8 mm

1 Performance summary

Table 1 Maximum Read rates

Transaction	Initial Access Latency (Cycles)	Clock Rate (MHz)	MBps
SPI Read	0	50	6.25
SPI Fast Read	9	166	20.75
Dual Read SDR	7	166	41.50
Quad Read SDR	10	166	83.00
Quad Read DDR	7	102	102.00

Table 2 Typical Program and Erase rates

Operation	KBps
Page Programming 256 Bytes page buffer (4 KB Sector / 256 KB Sector)	595 / 533
Page Programming 512 Bytes page buffer (4 KB Sector / 256 KB Sector)	753 / 898
256 KB Sector Erase	331
4 KB Sector Erase	95

Table 3 Typical Current Consumption DDP device

Operation	Current (mA)
SDR Read 50 MHz	31
SDR Read 166 MHz	96
DDR Read 102 MHz	105
Program	50
Erase	50
Standby (HS-T)	0.022
Standby (HL-T)	0.028
Deep Power Down (HS-T)	0.0026
Deep Power Down (HL-T)	0.0044

Table 4 Typical Current Consumption QDP device

Operation	Current (mA)
SDR Read 50 MHz	31
SDR Read 166 MHz	96
DDR Read 102 MHz	105
Program	50
Erase	50
Standby (HS-T)	0.044
Standby (HL-T)	0.054
Deep Power Down (HS-T)	0.0052
Deep Power Down (HL-T)	0.0088

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2 Pinout and Signal description

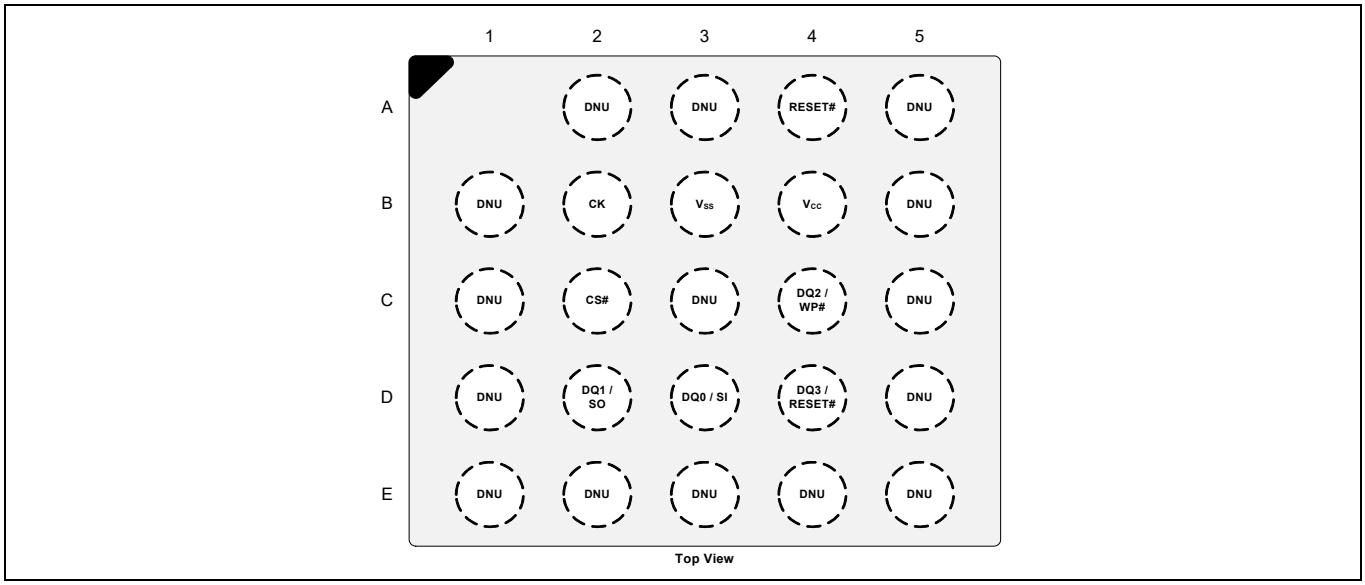


Figure 1 24-ball BGA pinout configuration

Table 5 Signal description

Symbol	Type	Mandatory / Optional	Description
CS#	Input	Mandatory	**Chip Select (CS#).** All bus transactions are initiated with a HIGH to LOW transition on CS# and terminated with a LOW to HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the active mode. When CS# is driven HIGH, the device enters Standby mode, unless an internal embedded operation is in progress. All other input pins are ignored and the output pins are put in high impedance state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH.
CK	Input	Mandatory	**Clock (CK).** Clock provides the timing of the serial interface. Transactions are latched on the rising edge of the clock. In SDR protocol, command, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DDR protocol, command, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.
DQ0 / SI	Input/ Output	Mandatory	Serial Input (SI) for single SPI protocol **DQ0 Input/ Output** for Dual or Quad SPI protocol
DQ1 / SO	Input/ Output	Mandatory	Serial Output (SO) for single SPI protocol **DQ1 Input/ Output** for Dual or Quad SPI protocol
DQ2 / WP#	Input/ Output (weak pull-up)	Optional	Write Protect (WP#) for single and dual SPI protocol **DQ2 Input/ Output** for Quad SPI protocol The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for Quad transactions or write protection. If write protection is enabled, the host system is required to drive WP# HIGH or LOW during write register transactions.

Table 5 Signal description *(continued)*

Symbol	Type	Mandatory / Optional	Description
DQ3 / RESET#	Input/ Output (weak pull-up)	Optional	**RESET#** for single and dual SPI protocol. This signal can be configured as RESET# when CS# is HIGH or Quad SPI protocol is disabled. **DQ3 Input/ Output** for Quad SPI protocol The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for Quad SPI transactions or RESET#
RESET#	Input (weak pull-up)	Optional	**Hardware Reset (RESET#)**. When LOW, the device will self initialize and return to the array read state. DQ[3:0] are placed into the high impedance state when RESET# is LOW. RESET# includes a weak pull-up, meaning, if RESET# is left unconnected it will be pulled up to the HIGH state on its own.
V_{CC}	Power Supply	Mandatory	Core Power Supply
V_{SS}	Ground Supply	Mandatory	Core Ground
DNU	–	–	Do Not Use

3 General description

The Infineon SEMPER™ Flash with Quad SPI family of products are high-speed CMOS, MIRRORBIT™ NOR flash devices. SEMPER™ Flash is designed for Functional Safety with development according to ISO 26262 standard to achieve ASIL-B compliance and ASIL-D readiness.

SEMPER™ Flash with Quad SPI devices support traditional SPI single bit serial input and output, optional two bit (Dual I/O or DIO) as well as four bit wide Quad I/O (QIO) and Quad Peripheral Interface (QPI) protocols. In addition, there are DDR read transactions for QIO and QPI that transfer address and read data on both edges of the clock.

Read operations from the device are burst oriented. Read transactions can be configured to use either a wrapped or linear burst. Wrapped bursts read from a single page whereas linear bursts can read the whole memory array.

The erased state of each memory bit is a logic 1. Programming changes a logic 1 (HIGH) to a logic 0 (LOW). Only an erase operation can change a memory bit from a 0 to a 1. An erase operation must be performed on a complete sector (4 KB or 256 KB).

SEMPER™ Flash provides a flexible sector architecture. The address space can be configured as either a uniform 256 KB sector array, or a hybrid configuration 1 where thirty-two 4 KB sectors are either grouped at the top or at the bottom while the reaming sectors are all 256 KB, or a hybrid configuration 2 where the thirty-two 4 KB sectors at the top and the bottom while the remaining sectors are all 256 KB.

The Page Programming Buffer used during a single programming operation is configurable to either 256 bytes or 512 bytes. The 512 byte option provides the highest programming throughput.

This device is an MCP with DDP or QDP stacked die, with the control signals for all dies tied together internally in the package.

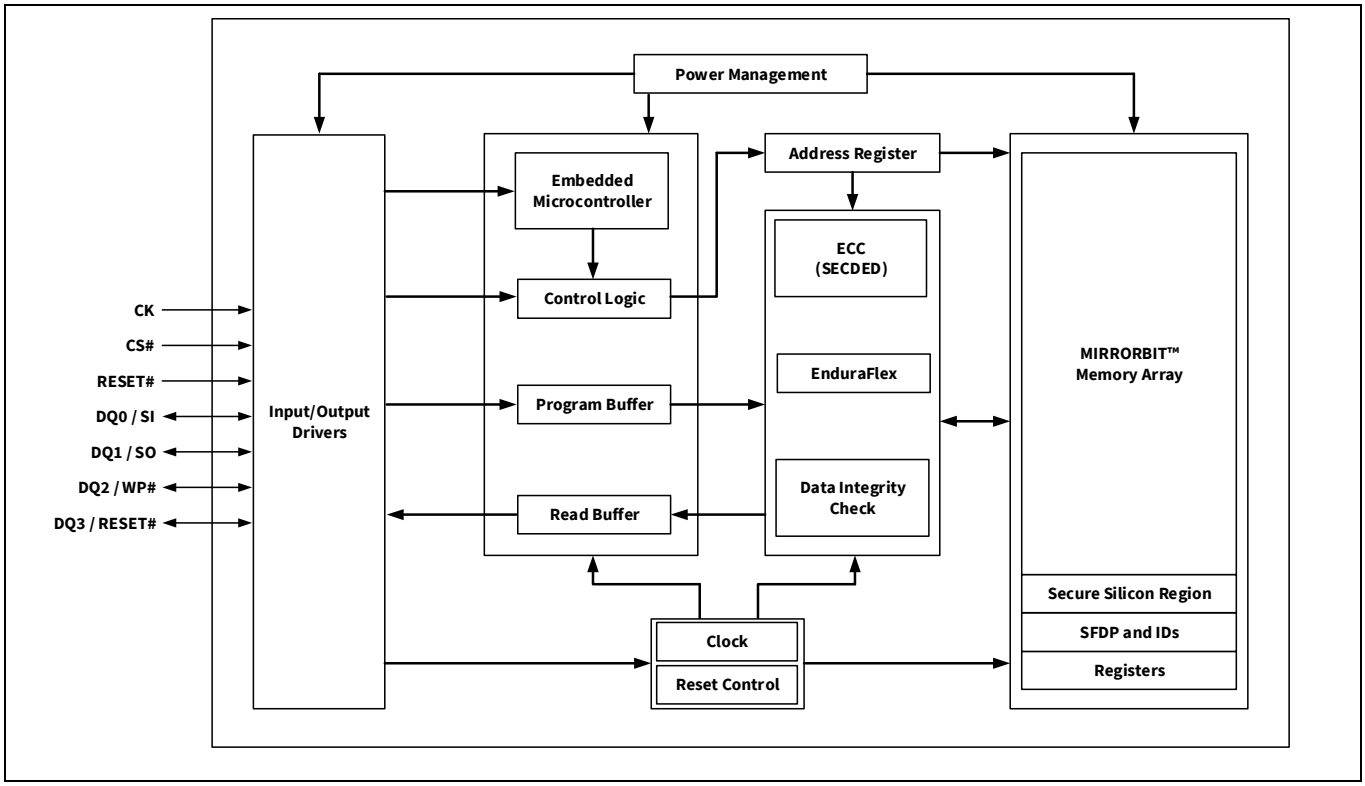


Figure 2 Logic block diagram monolithic device

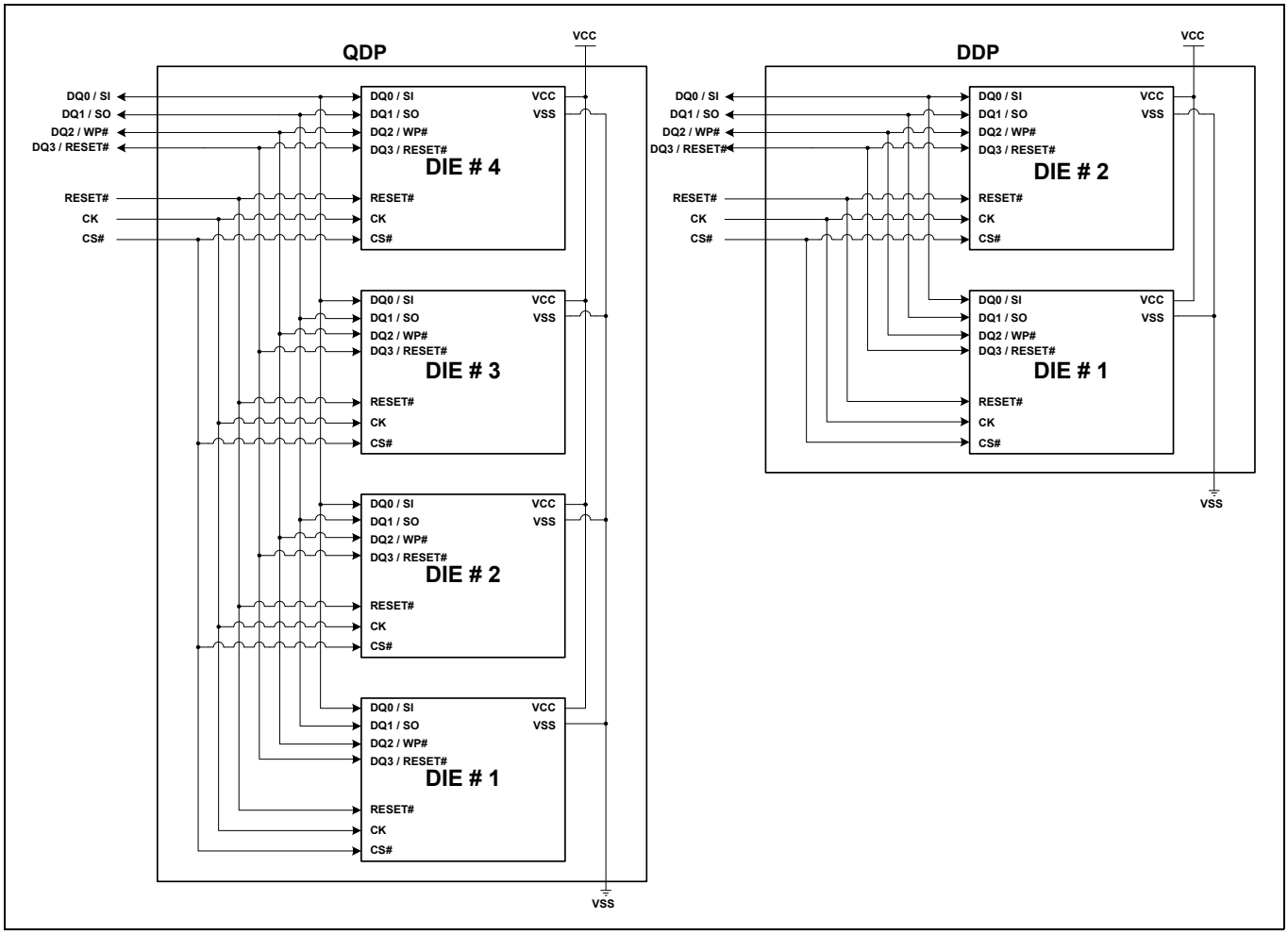


Figure 3 MCP diagram

General description

The SEMPER™ Flash with Quad SPI family consists of multiple densities with, 1.8 V and 3.0 V core voltage options.

The device control logic is subdivided into two parallel operating sections: the Host Interface Controller (HIC) and the Embedded Algorithm Controller (EAC). The HIC monitors signal levels on the device inputs and drives outputs as needed to complete read, program and write data transfers with the host system. The HIC delivers data from the currently entered address map on read transfers; places write transfer address and data information into the EAC command memory, and notifies the EAC of power transition, and write transfers. The EAC interrogates the command memory, after a program or write transfer, for legal command sequences and performs the related Embedded Algorithms.

Changing the nonvolatile data in the memory array requires a sequence of operations that are part of Embedded Algorithms (EA). The algorithms are managed entirely by the internal EAC. The main algorithms perform programming and erase of the main flash array data. The host system writes command codes to the flash device. The EAC receives the command, performs all the necessary steps to complete the transaction, and provides status information during the progress of an EA.

Executing code directly from Flash memory is often called Execute-In-Place (XIP). By using XIP with Semper Flash devices at the higher clock rates with Quad or DDR Quad SPI transactions, the data transfer rate can match or exceed traditional parallel or asynchronous NOR flash memories while reducing signal count dramatically.

EnduraFlex™ Architecture provides system designers the ability to customize the NOR Flash endurance and retention for their specific application. The host defines partitions for high endurance or long retention, providing up to 1+ million cycles or 25 years of data retention.

The SEMPER™ Flash with Quad SPI device supports error detection and correction by generating an embedded Hamming error correction code during memory array programming. This ECC code is then used for single-bit and double-bit error detection and single-bit correction during read.

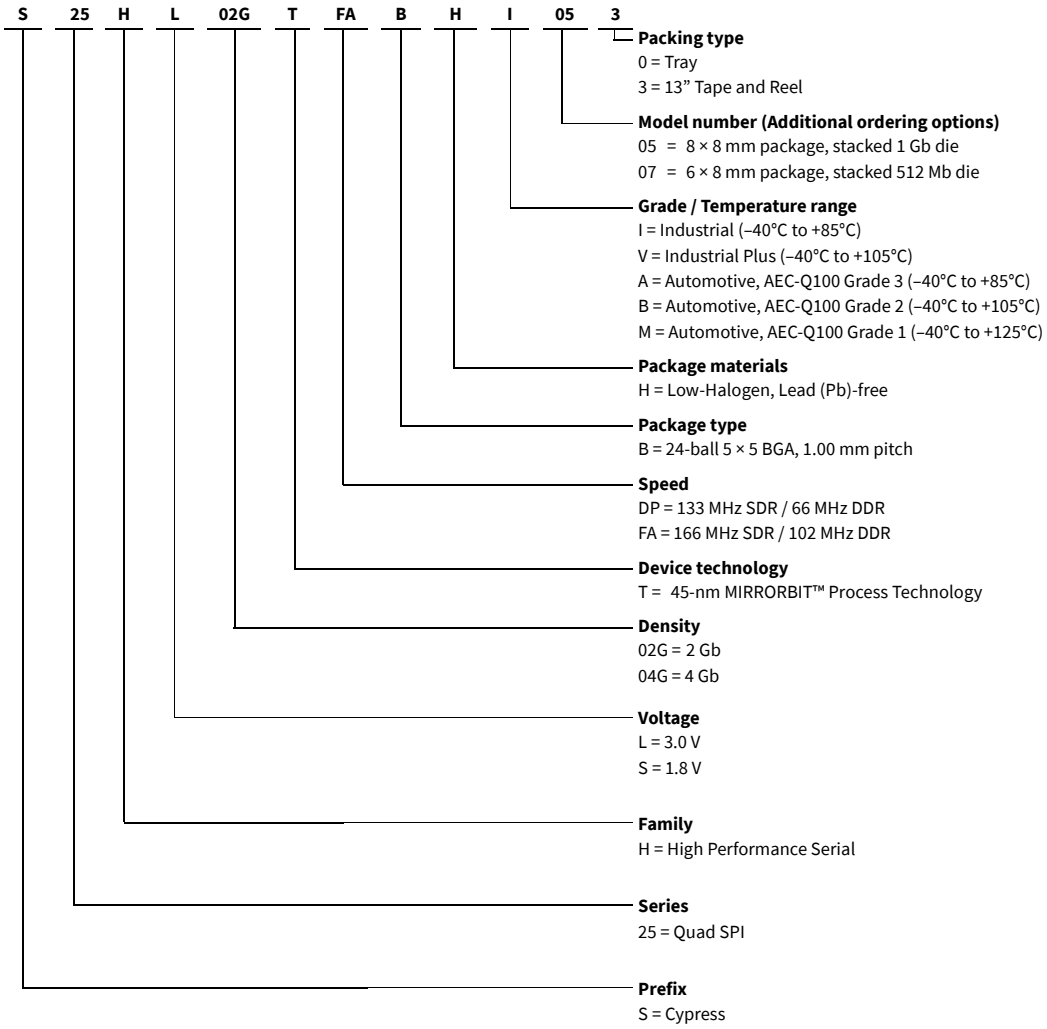
The SEMPER™ Flash with Quad SPI device has built-in diagnostic features providing the host system with the device status:

- Program and Erase Operation: Reporting of program or erase success, failure, and suspend status.
- Error Detection and Correction: 1-bit and/or 2-bit error status with address trapping and error count.
- Data Integrity Check: Error detection over memory array contents.
- SafeBoot: Reporting of proper flash device initialization and configuration corruption recovery.
- Sector Erase Status: Reporting of erase success or failure status per sector.
- Sector Erase Counter: Counts the number of erase cycles per sector.

4 Ordering information

4.1 Ordering part number

The ordering part number is formed by a valid combination of the following:



Register for the SEMPER™ Access Program and get access to datasheets, application notes, models, software and evaluation kits

Revision history

Document revision	Date	Description of changes
**	2019-11-11	Initial release of summary datasheet.
*A	2023-08-02	Updated Document Title to read as “S25HS02GT, S25HS04GT, S25HL02GT, S25HL04GT, 2-Gb (DDP)/4-Gb (QDP), SEMPER™ Flash with Quad SPI 1.8 V, 3.0 V”. Migrated to Infineon template.

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