BROADCOM®

Data Sheet

ACPL-071L and ACPL-074L

Single-Channel and Dual-Channel High-Speed 15-MBd CMOS Optocoupler

Description

The Broadcom® ACPL-071L (single-channel) and ACPL-074L (dual-channel) are 15-MBd CMOS optocouplers in SOIC-8 package. The optocouplers use the latest CMOS IC technology to achieve outstanding performance with very low power consumption. Basic building blocks of ACPL-071L and ACPL-074L are high speed LEDs and CMOS detector ICs. Each detector incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

Applications

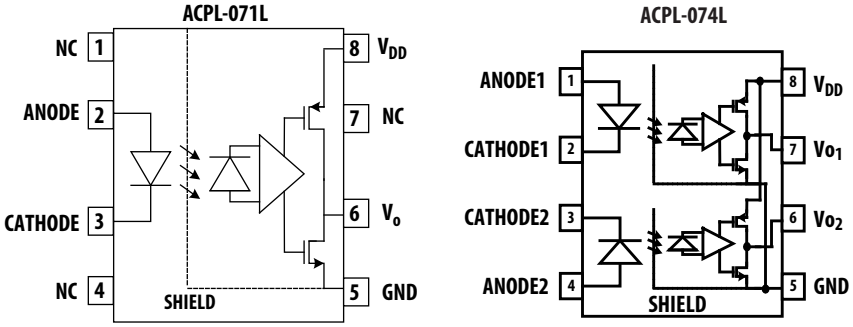
- Digital field bus isolation:
- CANBus, RS485, USB
- Multiplexed data transmission
- Computer peripheral interface
- Microprocessor system interface
- DC/DC converter

Features

- +3.3V and +5 V CMOS compatibility
- 30 ns max. pulse width distortion
- 40 ns max. propagation delay (3.3V supply voltage)
- 30 ns max. propagation delay skew
- High speed: 15 MBd min.
- 10 kV/µs minimum common mode rejection
- –40°C to 105°C temperature range
- Safety and regulatory approvals:
  - UL recognized: 3750 V rms for 1 min. per UL 1577
  - CSA component acceptance Notice #5
  - IEC/EN/DIN EN 60747-5-5

CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Functional Diagram



NOTE: A 0.1-µF bypass capacitor must be connected as close as possible between pins VDD and GND.

Truth Table	
LED	**V_O, OUTPUT**
OFF	H
ON	L

Ordering Information

ACPL-071L/074L are UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part Number	Option RoHS Compliant	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-071L	-000E	SO-8	X			100 per tube
	-500E		X	X		1500 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1500 per reel
ACPL-074L	-000E	SO-8	X			100 per tube
	-500E		X	X		1500 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-071L-500E to order product of Small Outline SO-8 package in Tape and Reel packaging in RoHS compliant.

Example 2:

ACPL-074L-000E to order product of Small Outline SO-8 package in tube packaging and RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Reflow Soldering Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

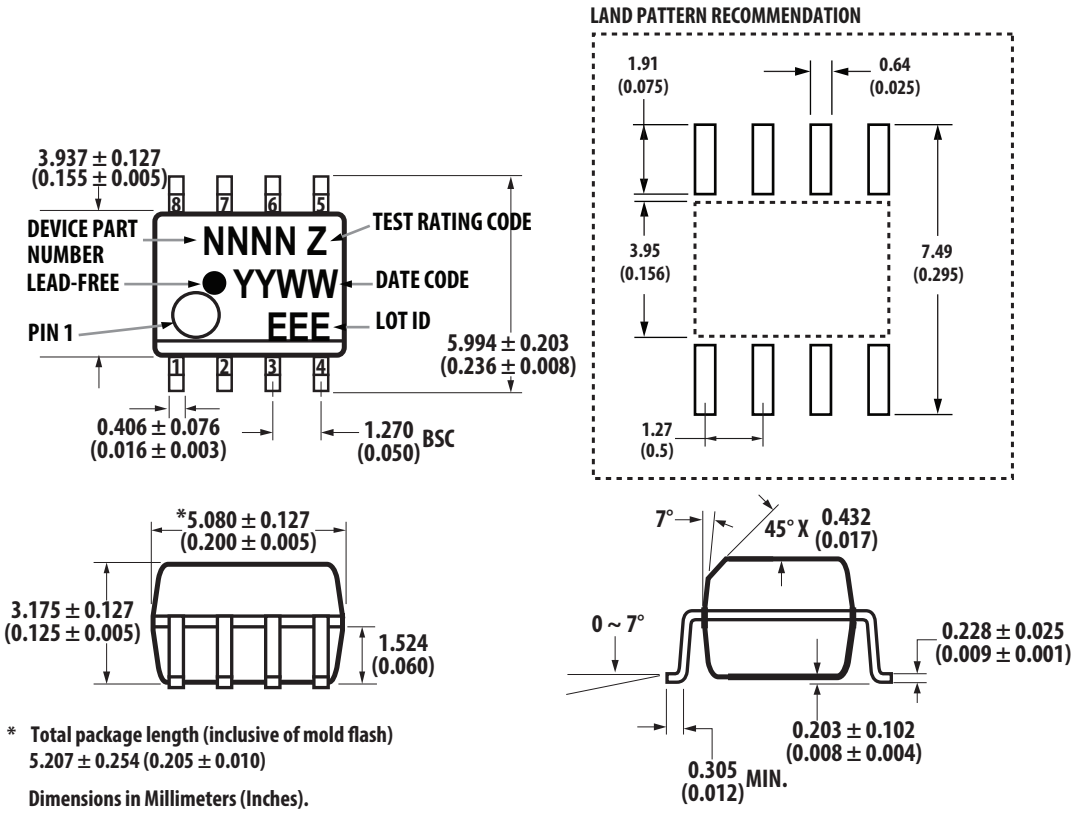
Regulatory Information

The ACPL-071L and ACPL-074L have been approved by the following organizations:

UL	Recognized under UL 1577, component recognition program, File E55361.
CSA	Approved under CSA Component Acceptance Notice #5, File CA88324.
IEC/EN/DIN EN 60747-5-5	

Package Dimensions

ACPL-071L and ACPL-074L (Small Outline S0-8 Package)



* Total package length (inclusive of mold flash)
5.207 ± 0.254 (0.205 ± 0.010)

Dimensions in Millimeters (Inches).

Note: Floating lead protrusion is 0.15 mm (6 mils) max.
Lead coplanarity = 0.10 mm (0.004 inches) max.

Option number 500 not marked.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Option 060	Unit
Installation classification per DIN VDE 0110, Table 1			
for rated mains voltage ≤ 150 Vrms		I – IV	
for rated mains voltage ≤ 300 Vrms		I – IV	
for rated mains voltage ≤ 600 Vrms		I – III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	Vpeak
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1s, Partial discharge < 5 pC	V_{PR}	1063	Vpeak
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m=10s, Partial discharge < 5 pC	V_{PR}	907	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60s)	V_{IOTM}	6000	Vpeak
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	150	°C
Input Current	$I_{S, INPUT}$	150	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, VIO = 500 V	R_S	≥ 10^9	Ω

NOTE: These optocouplers are suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	+125	°C
Ambient Operating Temperature	T_A	–40	+105	°C
Supply Voltages	V_{DD}	0	6.0	Volts
Output Voltage	V_O	–0.5	V_{DD} +0.5	Volts
Average Forward Input Current	I_F	—	20.0	mA
Average Output Current	I_o	—	10.0	mA
Input Power Dissipation	P_I	—	35	mW
Output Power Dissipation	P_O	—	100	mW
Lead Solder Temperature	260°C for 10s., 1.6 mm below seating plane			
Solder Reflow Temperature Profile	See Reflow Soldering Profile			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+105	°C
Supply Voltages	V_{DD}	4.5	5.5	V
		3.0	3.6	V
Input Current (ON)	I_F	12	18	mA
Supply Voltage Slew Rate[a]	S_R	0.5	500	V/ms

a. Slew rate of supply voltage ramping is recommended to ensure no glitch more than 1V to appear at the output pin.

Electrical Specifications

Over recommended temperature (T_A = –40°C to +105°C), 3.0V ≤ V_{DD} ≤ 3.6V and 4.5V ≤ V_{DD} ≤ 5.5V.

All typical specifications are at T_A = +25°C, V_{DD} = +3.3V.

Parameter	Symbol	Part Number	Min.	Typ.	Max.	Units	Test Conditions
Input Forward Voltage	V_F		1.3	1.5	1.8	V	I_F = 14 mA
Input Reverse Breakdown Voltage	BV_R		5.0	—	—	V	I_R = 10 µA
Logic High Output Voltage	V_{OH}		V_{DD} – 1	V_{DD} – 0.3	—	V	I_F = 0, I_O = –4 mA, V_{DD} = 3.3V
			V_{DD} – 1	V_{DD} – 0.2	—	V	I_F = 0, I_O = –4 mA, V_{DD} = 5V
Logic Low Output Voltage	V_{OL}		—	0.35	0.8	V	I_F = 14 mA, I_O = 4 m A, V_{DD} = 3.3V
			—	0.2	0.8	V	I_F = 14 mA, I_O = 4 mA, V_{DD} = 5V
Input Threshold Current	I_{TH}		—	4.5	8.8	mA	I_{OL} = 20 µA
Logic Low Output Supply Current	I_{DDL}	ACPL-071L	—	4.1	6.0	mA	I_F = 14 mA
		ACPL-074L	—	8.3	12.0	mA	I_F = 14 mA
Logic Low Output Supply Current	I_{DDH}	ACPL-071L	—	3.8	6.0	mA	I_F = 0
		ACPL-074L	—	7.6	12.0	mA	I_F = 0

Switching Specifications

Over recommended temperature (T_A = –40°C to +105°C), 3.0V ≤ V_{DD} ≤ 3.6V and 4.5V ≤ V_{DD} ≤ 5.5V.

All typical specifications are at T_A = +25°C, V_{DD} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Time to Logic Low Output[a]	t_{PHL}	—	29	40	ns	I_F = 14 mA, C_L = 15 pF, V_{DD} = 3.3V, CMOS Signal Levels
		—	—	50	ns	I_F = 14 mA, C_L = 15 pF, V_{DD} = 5V, CMOS Signal Levels
Propagation Delay Time to Logic High Output[a]	t_{PLH}	—	22	40	ns	I_F = 14 mA, C_L = 15 pF, V_{DD} = 3.3V, CMOS Signal Levels
		—	—	50	ns	I_F = 14 mA, C_L = 15 pF, V_{DD} = 5V, CMOS Signal Levels
Pulse Width	t_{PW}	66.7	—	—	ns	
Pulse Width Distortion[b]	|PWD |	0	7	25	ns	I_F = 14 mA, C_L = 15 pF, V_{DD} = 3.3V, CMOS Signal Levels
		—	—	30	ns	I_F = 14 mA, C_L = 15 pF, V_{DD} = 5V, CMOS Signal Levels
Propagation Delay Skew[c]	t_{PSK}	—	—	30	ns	I_F = 14 mA, C_L = 15 pF, CMOS Signal Levels
Output Rise Time (10% – 90%)	t_R	—	20	—	ns	I_F = 14 mA, C_L = 15 pF, CMOS Signal Levels
Output Fall Time (90% - 10%)	t_F	—	25	—	ns	I_F = 14 mA, C_L = 15 pF, CMOS Signal Levels
Common Mode Transient Immunity at Logic High Output[d]	| CM_H |	10	15	—	kV/µs	V_{CM} = 1000 V, T_A = 25°C, I_F = 0 mA
Common Mode Transient Immunity at Logic Low Output[e]	| CM_L |	10	15	—	kV/µs	V_{CM} = 1000 V, T_A = 25°C, I_F = 14 mA

a. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input pulse to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input pulse to the 50% level of the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

Package Characteristics

All Typical at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Insulation	II-O	—	—	1.0	µA	45% RH, t = 5s, V_{I-O} = 3 kV DC, T_A = 25°C
Input-Output Momentary Withstand Voltage	VISO	3750	—	—	Vrms	RH 50%, t = 1 min., T_A = 25°C
Input-Output Resistance	R I-O	—	10^{12}	—	Ω	V_{I-O} = 500 V dc
Input-Output Capacitance	C I-O	—	0.6	—	pF	f = 1 MHz, T_A = 25°C

Figure 1: Typical Input Diode Forward Characteristic

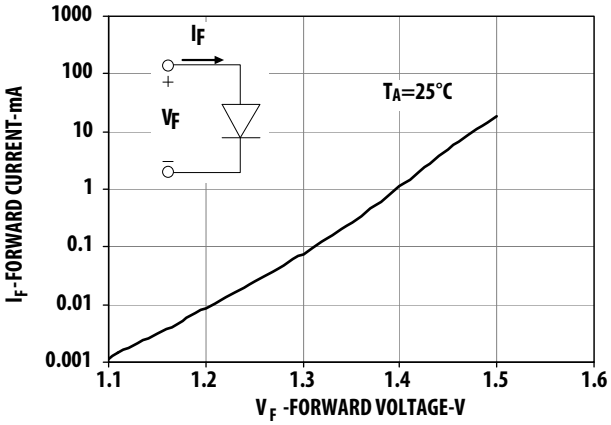


Figure 2: Typical Input Threshold Current vs. Temperature

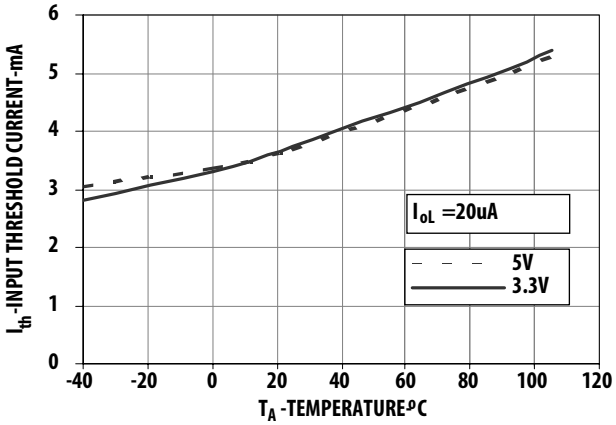


Figure 3: Typical Logic High O/P Supply Current vs. Temperature for ACPL-074L

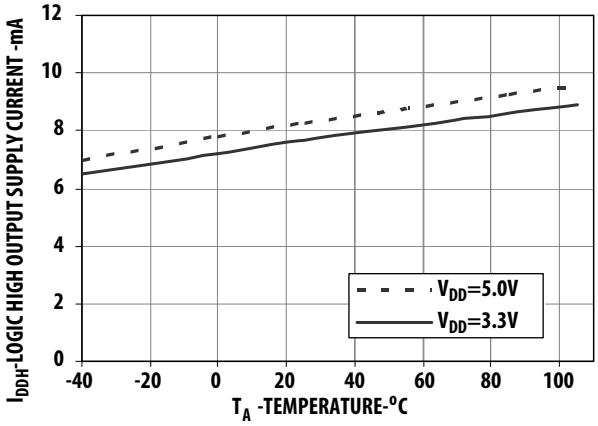


Figure 4: Typical Logic Low O/P Supply Current vs. Temperature for ACPL-074L

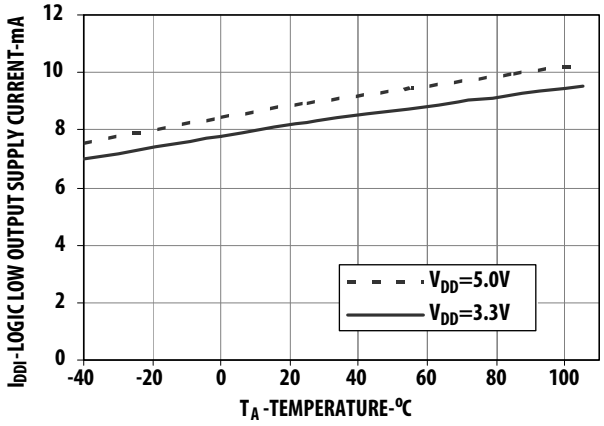


Figure 5: Typical Switching speed vs. Pulse Input Current at 5V Supply Voltage

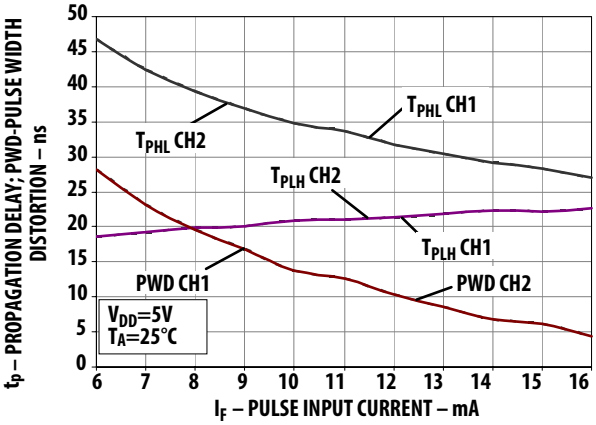


Figure 6: Typical Switching Speed vs. Pulse Input Current at 3.3V Supply Voltage

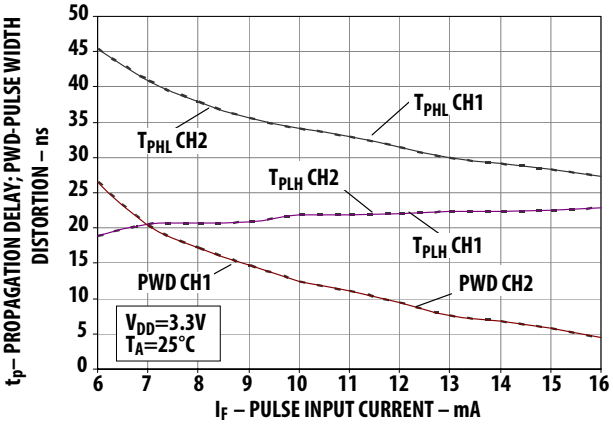
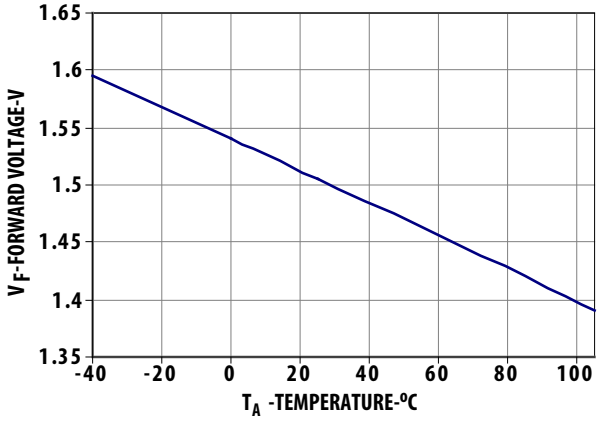


Figure 7: Typical V_F vs. Temperature



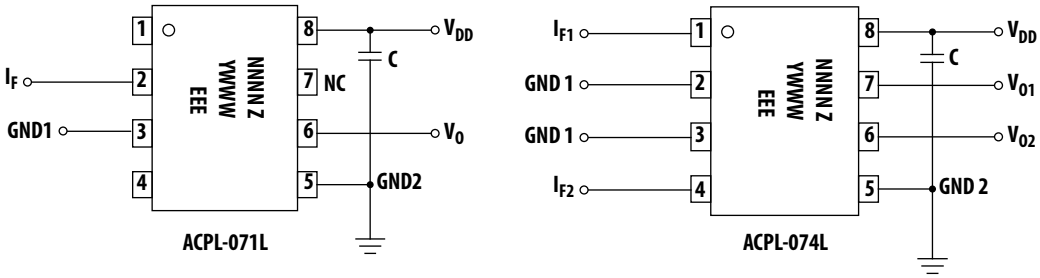
Application Information

Bypassing and PC Board Layout

The ACPL-071L and ACPL-074L optocouplers are extremely easy to use. ACPL-071L and ACPL-074L provide CMOS logic output due to the high-speed CMOS IC technology used.

The external components required for proper operation are the input limiting resistor and the output bypass capacitor. Capacitor should be placed as close as possible to the optocoupler and values should be between 0.01 µF and 0.1 µF.

Figure 8: Recommended Printed Circuit Board Layout



Powering Sequence

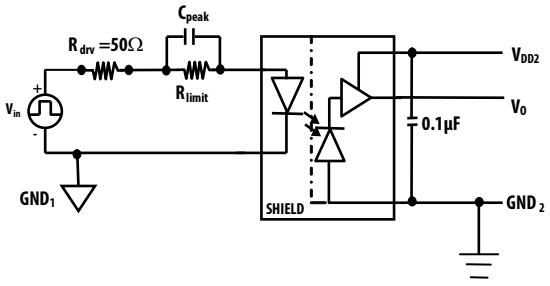
V_{DD} needs to achieve a minimum level of 3.0V before powering up the output connecting component.

Input Limiting Resistors

ACPL-071L and ACPL-074L are direct current driven (Figure 8), and thus eliminate the need for input power supply. To limit the amount of current flowing through the LED, it is recommended that a 210Ω resistor is connected in series with anode of LED (that is, Pin 2 for ACPL-071L and Pins 1 and 4 for ACPL-074L) at 5V input signal. At 3.3V input signal, it is recommended to connect a 80Ω resistor in series with anode of LED.

The recommended limiting resistors are based on the assumption that the driver output impedence is 50 (as shown in Figure 9).

Figure 9: Connection of Peaking capacitor (Cpeak) in Parallel of the Input Limiting Resistor (RIlimit) to Improve Speed Performance



Speed Improvement

A peaking capacitor can be placed across the input current limit resistor (Figure 9) to achieve enhanced speed performance. The value of the peaking cap is dependent to the rise and fall time of the input signal and supply voltages and LED input driving current (If). Figure 10 shows significant improvement of propagation delay and pulse with distortion with added peak capacitor at driving current of 14 mA and 3.3V or 5V power supply.

Figure 10: Improvement of t_p and PWD with Added 100 pF Peaking Capacitor in Parallel of Input Limiting Resistor

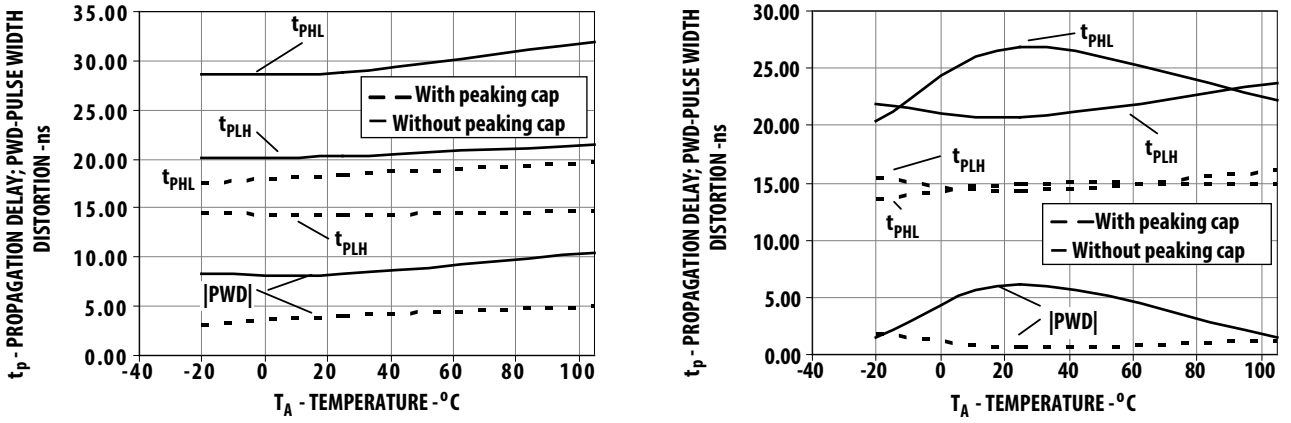
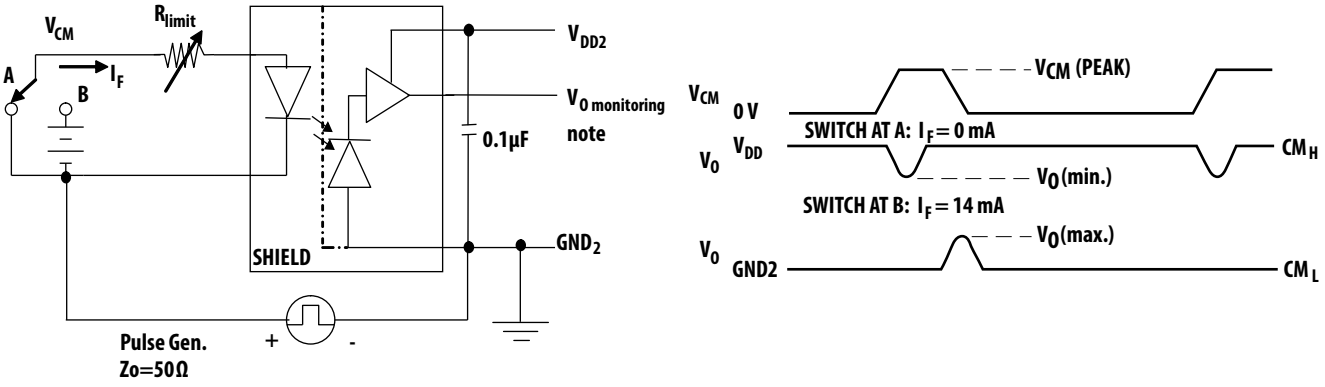


Figure 11: Test circuit for Common Mode Transient Immunity and Typical Waveforms. R_{total} is the total resistance of the driver output impedence (which is assumed to be 50Ω) and the limiting resistor ($R_{total} = R_{drv} + R_{limit}$).



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