# SNx4HCT245 具有三态输出的八路总线收发器

## 1 特性

- 4.5V 至 5.5V 的工作电压范围
- 高电流三态输出直接驱动总线或多达 15 个 LSTTL 负载
- 低功耗，$I_{CC}$ 最大值为 80μA
- $t_{pd}$ 典型值 = 14 ns
- 电压为 5V 时，输出驱动为 ±6mA
- 低输入电流，最大值 1μA
- 输入兼容 TTL 电压

## 2 应用

- 工厂自动化与控制
- 电网基础设施
- 电子销售终端
- 多功能打印机
- 电机驱动器
- 存储器
- 电信基础设施

## 3 说明

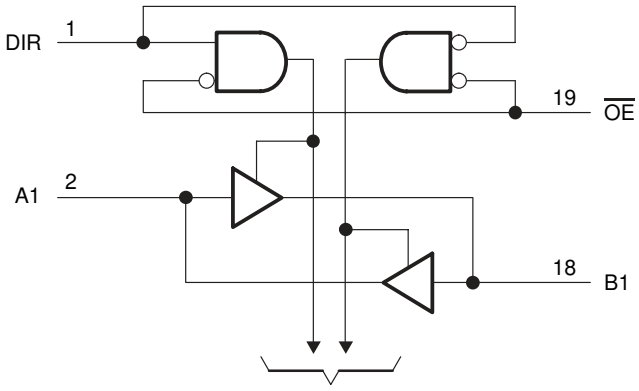
SNx4HCT245 八路总线收发器专为数据总线之间的异步双向通信而设计。控制功能实现可更大限度地减少外部时序要求。

根据方向控制 (DIR) 输入上的逻辑电平，SNx4HCT245 器件将数据从 A 总线发送至 B 总线，或者将数据从 B 总线发送至 A 总线。输出使能 ($\overline{OE}$) 输入可用于禁用器件，这样可有效隔离总线。

**器件信息**

| 器件型号 | 封装(1) | 封装尺寸（标称值） |
|---|---|---|
| SN54HCT245 | J（CDIP，20） | 24.20mm × 6.92mm |
| | FK（LCCC，20） | 8.89mm × 8.89mm |
| | W（CFP，20） | 13.09mm × 6.92mm |
| SN74HCT245 | DW（SOIC，20） | 12.80mm × 7.50mm |
| | N（PDIP，20） | 24.33mm × 6.35mm |
| | NS（SO，20） | 12.60mm × 5.30mm |
| | PW（TSSOP，20） | 6.50mm × 4.40mm |
| | DB（SSOP，20） | 7.80mm × 7.20mm |
| | DGS（VSSOP，20） | 5.10mm × 3.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

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**逻辑图（正逻辑）**

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision G (September 2022) to Revision H (December 2022) | Page |
|---|---|
| • 添加了 DGS 封装信息 | 1 |
| • Added DGS package values in the *Thermal Information* table | 5 |

| Changes from Revision F (August 2016) to Revision G (September 2022) | Page |
|---|---|
| • 更新了整个文档中的表格、图和交叉参考的编号格式 | 1 |

| Changes from Revision E (August 2003) to Revision F (August 2016) | Page |
|---|---|
| • 删除了“订购信息”，请参阅数据表末尾的 POA | 1 |
| • 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 | 1 |
| • Updated values in the *Thermal Information* table | 5 |


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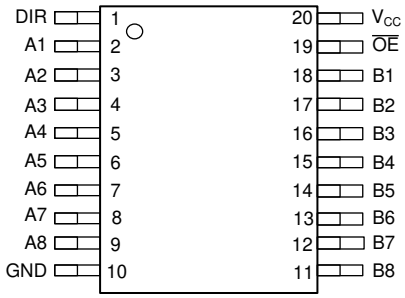
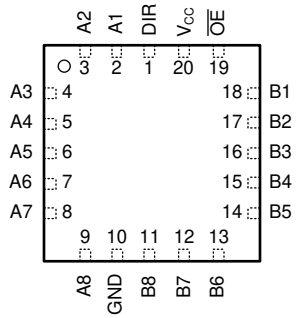
## 5 Pin Configuration and Functions




**J, W, DB, DW, N, NS, PW or DGS Packages 20-Pin CDIP, CFP, SSOP, SOIC, PDIP, SO, TSSOP or VSSOP Top View**




**FK Package 20-Pin LCCC Top View**

**Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | DIR | I | Direction select. High = A to B, Low = B to A |
| 2 | A1 | I/O | Channel 1 port A |
| 3 | A2 | I/O | Channel 2 port A |
| 4 | A3 | I/O | Channel 3 port A |
| 5 | A4 | I/O | Channel 4 port A |
| 6 | A5 | I/O | Channel 5 port A |
| 7 | A6 | I/O | Channel 6 port A |
| 8 | A7 | I/O | Channel 7 port A |
| 9 | A8 | I/O | Channel 8 port A |
| 10 | GND | — | Ground |
| 11 | B8 | O/I | Channel 8 port B |
| 12 | B7 | O/I | Channel 7 port B |
| 13 | B6 | O/I | Channel 6 port B |
| 14 | B5 | O/I | Channel 5 port B |
| 15 | B4 | O/I | Channel 4 port B |
| 16 | B3 | O/I | Channel 3 port B |
| 17 | B2 | O/I | Channel 2 port B |
| 18 | B1 | O/I | Channel 1 port B |
| 19 | $\overline{OE}$ | I | Output enable, active low. High = all ports in high impedance mode, Low = all ports active |
| 20 | $V_{CC}$ | — | Power supply |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_J$ | Operating virtual junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $\Delta t/\Delta v$ | Input transition rise and fall time | | | | 500 | ns |
| $T_A$ | Operating free-air temperature | SN54HCT245 | –55 | | 125 | °C |
| | | SN74HCT245 | –40 | | 85 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | SNx4HCT245 | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | J (CDIP) | W (CFP) | FK (LCCC) | DB (SSOP) | DW (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | DGS (VSSOP) | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | — | — | — | 84.6 | 70.4 | 43.4 | 68.9 | 94.9 | 118.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 38.7 | 60.8 | 37.1 | 44.3 | 36.5 | 29.5 | 34.7 | 30.2 | 57.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.8 | 100.4 | 36.1 | 40.2 | 38.1 | 24.3 | 36.4 | 45.7 | 73.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | — | — | — | 11.1 | 11.3 | 15 | 11.6 | 1.5 | 5.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | — | — | — | 39.7 | 37.7 | 24.2 | 36 | 45.1 | 72.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 11.5 | 8.5 | 4.3 | — | — | — | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-Level Output Voltage | | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 µA | $T_A$ = 25°C | 4.5 V | 4.4 | 4.499 | | V |
| | | | | | SN54HCT245 | | 4.4 | | | |
| | | | | | SN74HCT245 | | 4.4 | | | |
| | | | | $I_{OH}$ = –6 mA | $T_A$ = 25°C | | 3.98 | 4.3 | | |
| | | | | | SN54HCT245 | | 3.7 | | | |
| | | | | | SN74HCT245 | | 3.84 | | | |
| $V_{OL}$ | Low-Level Output Voltage | | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | $T_A$ = 25°C | 4.5 V | | 0.001 | 0.1 | V |
| | | | | | SN54HCT245 | | | | 0.1 | |
| | | | | | SN74HCT245 | | | | 0.1 | |
| | | | | $I_{OL}$ = 6 mA | $T_A$ = 25°C | | | 0.17 | 0.26 | |
| | | | | | SN54HCT245 | | | | 0.4 | |
| | | | | | SN74HCT245 | | | | 0.33 | |
| $I_I$ | Input Current | DIR or $\overline{OE}$ | $V_I = V_{CC}$ or 0 | $T_A$ = 25°C | | 5.5 V | | ±0.1 | ±100 | nA |
| | | | | SN54HCT245 | | | | | ±1000 | |
| | | | | SN74HCT245 | | | | | ±1000 | |
| $I_{OZ}$ | Off-State Output Current | A or B | $V_O = V_{CC}$ or 0 | $T_A$ = 25°C | | 5.5 V | | ±0.01 | ±0.5 | µA |
| | | | | SN54HCT245 | | | | | ±10 | |
| | | | | SN74HCT245 | | | | | ±5 | |
| $I_{CC}$ | Supply Current | | $V_I = V_{CC}$ or 0 | $I_O$ = 0 | $T_A$ = 25°C | 5.5 V | | | 8 | µA |
| | | | | | SN54HCT245 | | | | 160 | |
| | | | | | SN74HCT245 | | | | 80 | |
| $\Delta I_{CC}$ [1] | Supply-Current Change | | One input at 0.5 V or 2.4 V, Other inputs at 0 or VCC | $T_A$ = 25°C | | 5.5 V | | 1.4 | 2.4 | mA |
| | | | | SN54HCT245 | | | | | 3 | |
| | | | | SN74HCT245 | | | | | 2.9 | |

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over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $C_i$ (2) | Input Capacitance | DIR or $\overline{OE}$ | $T_A$ = 25°C | 4.5 V to 5.5 V | | 3 | 10 | pF |
| | | | SN54HCT245 | | | | 10 | |
| | | | SN74HCT245 | | | | 10 | |

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.
(2) Parameter $C_i$ does not apply to transceiver I/O ports.

## 6.6 Switching Characteristics: $C_L$ = 50 pF

over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see 图 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A or B | B or A | 4.5 V | $T_A$ = 25°C | | 16 | 22 | ns |
| | | | | SN54HCT245 | | | 33 | |
| | | | | SN74HCT245 | | | 28 | |
| | | | 5.5 V | $T_A$ = 25°C | | 14 | 20 | |
| | | | | SN54HCT245 | | | 30 | |
| | | | | SN74HCT245 | | | 25 | |
| $t_{en}$ | $\overline{OE}$ | A or B | 4.5 V | $T_A$ = 25°C | | 25 | 46 | ns |
| | | | | SN54HCT245 | | | 69 | |
| | | | | SN74HCT245 | | | 58 | |
| | | | 5.5 V | $T_A$ = 25°C | | 22 | 41 | |
| | | | | SN54HCT245 | | | 62 | |
| | | | | SN74HCT245 | | | 52 | |
| $t_{dis}$ | $\overline{OE}$ | A or B | 4.5 V | $T_A$ = 25°C | | 26 | 40 | ns |
| | | | | SN54HCT245 | | | 60 | |
| | | | | SN74HCT245 | | | 50 | |
| | | | 5.5 V | $T_A$ = 25°C | | 23 | 36 | |
| | | | | SN54HCT245 | | | 54 | |
| | | | | SN74HCT245 | | | 45 | |
| $t_t$ | | A or B | 4.5 V | $T_A$ = 25°C | | 9 | 12 | ns |
| | | | | SN54HCT245 | | | 18 | |
| | | | | SN74HCT245 | | | 15 | |
| | | | 5.5 V | $T_A$ = 25°C | | 8 | 11 | |
| | | | | SN54HCT245 | | | 16 | |
| | | | | SN74HCT245 | | | 14 | |


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## 6.7 Switching Characteristics: $C_L$ = 150 pF

over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see 图 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A or B | B or A | 4.5 V | $T_A$ = 25°C | | 20 | 30 | ns |
| | | | | SN54HCT245 | | | 45 | |
| | | | | SN74HCT245 | | | 38 | |
| | | | 5.5 V | $T_A$ = 25°C | | 18 | 27 | |
| | | | | SN54HCT245 | | | 41 | |
| | | | | SN74HCT245 | | | 34 | |
| $t_{en}$ | $\overline{OE}$ | A or B | 4.5 V | $T_A$ = 25°C | | 36 | 59 | ns |
| | | | | SN54HCT245 | | | 89 | |
| | | | | SN74HCT245 | | | 74 | |
| | | | 5.5 V | $T_A$ = 25°C | | 30 | 53 | |
| | | | | SN54HCT245 | | | 80 | |
| | | | | SN74HCT245 | | | 67 | |
| $t_t$ | | A or B | 4.5 V | $T_A$ = 25°C | | 17 | 42 | ns |
| | | | | SN54HCT245 | | | 63 | |
| | | | | SN74HCT245 | | | 53 | |
| | | | 5.5 V | $T_A$ = 25°C | | 14 | 38 | |
| | | | | SN54HCT245 | | | 57 | |
| | | | | SN74HCT245 | | | 48 | |

## 6.8 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per transceiver | No load | 40 | pF |

## 6.9 Typical Characteristics

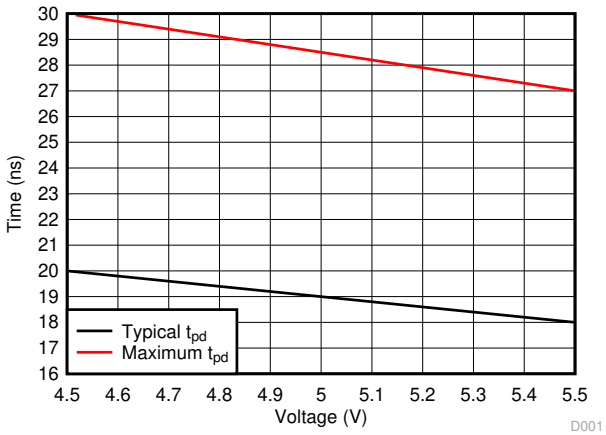


图 6-1. Propagation Delay Over Operating Voltage Range, $T_A$ = 25°C

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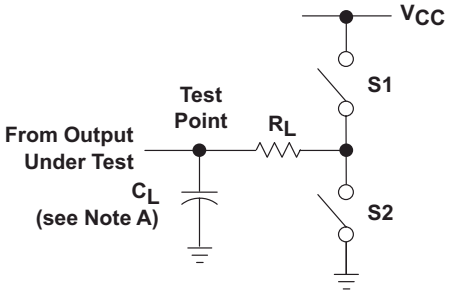
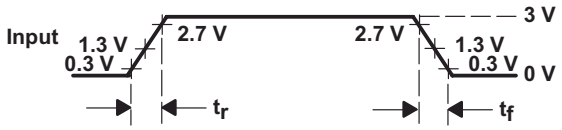
## 7 Parameter Measurement Information

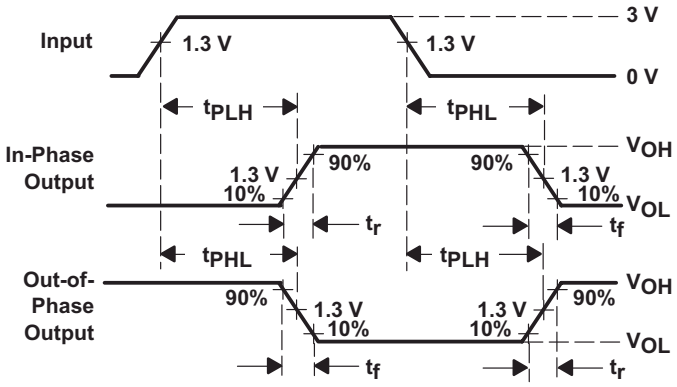



LOAD CIRCUIT

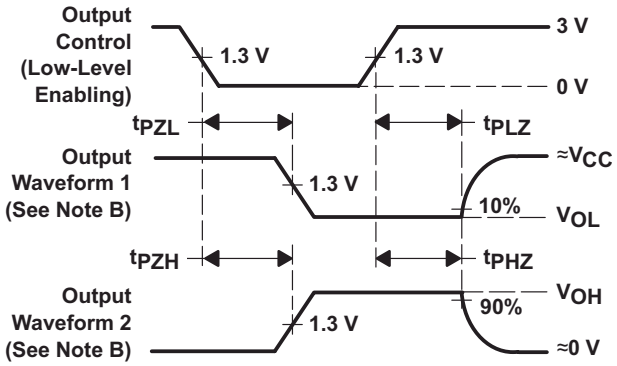
| PARAMETER | | $R_L$ | $C_L$ | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 1 kΩ | 50 pF or 150 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 1 kΩ | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | — | 50 pF or 150 pF | Open | Open |




VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**图 7-1. Load Circuit and Voltage Waveforms**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# 8 Detailed Description

## 8.1 Overview

The SNx4HCT245 is a bidirectional buffer with direction control and active low output enable. This device is commonly used in logic systems for isolation and increasing drive strength.

## 8.2 Functional Block Diagram

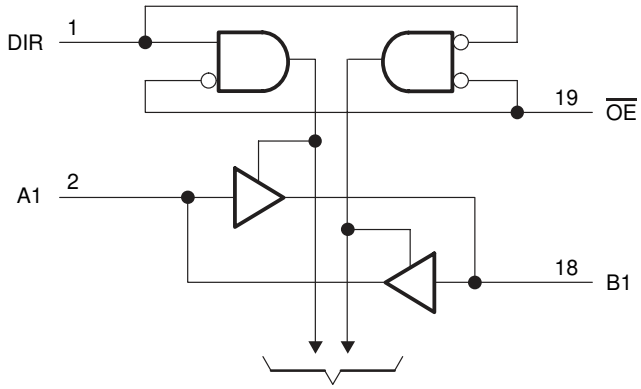


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**图 8-1. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

Voltage operating range from 4.5 V to 5.5 V is forgiving of 5-V power supply rail accuracy. Outputs can operate up to 15 LSTTL loads. This device has balanced propagation delay, typically 14 ns, and balanced output drive of ±6 mA at 5 V. It has low power consumption of only 80-µA maximum static supply current. The center $V_{CC}$ and GND pin configurations minimize high-speed switching noise. Inputs are TTL-voltage compatible.

## 8.4 Device Functional Modes

This device is a standard '245 logic function. It has an active low output enable, a direction pin, and eight communication channels.

**表 8-1. Function Table**

| INPUTS(1) | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don’t Care

# 9 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 9.1 Application Information

The SNx4HCT245 is a versatile device with many available applications. The application chosen as an example here is connecting a master and slave device through a ribbon cable. This configuration is common due to losses in this type of cable.

## 9.2 Typical Application

Logic transceivers are commonly seen in back plane and ribbon cable applications where a signal direct from an FPGA or MCU would be too weak to reach the distant end. The transceiver acts as an amplifier to get the signal across the line, and since it is bidirectional, data can be sent from master to slave or slave to master. The additional buffer on the direction line is necessary to ensure the direction signal can always reach the distant end.

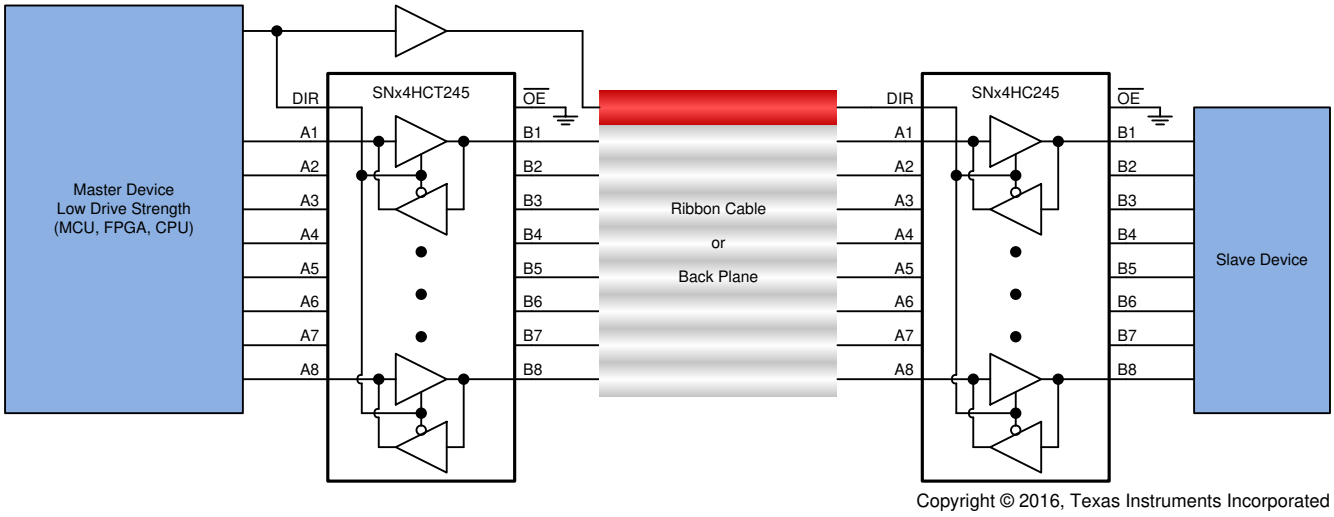


**图 9-1. Typical application for SNx4HC245**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care must be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive, but the high drive also creates faster edges into light loads, so routing and load conditions must be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See ( $\Delta t/\Delta V$) in the *Recommended Operating Conditions*.
   - Specified high and low levels: See (VIH and VIL) in the *Recommended Operating Conditions*.
2. Recommended Output Conditions
   - Load currents should not exceed 35 mA per output and 70 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.


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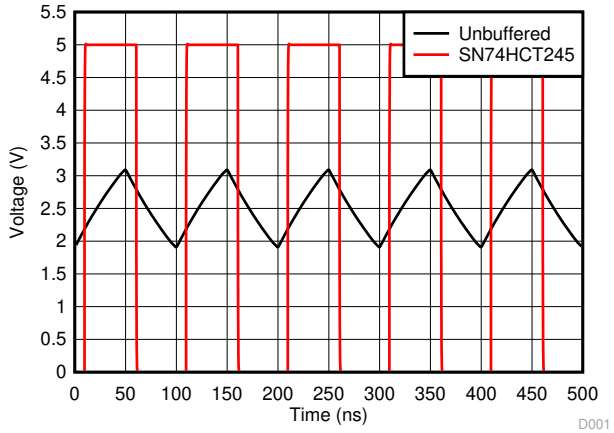
### 9.2.3 Application Curve

It is common to see significant losses in ribbon cables and back planes. The plot shown in 图 9-2 is a simplified simulation of a ribbon cable from a 5-V, 10-MHz low drive strength source. It shows the difference between an input signal from a weak driver like an MCU or FPGA compared to a strong driver like the SN74HCT245 when measured at the distant end of the cable. By adding a high-current drive transceiver before the cable, the signal strength can be significantly improved, and subsequently the cable can be longer.




Unbuffered line is directly connected to low current source, SN74HCT245 line is buffered through the transceiver. Both signals are measured at the distant end of the ribbon cable.

**图 9-2. Simulated Outputs From Ribbon Cable With a 5-V, 10-MHz Source**

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## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple VCC pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only six channels of an eight channel transceiver are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or $V_{CC}$, whichever makes more sense or is more convenient.

The output enable pin disables the output section of the part when asserted. This does not disable the input section of the IOs, so they cannot float when disabled.

图 11-1 shows the proper method to terminate unused channels using a large resistance (in this example, 10-k Ω resistors). This avoids overloading the outputs , and maintains a valid voltage on the inputs. Note that it is also valid to tie both sides of an unused transceiver directly to ground or $V_{CC}$; however, the two sides must never be tied to different states directly.

### 11.2 Layout Example

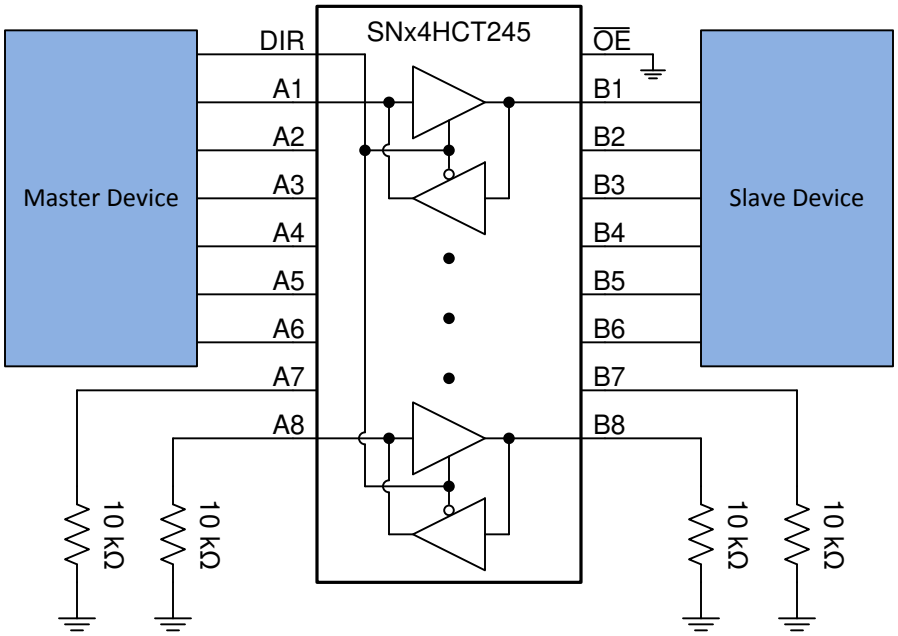


**图 11-1. Proper Termination of $\overline{OE}$ Pin And Unused Channels 7 and 8**


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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs* (SCBA004)

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 12-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54HCT245 | Click here | Click here | Click here | Click here | Click here |
| SN74HCT245 | Click here | Click here | Click here | Click here | Click here |

## 12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-8550601VRA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8550601VRA SNV54HCT245J |
| 5962-8550601VRA.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8550601VRA SNV54HCT245J |
| 5962-8550601VSA | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8550601VSA SNV54HCT245W |
| 5962-8550601VSA.A | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8550601VSA SNV54HCT245W |
| 85506012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 85506012A SNJ54HCT 245FK |
| 8550601RA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8550601RA SNJ54HCT245J |
| JM38510/65553BRA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65553BRA |
| JM38510/65553BRA.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65553BRA |
| JM38510/65553BSA | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65553BSA |
| JM38510/65553BSA.A | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65553BSA |
| M38510/65553BRA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65553BRA |
| M38510/65553BSA | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65553BSA |
| SN54HCT245J | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HCT245J |
| SN54HCT245J.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HCT245J |
| SN74HCT245DBR | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT245 |
| SN74HCT245DBR.A | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT245 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74HCT245DBRG4 | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT245 |
| SN74HCT245DGSR | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HT245 |
| SN74HCT245DGSR.A | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HT245 |
| SN74HCT245DW | Obsolete | Production | SOIC (DW) \| 20 | - | - | Call TI | Call TI | -40 to 85 | HCT245 |
| SN74HCT245DWR | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT245 |
| SN74HCT245DWR.A | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT245 |
| SN74HCT245DWRE4 | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT245 |
| SN74HCT245DWRG4 | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT245 |
| SN74HCT245N | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HCT245N |
| SN74HCT245N.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HCT245N |
| SN74HCT245NE4 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HCT245N |
| SN74HCT245NSR | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT245 |
| SN74HCT245NSR.A | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT245 |
| SN74HCT245PW | Obsolete | Production | TSSOP (PW) \| 20 | - | - | Call TI | Call TI | -40 to 85 | HT245 |
| SN74HCT245PWR | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT245 |
| SN74HCT245PWR.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT245 |
| SN74HCT245PWRE4 | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT245 |
| SN74HCT245PWRG4 | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT245 |
| SN74HCT245PWRG4.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT245 |
| SN74HCT245PWT | Obsolete | Production | TSSOP (PW) \| 20 | - | - | Call TI | Call TI | -40 to 85 | HT245 |
| SNJ54HCT245FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 85506012A SNJ54HCT 245FK |
| SNJ54HCT245FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 85506012A SNJ54HCT 245FK |
| SNJ54HCT245J | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8550601RA SNJ54HCT245J |
| SNJ54HCT245J.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8550601RA SNJ54HCT245J |
| SNJ54HCT245W | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54HCT245W |
| SNJ54HCT245W.A | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54HCT245W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HCT245, SN54HCT245-SP, SN74HCT245 :**

- Catalog : SN74HCT245, SN54HCT245
- Military : SN54HCT245
- Space : SN54HCT245-SP

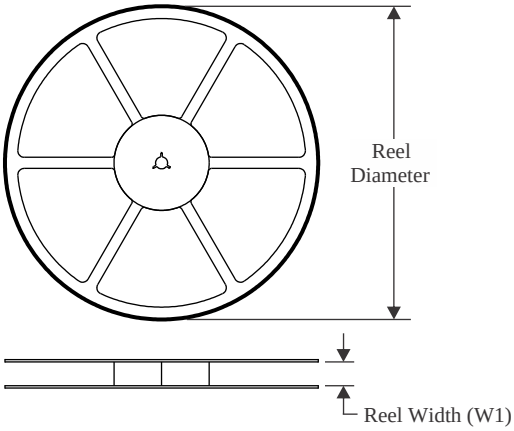
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

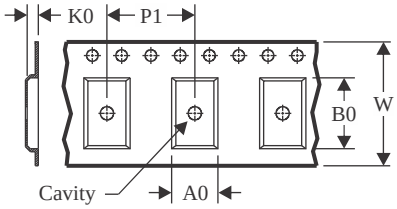
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

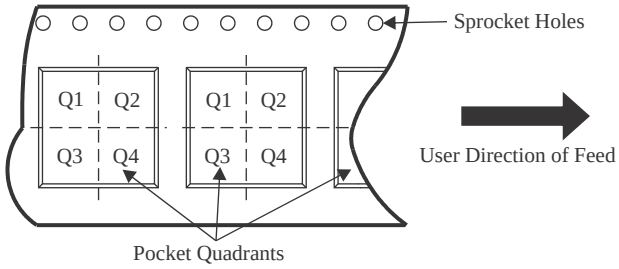



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

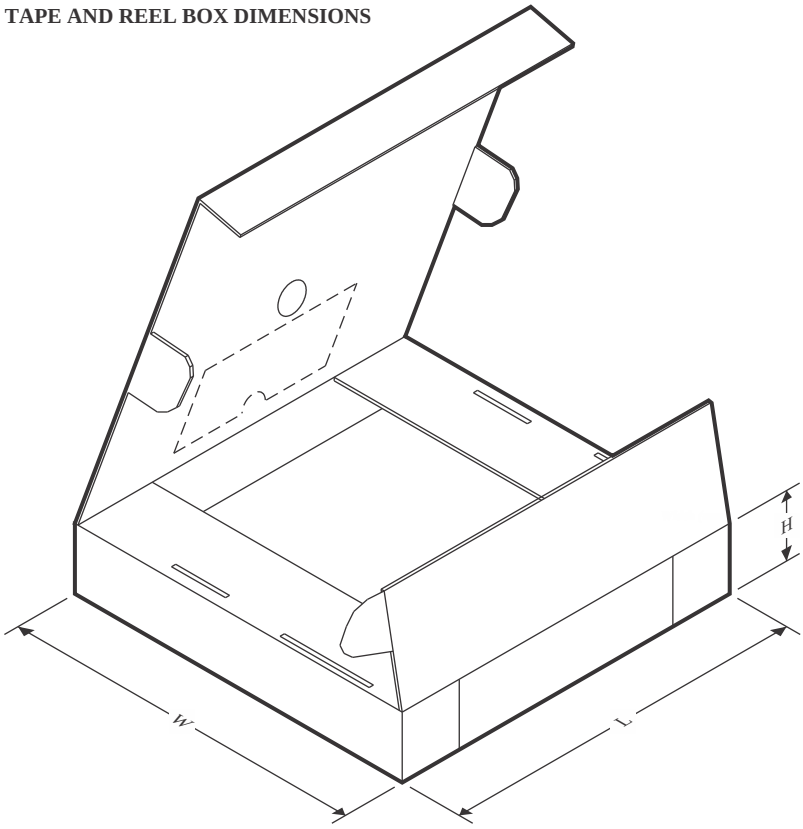
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCT245DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HCT245DGSR | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| SN74HCT245DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HCT245NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74HCT245PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74HCT245PWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

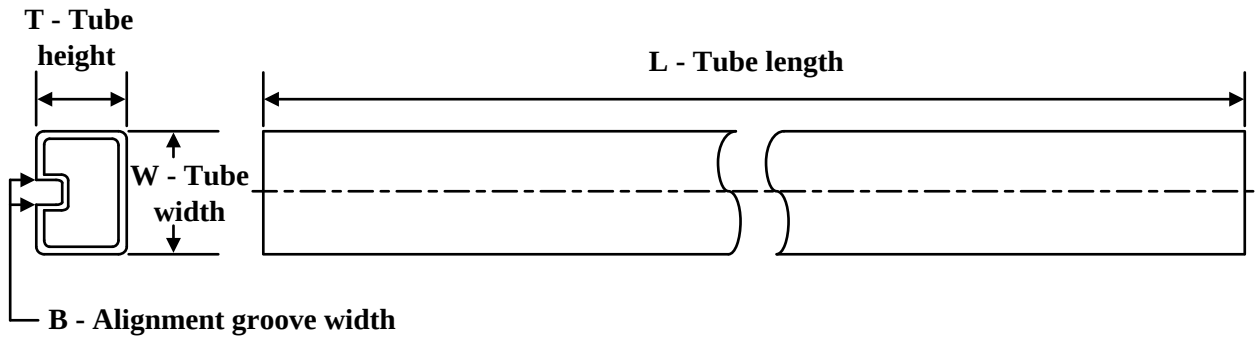
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HCT245DBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HCT245DGSR | VSSOP | DGS | 20 | 5000 | 353.0 | 353.0 | 32.0 |
| SN74HCT245DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74HCT245NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74HCT245PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HCT245PWRG4 | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |

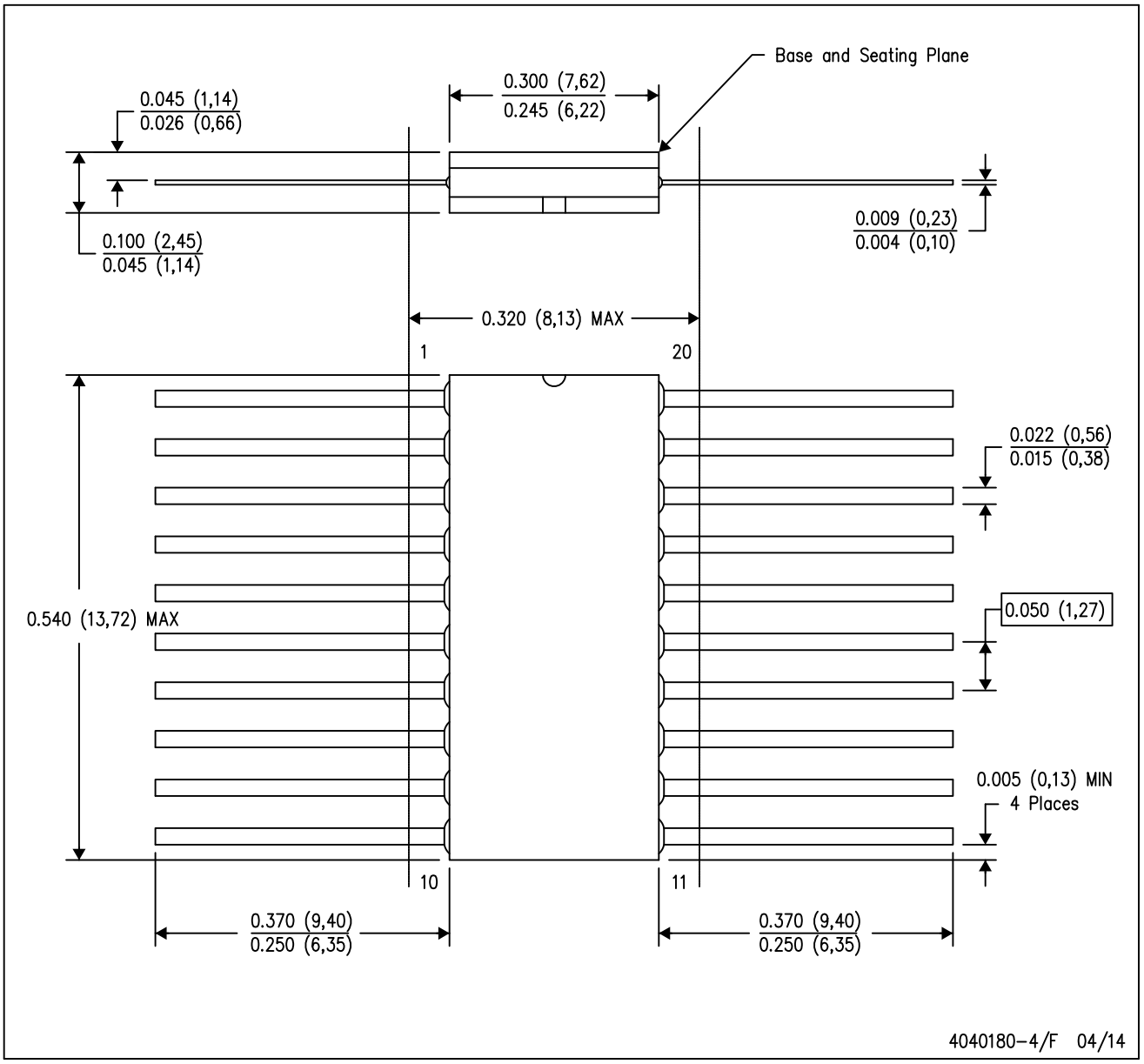
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-8550601VSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-8550601VSA.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| 85506012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/65553BSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/65553BSA.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| M38510/65553BSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74HCT245N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT245N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT245NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HCT245FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HCT245FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HCT245W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54HCT245W.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



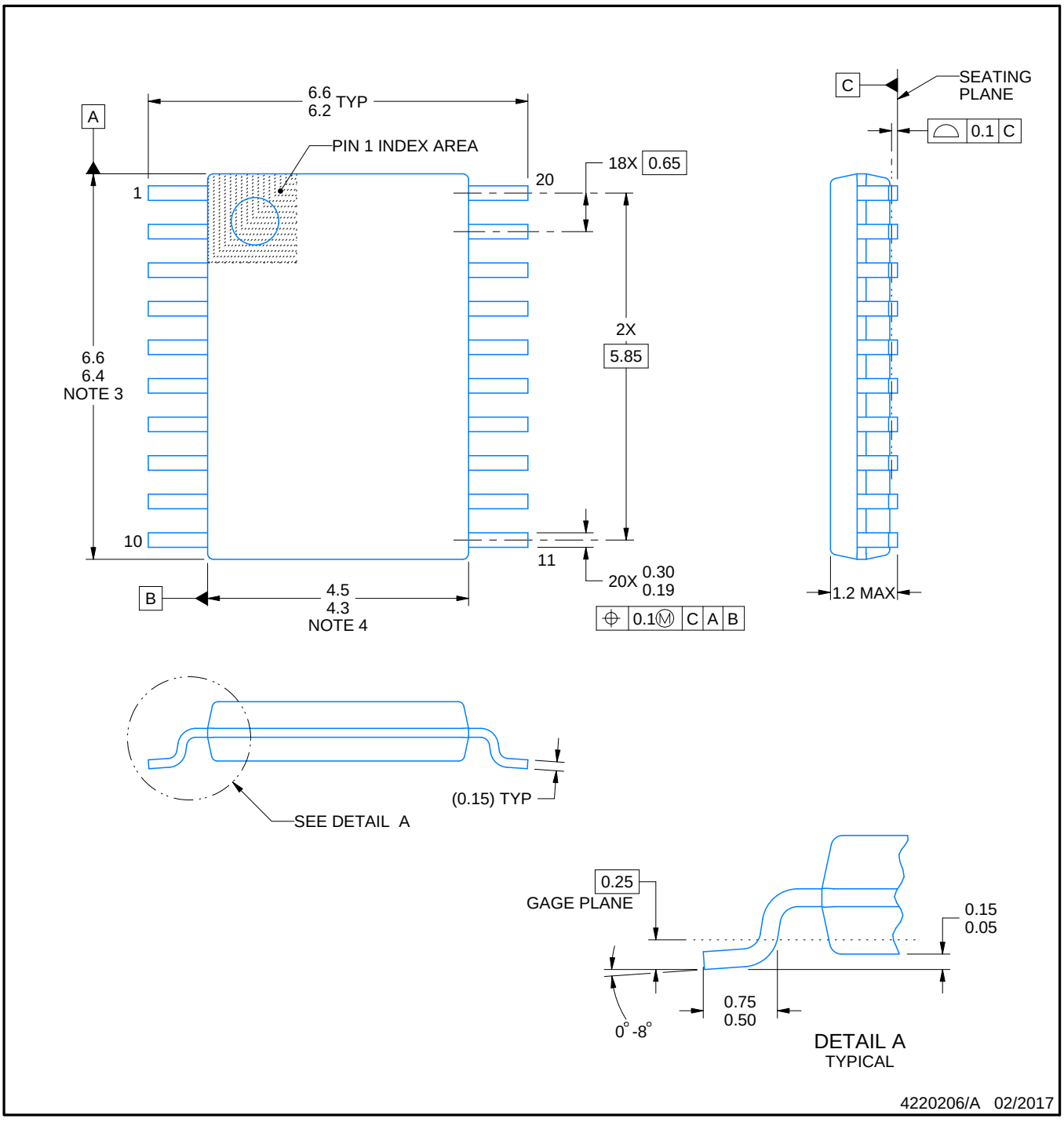

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## PW0020A

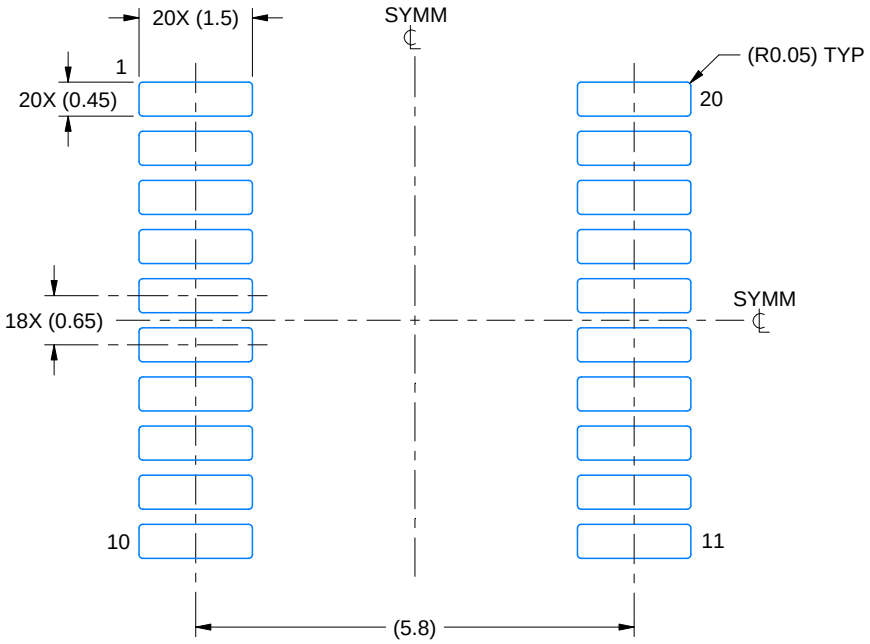
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

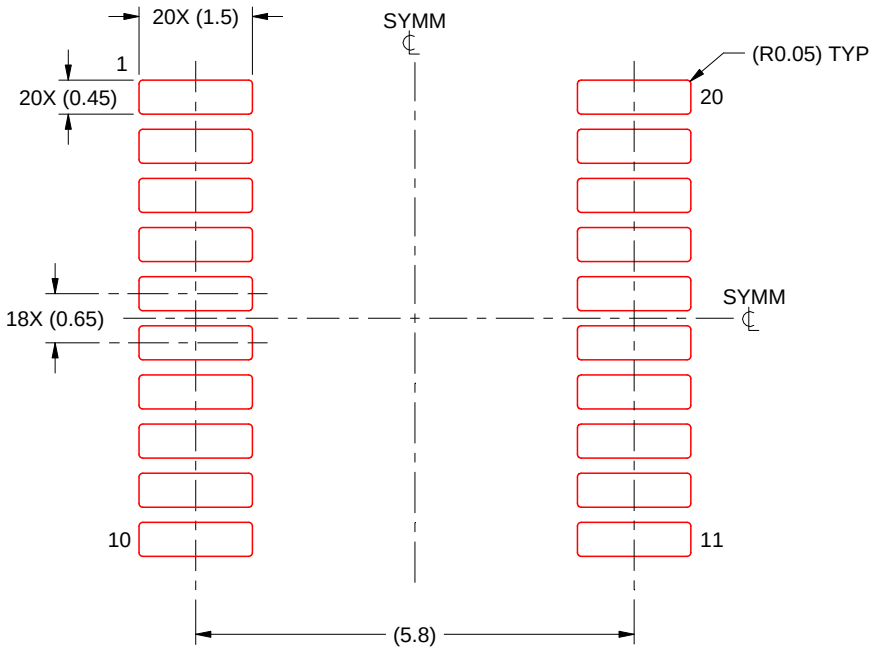
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

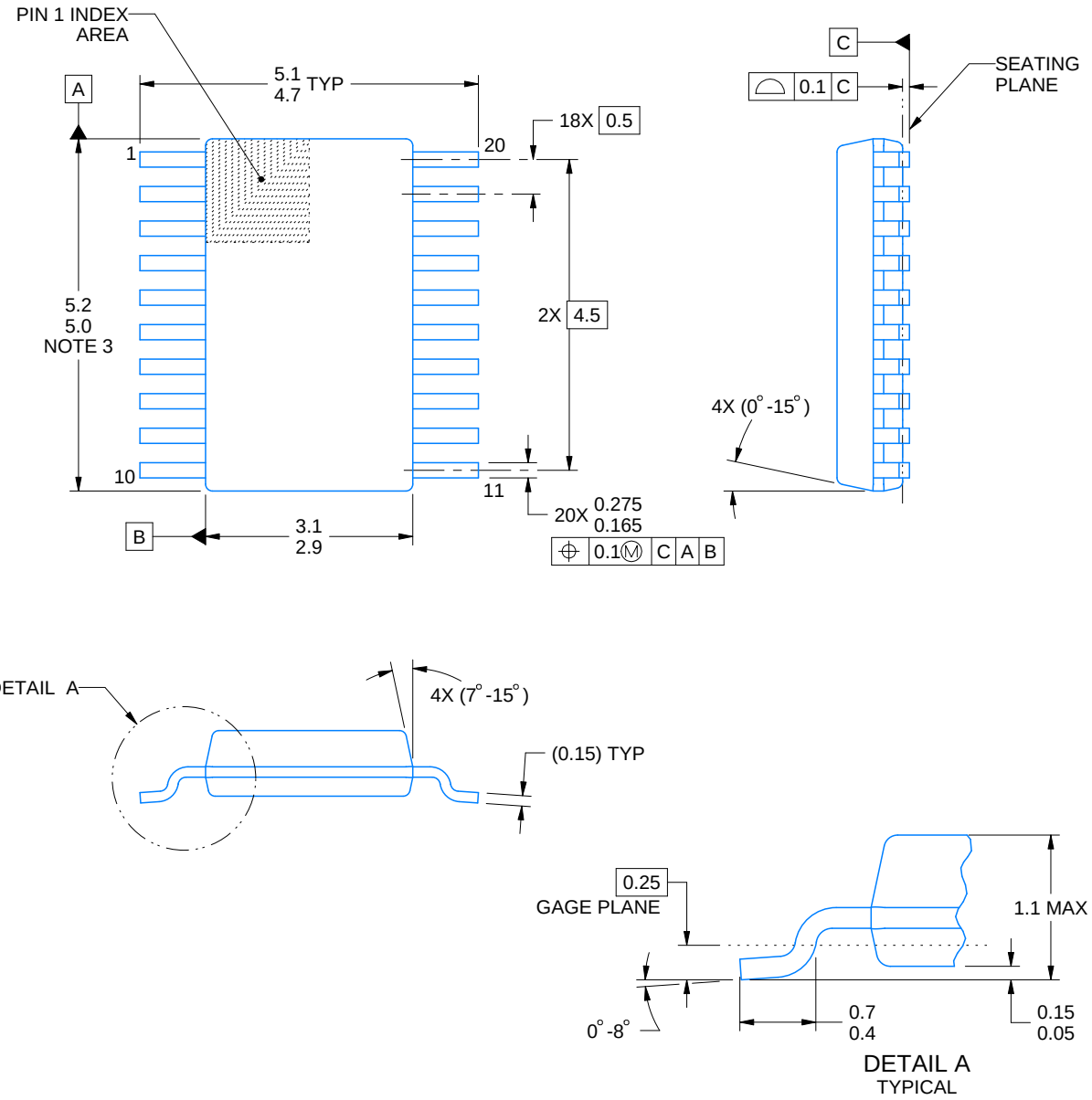
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGS0020A

## VSSOP - 1.1 mm max height

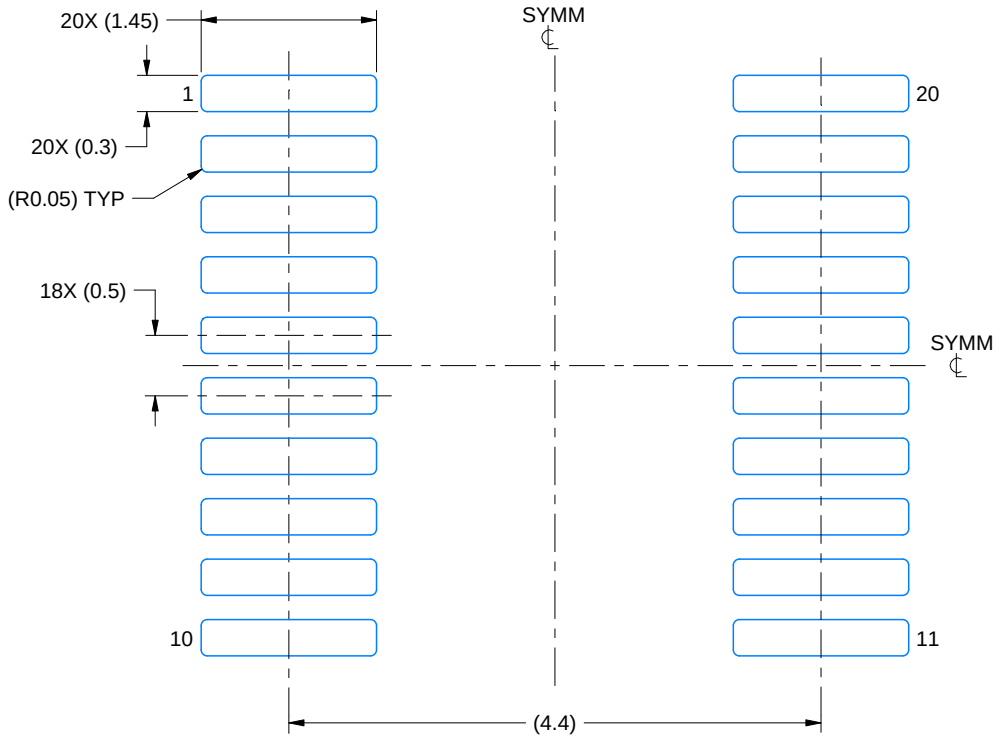
SMALL OUTLINE PACKAGE



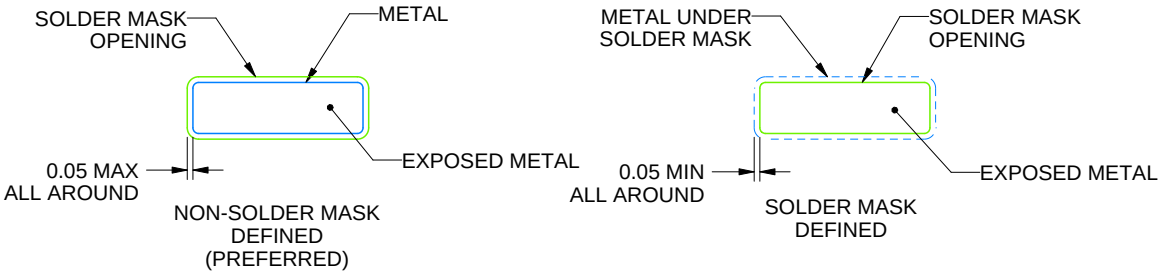

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
SCALE: 16X

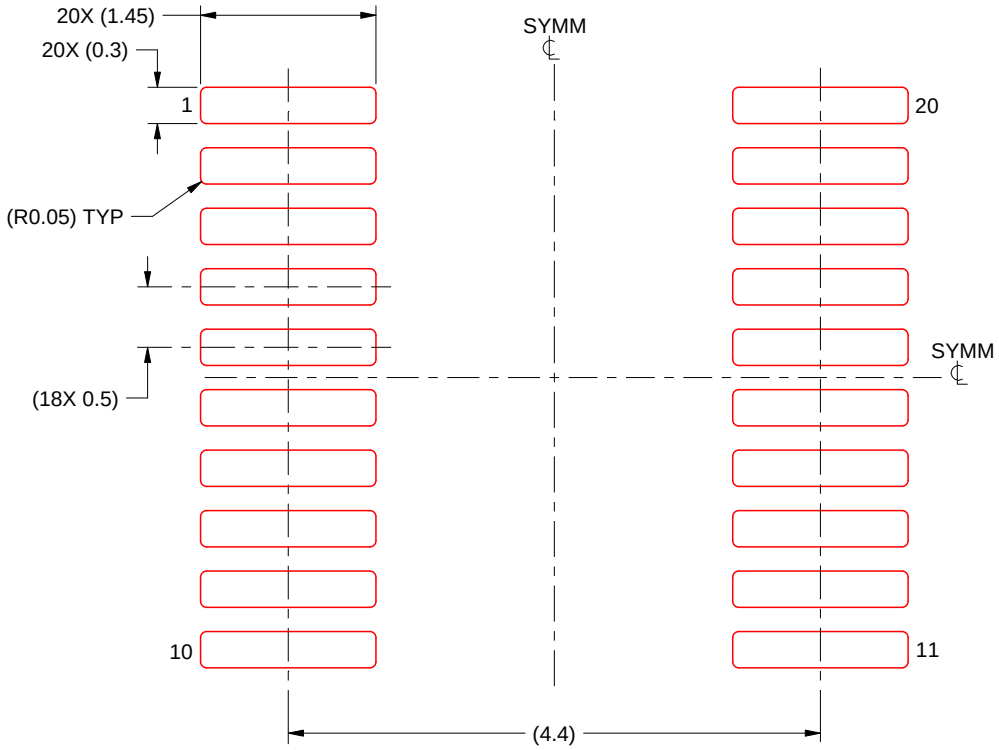



SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



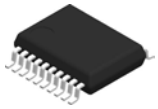

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

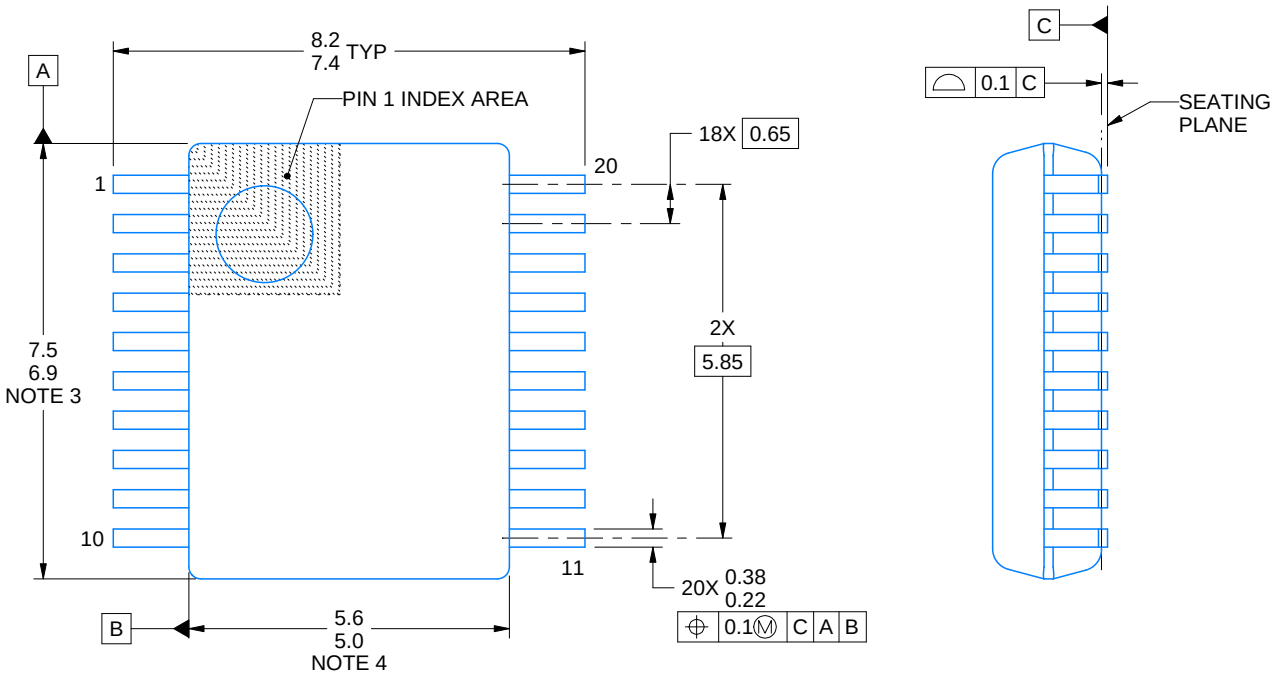
# DB0020A

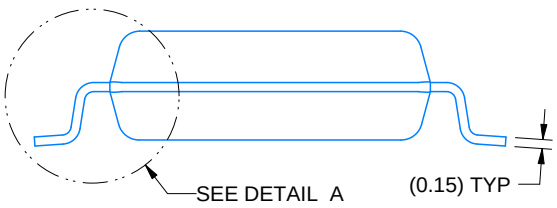


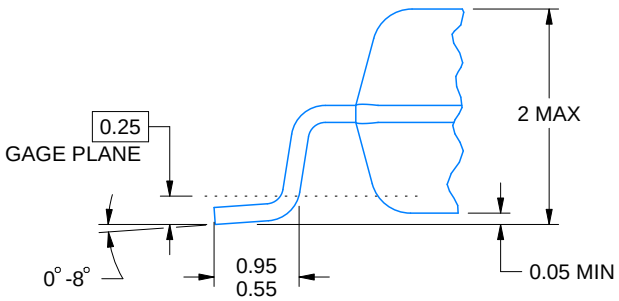
# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



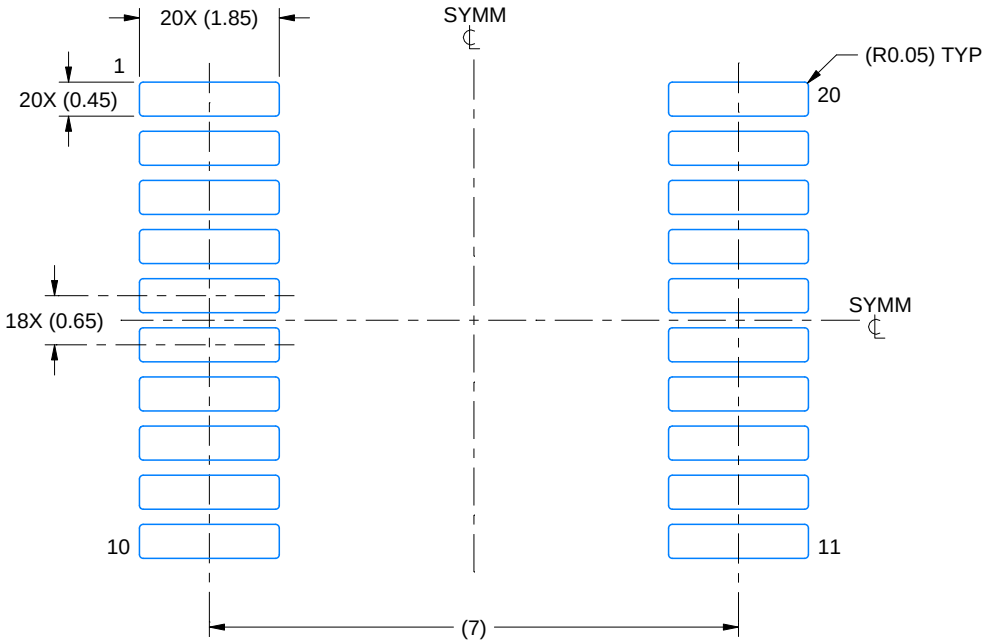




DETAIL A
TYPICAL

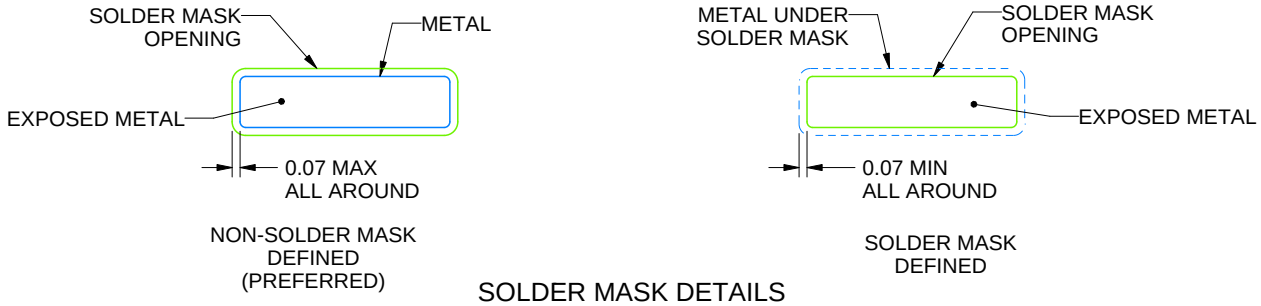
4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

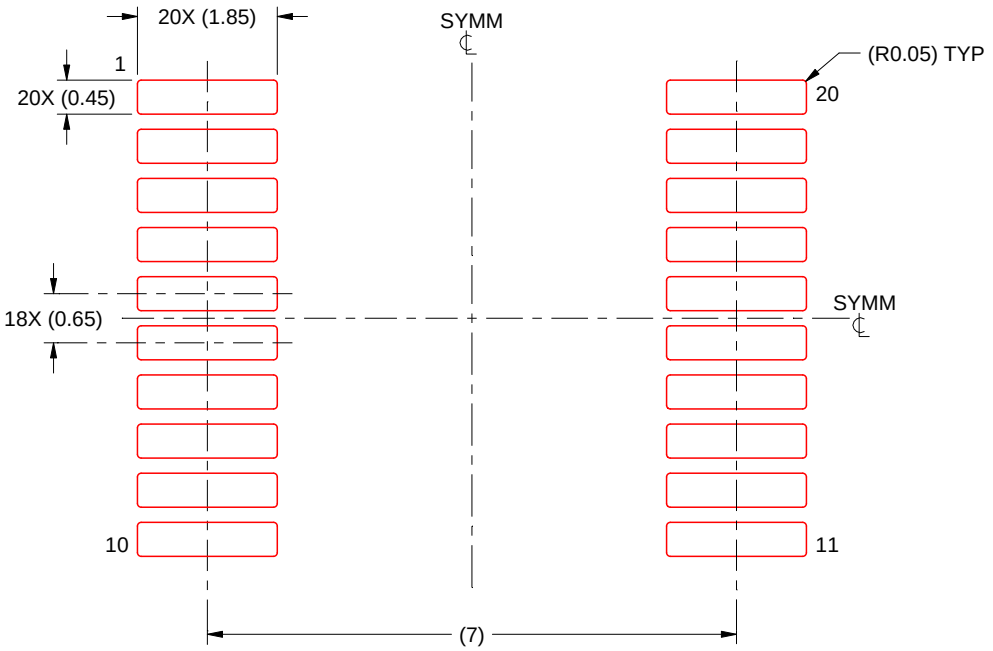
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

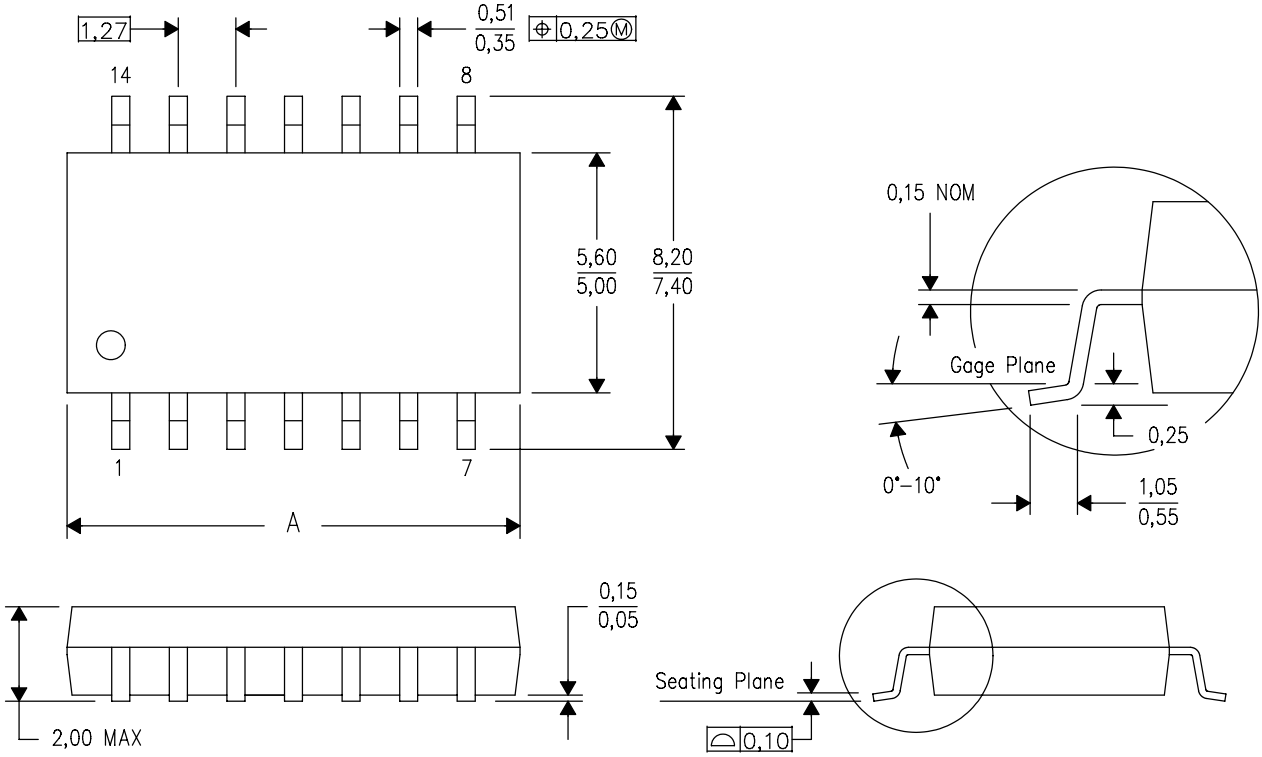
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

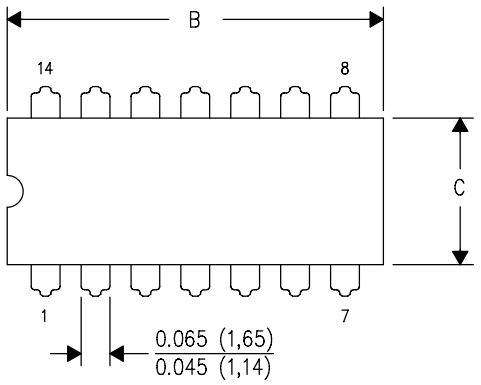
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

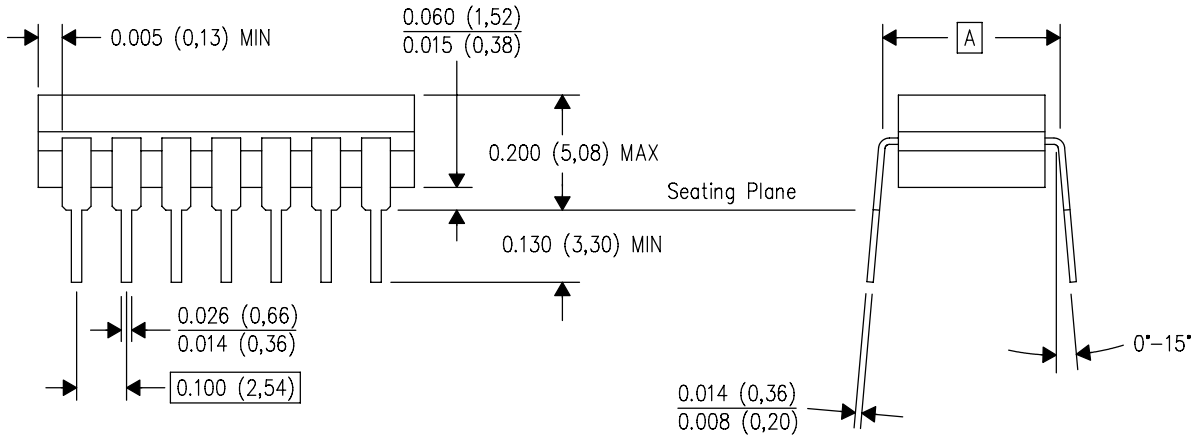
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# GENERIC PACKAGE VIEW

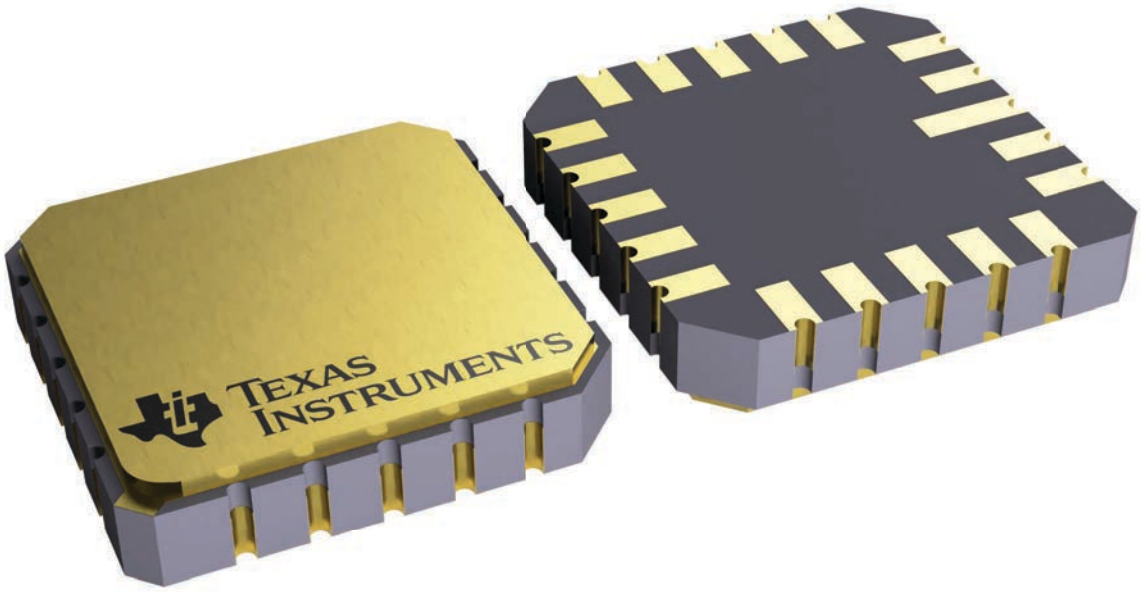
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

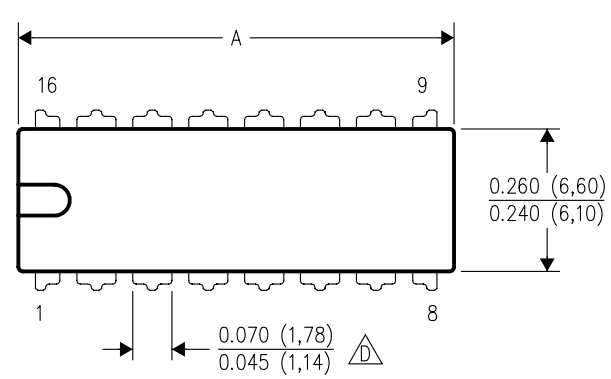



4229370VA\

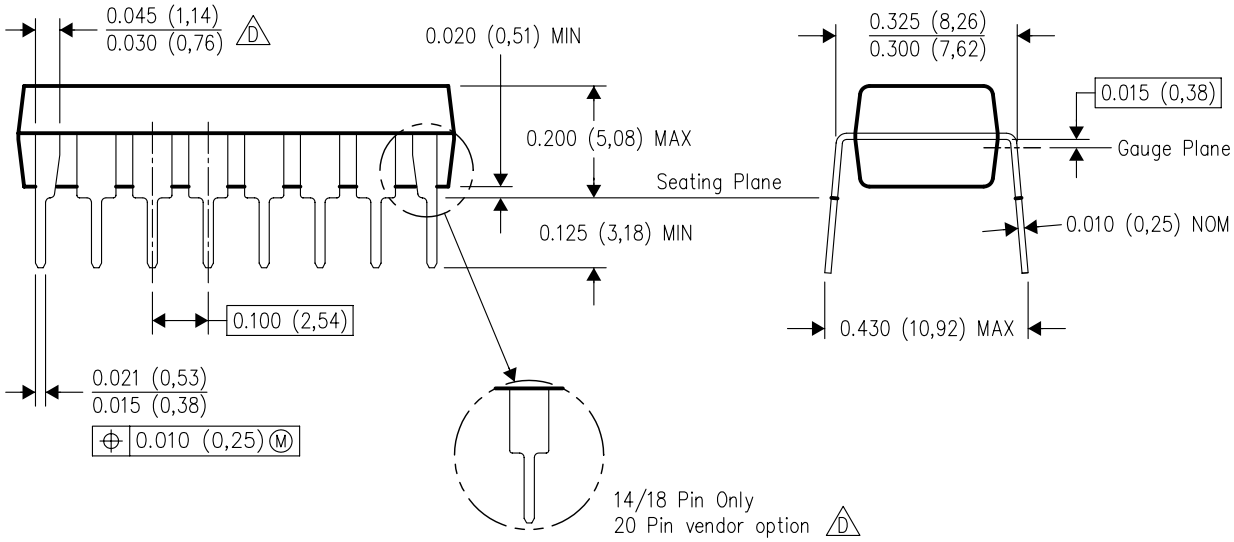
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

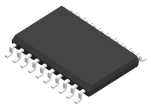



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

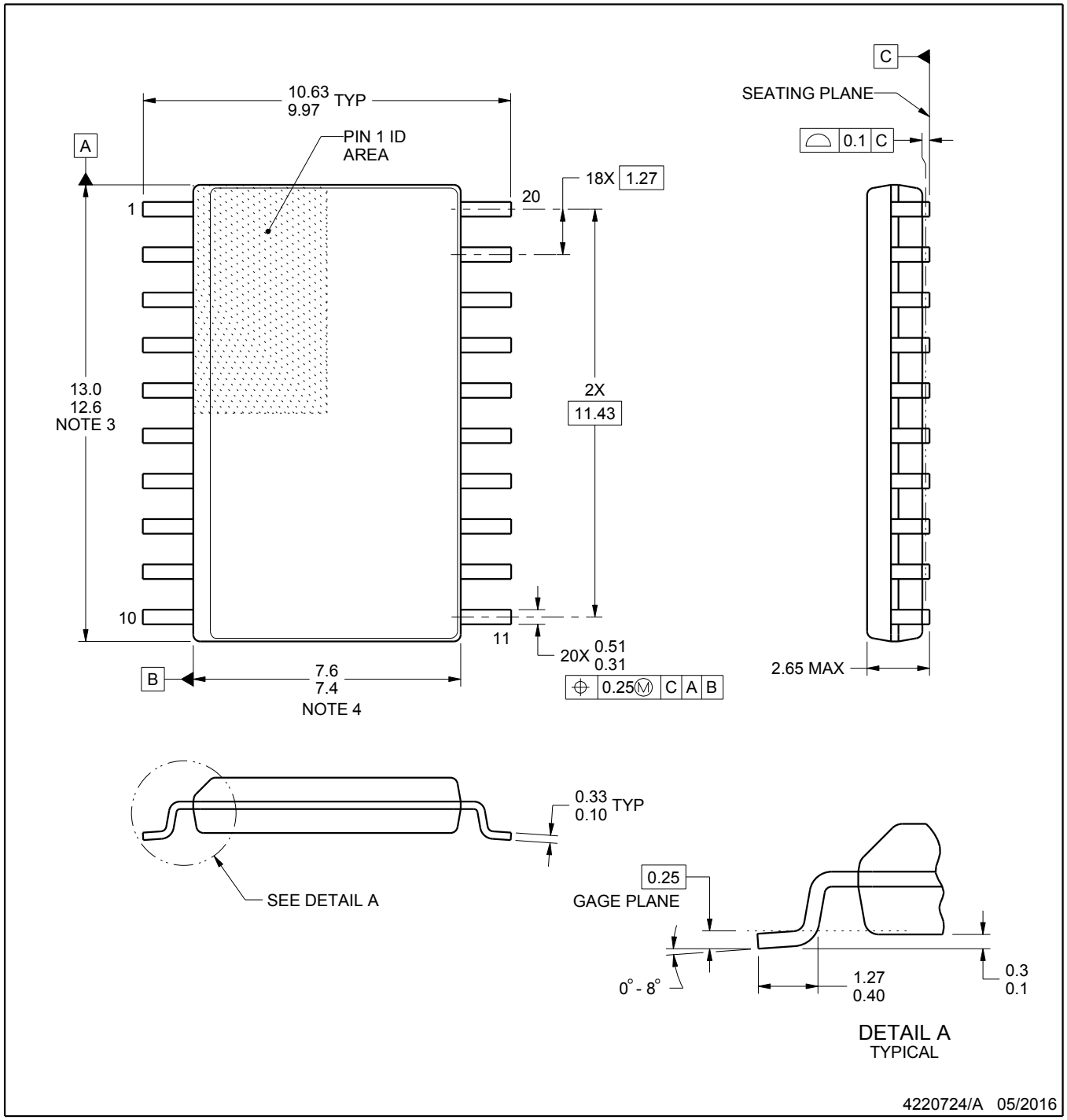


# PACKAGE OUTLINE

## DW0020A

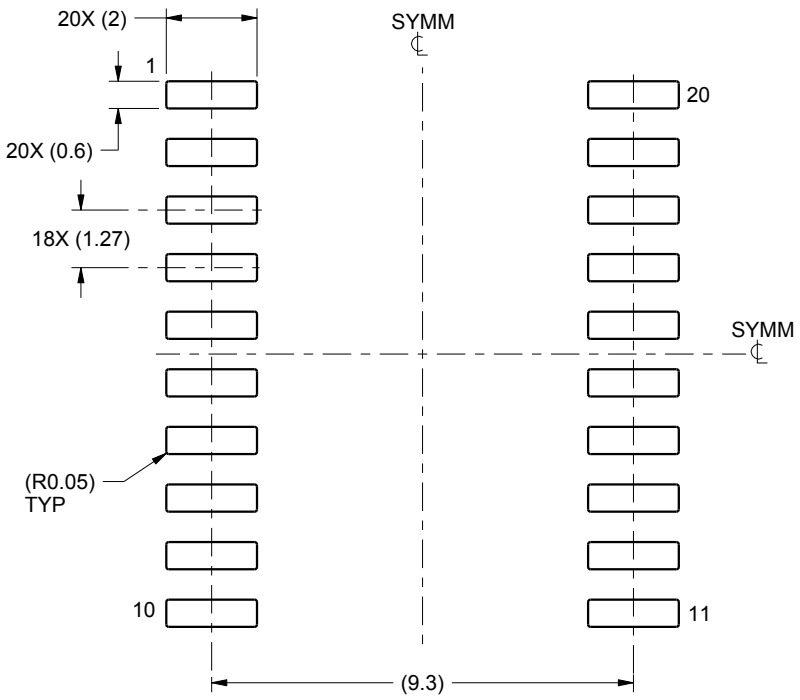
## SOIC - 2.65 mm max height

SOIC

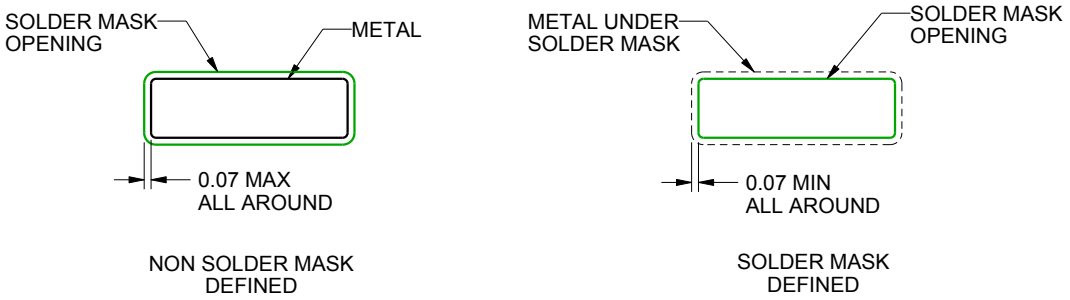



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

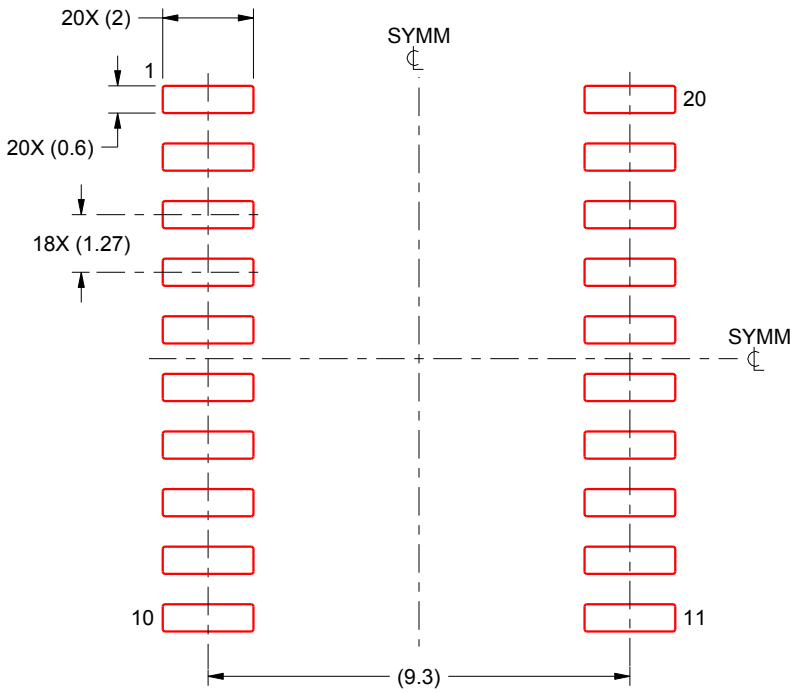



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月