3.8V-28V Vin, 3A Synchronous Step-down DCDC Converter with EMI Reduction

FEATURES

- EMI Reduction with Switching Node Ringing-free
- 400kHz Switching Frequency
- Pulse Skipping Mode PSM with 25uA Quiescent Current in Light Load Condition
- 3.8V-28V Wide Input Voltage Range
- Up to 3A Continuous Output Load Current
- 0.8V ±1% Feedback Reference Voltage
- Fully Integrated 80mΩ R_{dson} High Side MOSFET and 42mΩ R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- 4ms Built-in Soft Start Time
- Output Over Voltage Protection
- Thermal Shutdown Protection at 160°C
- Available in TSOT23-6L Package

APPLICATIONS

- White Goods, Home Appliance
- Surveillance
- Audio, WiFi Speaker
- Printer, Charging Station
- DTV, STB, Monitor/LCD Display

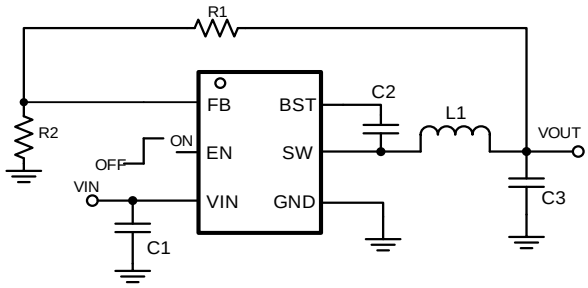
DESCRIPTION

The SCT2330C is 3A synchronous buck converters with up to 28V wide input voltage range, which fully integrates an 80mΩ high-side MOSFET and a 42mΩ low-side MOSFET to provide high efficiency step-down DC-DC conversion. The SCT2330C adopts peak current mode control with the integrated compensation network, which makes SCT2330C easily to be used by minimizing the off-chip component count. The SCT2330C supports the Pulse Skipping Modulation (PSM) with typical 25uA Ultra-Low Quiescent.

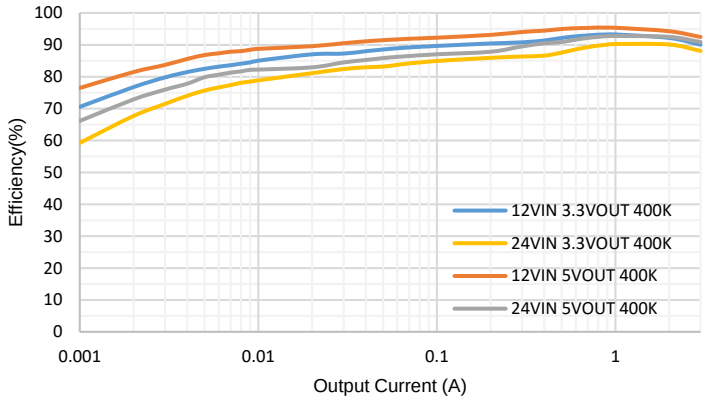
The SCT2330C is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

The SCT2330C offers output over-voltage protection, cycle-by-cycle peak current limit, and thermal shutdown protection. The device is available in a low-profile TSOT23-6 package.

TYPICAL APPLICATION



3.8V-28V, synchronous Buck Converter



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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to Market

DEVICE ORDER INFORMATION

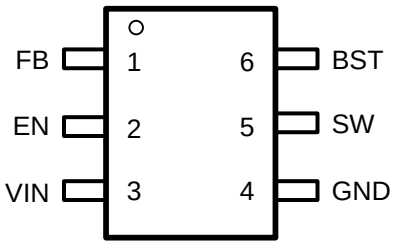
PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT2330CTVB	330C	TSOT23-6L
1) For Tape & Reel, Add Suffix R (e.g. SCT2330CTVBR)		

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	38	V
VIN, SW, EN	-0.3	32	V
FB	-0.3	5.5	V
Operating junction temperature(2)	-40	125	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: TSOT23-6L, Plastic

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
FB	1	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
EN	2	Enable logic input. Floating the pin enables the device. This pin supports high voltage input up to VIN supply to be connected VIN directly to enable the device automatically. The device has precision enable thresholds 1.18V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
VIN	3	Power supply input. Must be locally bypassed.
GND	4	Power ground. Must be soldered directly to ground plane.
SW	5	Switching node of the buck converter.

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BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	28	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	TSOT23-6L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	89	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	39	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2330C is mounted. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2330C. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.8		28	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		3.4 270		V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1	3	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V. BST-SW=5V		25		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.2		V
V_{EN_L}	Enable low threshold			1.1		V
I_{EN}	Enable pin input current	EN=1V		1		uA
I_{EN_HYS}	Enable pin hysteresis current	EN=1.5V		4.2		uA
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			80		mΩ
R_{DSON_L}	Low side FET on-resistance			42		mΩ
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage		0.792	0.8	0.808	V
Current Limit						
I_{LIM_HSD}	HSD peak current limit		4	4.5	5	A
I_{LIM_LSD}	LSD valley current limit		3.2	4	4.8	A
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V	360	400	440	kHz
t_{ON_MIN}	Minimum on-time			80		ns
t_{OFF_MIN}	Minimum off-time			100		ns
Soft Start Time						
t_{SS}	Internal soft-start time			4		ms
Protection						
V_{OVP}	Output OVP threshold Hysteresis	V_{OUT} rising		110 5		% %
T_{HIC_W}	OCP hiccup wait time			4		ms
T_{HIC_R}	OCP hiccup restart time			33		ms
T_{SD}	Thermal shutdown threshold Hysteresis	T_J rising		160 25		°C

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TYPICAL CHARACTERISTICS

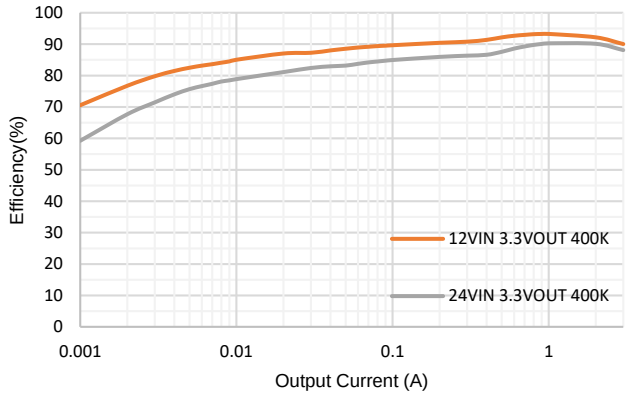

Figure 1. Efficiency vs Load Current, Vin=12V

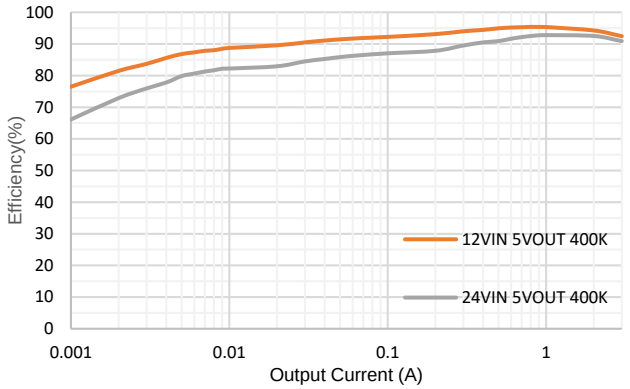

Figure 2. Efficiency vs Load Current, Vin=24V

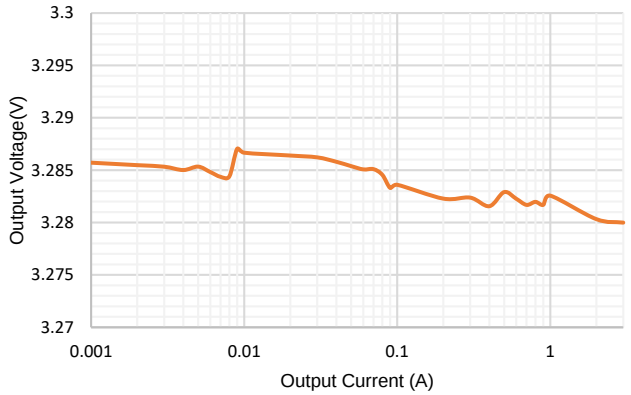

Figure 3. Load Regulation, Vin=12V, Vout=3.3V

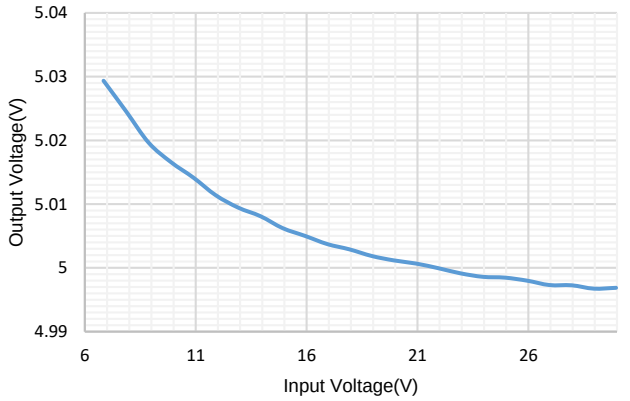

Figure 4. Line Regulation, Vout=5V, Iload=3A

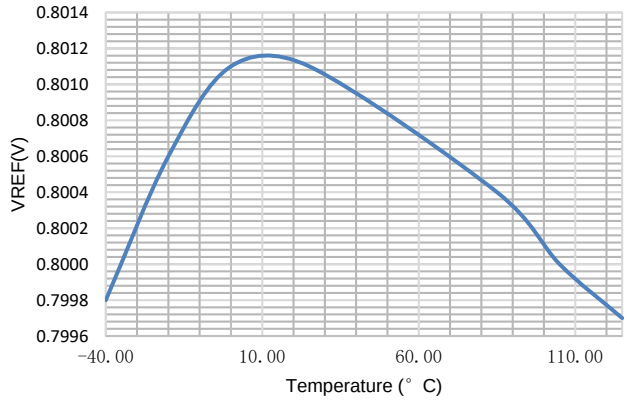

Figure 3. Reference Voltage vs Temperature

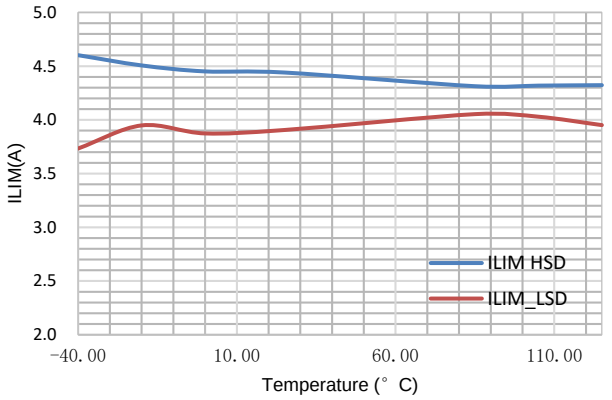

Figure 4. Current Limit vs Temperature

FUNCTIONAL BLOCK DIAGRAM

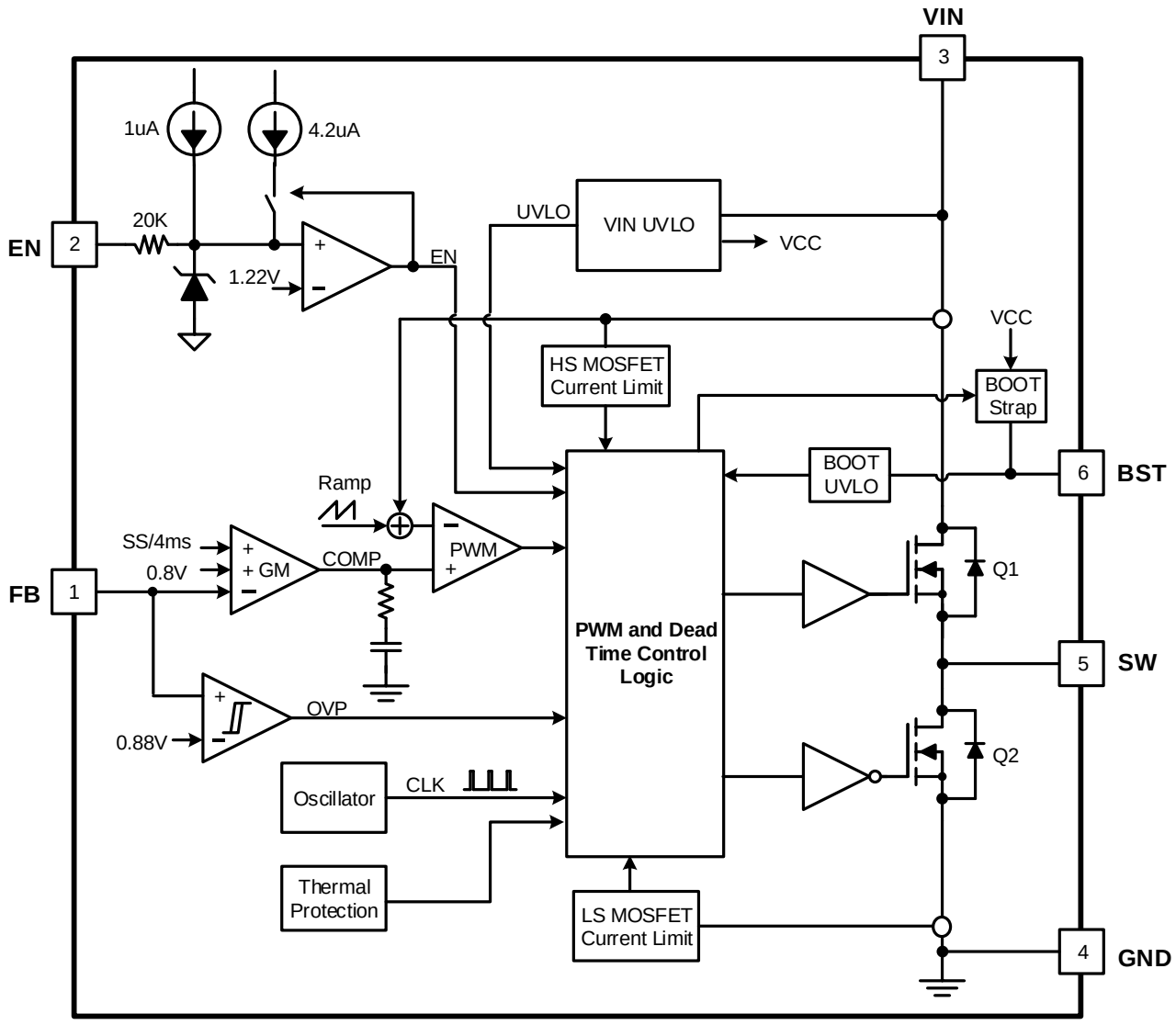

Figure7. Functional Block Diagram

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OPERATION

Overview

The SCT2330C device is 3.8V-28V input, 3A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 400kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 4ms soft-start simplify the SCT2330C footprints and minimize the off-chip component counts.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The quiescent current of SCT2330C is 25uA typical under no-load condition and no switching. When disabling the device, the supply shut down current is only 1μA. The SCT2330C works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition, hence the power efficiency can be achieved up to 86% at 5mA load condition.

The converter has optimized gate driver scheme to achieve switching node voltage ringing-free without sacrificing the MOSFET switching time to further damping high frequency radiation EMI noise.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 4ms and the hiccup restart time is 33ms. The SCT2330C device also features protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

VIN Power

The SCT2330C is designed to operate from an input voltage supply range between 3.8V to 28V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT2330C Under Voltage Lock Out (UVLO) default startup threshold is typical 3.4V with VIN rising and shutdown threshold is 3.13V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.2V/rise), the SCT2330C enables all functions and the device starts soft-start phase. The SCT2330C has the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating

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EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4.2uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 8. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

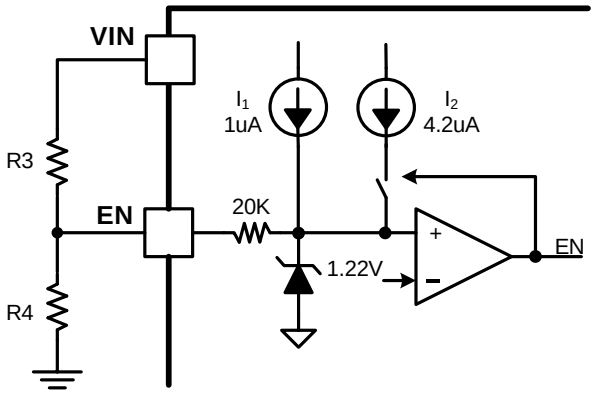

Figure 8. Adjustable VIN UVLO

$$R3 = \frac{V_{Start}\left(\frac{V_{ENF}}{V_{ENR}}\right) - V_{Stop}}{I_1\left(1 - \frac{V_{ENF}}{V_{ENR}}\right) + I_2} \quad (1)$$

$$R4 = \frac{R_3 \times V_{ENF}}{V_{Stop} - V_{ENF} + R_3(I_1 + I_2)} \quad (2)$$

Where:

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1uA
I_2=4.2uA
V_{ENR}=1.2V
V_{EMF}=1.1V

EMI Reduction with Frequency Spread Spectrum and Switching Node Ringing-free

In some applications, the system EMI test must meet EMI standards EN55011 and EN55022. To improve EMI performance, SCT2330C adopts Frequency Spread Spectrum (FSS) to spread the switching noise over a wider band and therefore reduces conducted and radiated interference peak amplitude at particular frequency. The SCT2330C features 400kHz switching frequency with spreading frequency of +/-6% and modulation rate 1/512 of switching frequency. The FSS technique effectively decreases the EMI noise by spreading the switching frequency from fixed 400kHz to a range 376kHz ~ 424Hz. As a result, the harmonic wave amplitude is reduced and the harmonic wave band is wider.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT2330C implements the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the

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converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design). The switching node zoomed in wave form is shown in Figure 9.

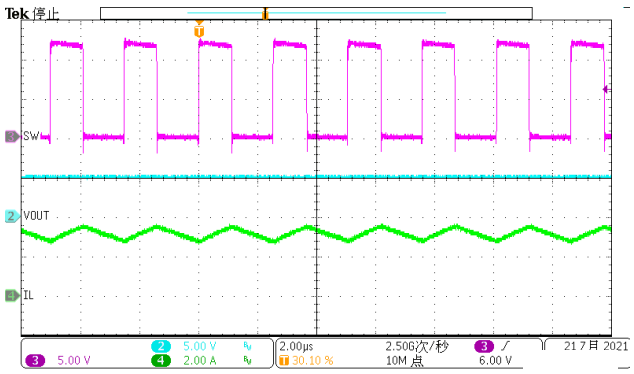

Figure 9. SCT2330C Switching Node Waveform

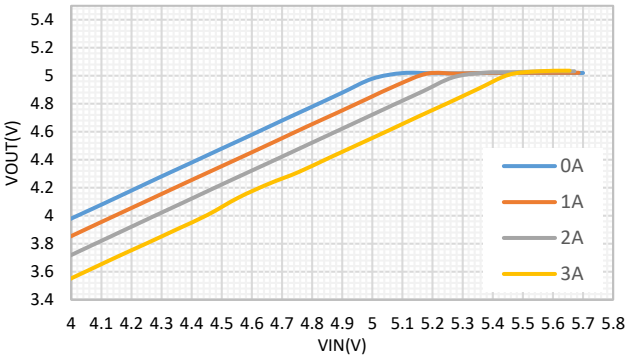

Figure 10. SCT2330C LDO Mode Waveform

Peak Current Limit and Hiccup Mode

The SCT2330C has cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

Over Voltage Protection and Minimum On-time

Both SCT2330C features buck converter output over voltage protection (OVP). If the output feedback pin voltage exceeds110% of feedback reference voltage (0.8V), the converter stops switching immediately. When the output feedback pin voltage drops below 105% of feedback reference voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 80ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

PSM Working Modes

In heavy load condition, the SCT2330C forces the device operating at forced Pulse Width Modulation (PWM) mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 480mA peak inductor current. When the load current approaches zero, the SCT2330C enter Pulse Skipping Mode (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

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Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT2330C intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Low Drop-out Regulation

To support the application of small voltage-difference between Vout and Vin, the Low Drop Out (LDO) Operation is implemented by the SCT2330C. When VIN is close to output voltage and minimum off time is triggered, switching on time will be extended to avoid output voltage drops, switching frequency will decrease accordingly. After maximum On-time (Typ.25μs) is triggered, SW will be in max duty cycle (Typ. 99.5%) operation. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high as shown in Figure 10.

During ultra-low voltage difference of input and output voltages, i.e. the input voltage ramping down to power down, the output can track input closely thanks to LDO operation mode.

The minimum operating frequency limit of about 40KHz can also effectively prevent audio noise interference caused by switching frequency when working with large duty cycle**.**

Thermal Shutdown

Once the junction temperature in the SCT2330C exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 135°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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APPLICATION INFORMATION

Typical Application

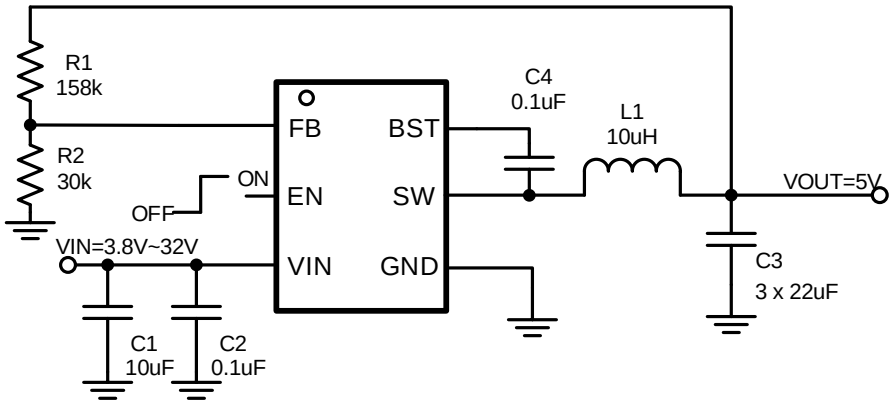

Figure 11. 24V Input, 5V/3A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	24V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	±8mV
Switching Frequency	400kHz

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Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor anda0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2330C.

Use Equation (3) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

$$L_{INDMIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (4)$$

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation (5).

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} \quad (5)$$

Set the current limit of the SCT2330C higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core

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loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Output Capacitor Selection

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor, for example, X5R and X7R family. Typically, 1～3x 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's de-rating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

From the required output voltage ripple, use the equation (6) to calculate the minimum required effective capacitance, C_{OUT}.

$$C_{OUT} = \frac{\Delta I_{LPP}}{8 \times V_{OUTRipple} \times f_{SW}} \quad (6)$$

Where

- $V_{OUTRipple}$ is output voltage ripple caused by charging and discharging of the output capacitor.
- ΔI_{LPP} is the inductor peak to peak ripple current, equal to k_{IND} * I_{OUT}.
- f_{SW} is the converter switching frequency.

The allowed maximum ESR of the output capacitor is calculated by the equation (7).

$$R_{ESR} = \frac{V_{OUTRipple}}{\Delta I_{LPP}} \quad (7)$$

The output capacitor affects the crossover frequency f_C. Considering the loop stability and effect of the internal loop compensation parameters, choose the crossover frequency less than 55 kHz ($\frac{1}{10} \times f_{SW}$) without considering the feed-forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor is shown in equation (8), assuming C_{OUT} has small ESR.

$$C_{OUT} > \frac{18k \times G_M \times G_{MP} \times 0.8V}{2\pi \times V_{OUT} \times f_C} \quad (8)$$

Where

- G_M is the transfer conductance of the error amplifier (300uS).
- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{COUTRMS} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_{IND} \cdot f_{SW}} \quad (9)$$

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Output Feed-Forward Capacitor Selection

The SCT2330C has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C_{ff} is used to boost the phase margin at the converter cross-over frequency f_c. Equation (10) is used to calculate the feed-forward capacitor.

$$C_{ff} = \frac{1}{2\pi \cdot f_C \times R_1} \quad (10)$$

Output Feedback Resistor Divider Selection

The SCT2330C features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure15. Use equation (11) to calculate the resistor divider values.

$$R_1 = \frac{(V_{OUT} - V_{ref}) \times R_2}{V_{ref}} \quad (11)$$

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.

Table 1. Recommended External Components

Vout	L1	COUT	R1	R2
3.3V	6.5uH	3*22uF	93.5k	30k
5V	10uH	3*22uF	158k	30k
12V	22uH	3*22uF	422k	30k

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Application Waveforms (VIN=24V,VOUT=5V)

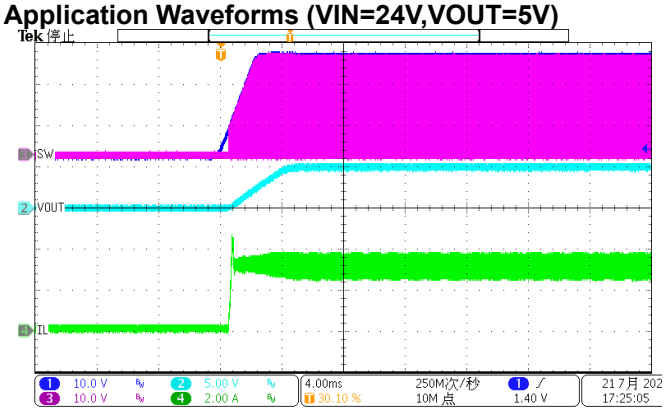

Figure 12. Power Up, IOUT=3A

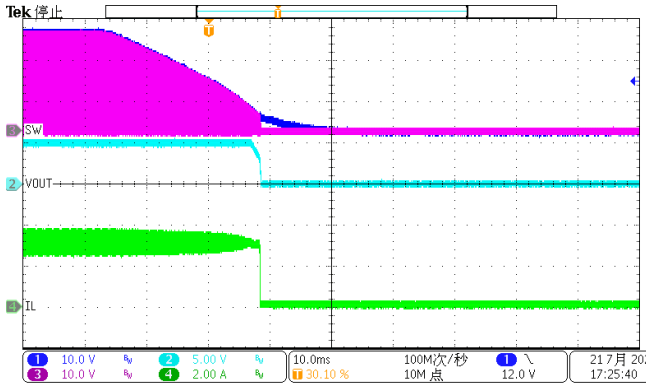

Figure 13. Power Down, IOUT=3A

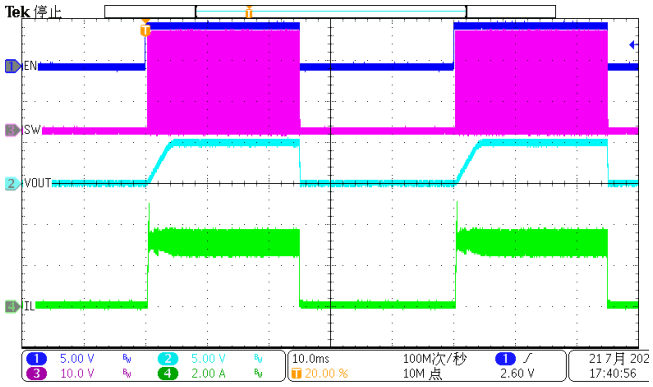

Figure 14. EN Toggle, IOUT=3A

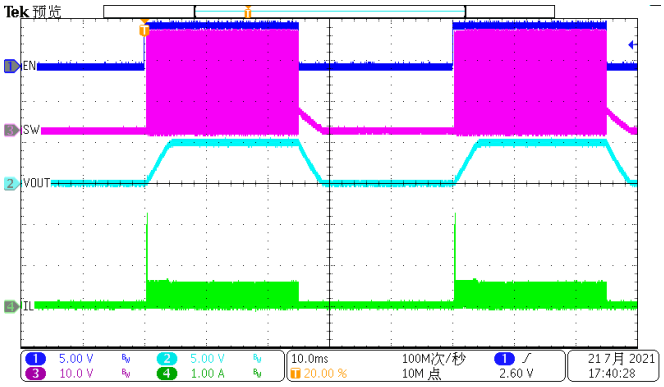

Figure 15. EN Toggle, IOUT=0.1A

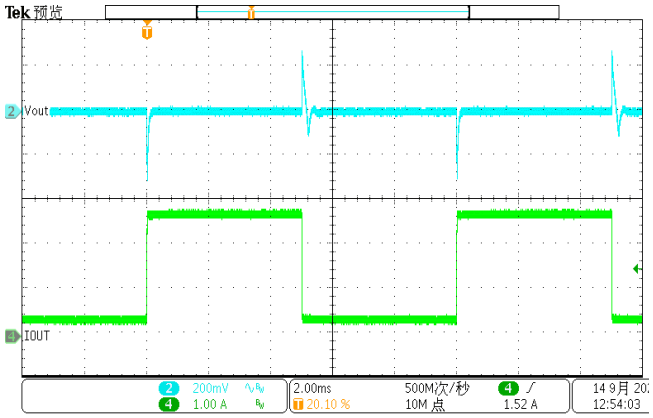

Figure 16. Load Transient
IOUT=0.3A to 2.7A, SR=1600mA/us

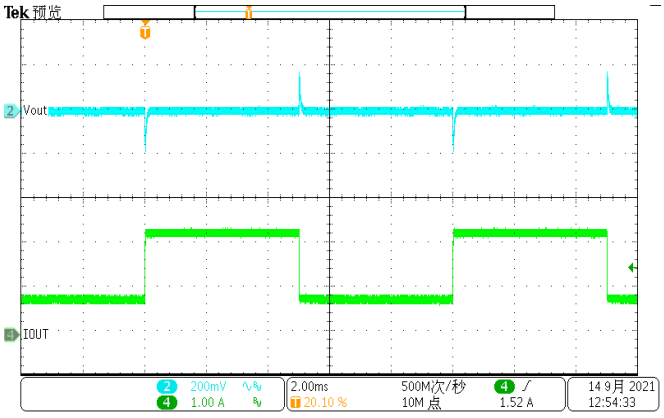

Figure 17. Load Transient
IOUT=0.75A to 2.25 A, SR=1600mA/us

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Application Waveforms (Continued)

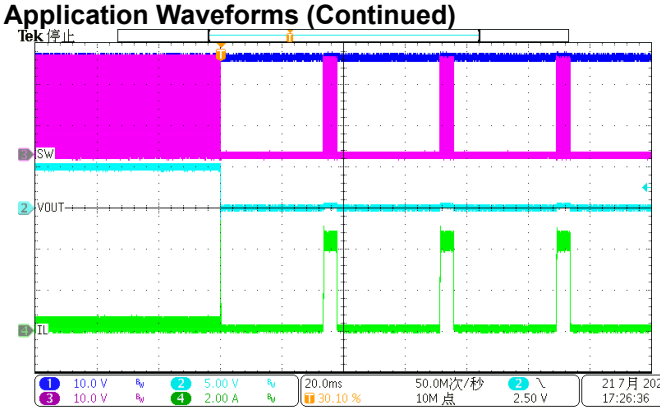

Figure 18. Over Current Protection(0A to hard short)

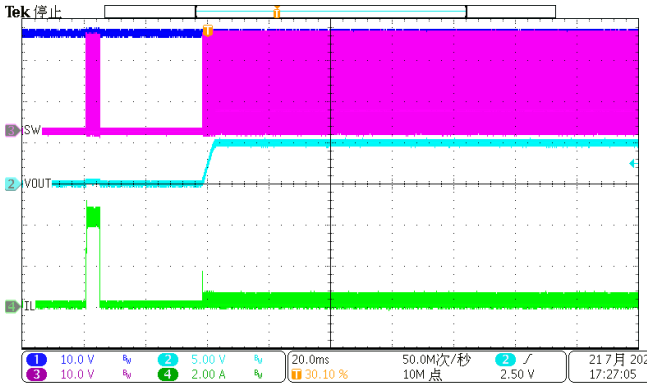

Figure 19. Over Current Release (hard short to 0A)

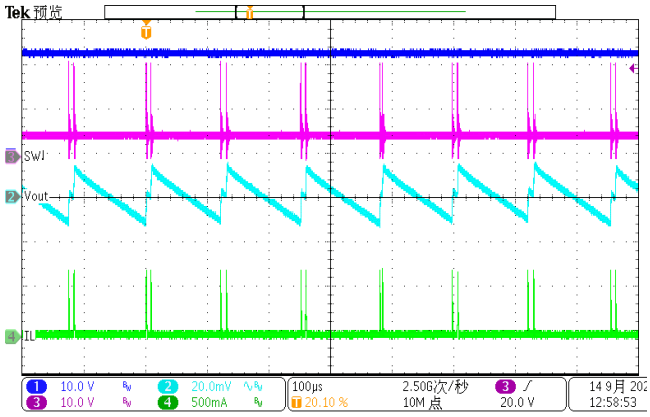

Figure 20. Output Ripple (Iload=10mA)

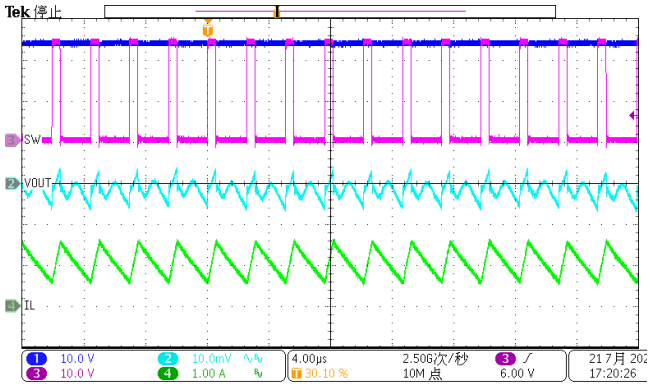

Figure 21. Output Ripple (Iload=1A)

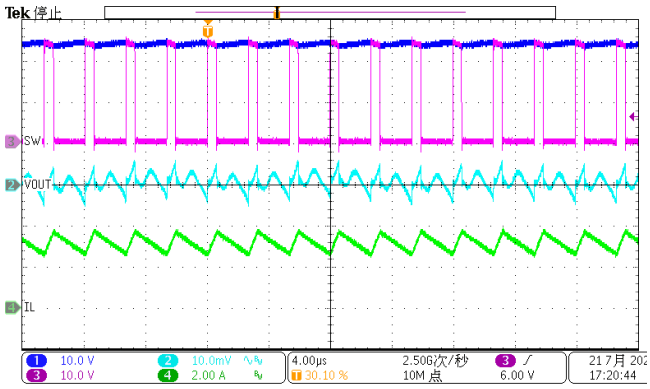

Figure 22. Output Ripple (Iload=3A)

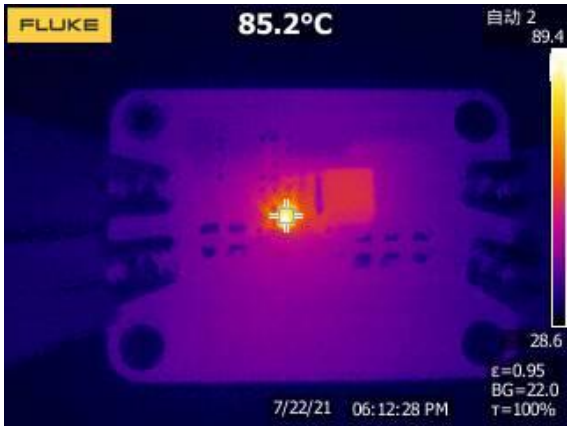

Figure 23. Thermal, 24VIN, 5Vout, 3A

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Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 24 is the recommended PCB layout of SCT2330C.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

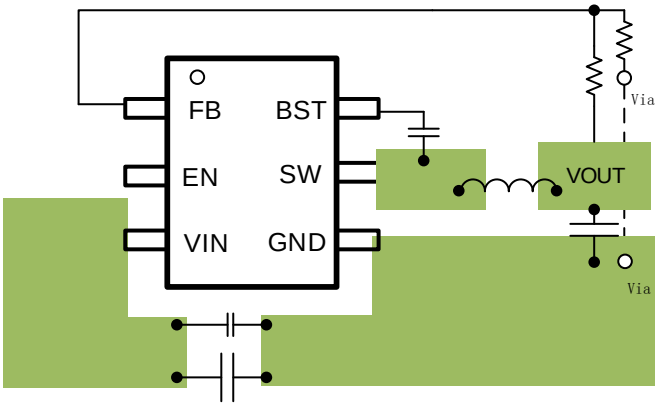

Figure 24. PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (12).

$$P_{D(MAX)} = \frac{125 - T_A}{R_{\theta JA}} \quad (12)$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

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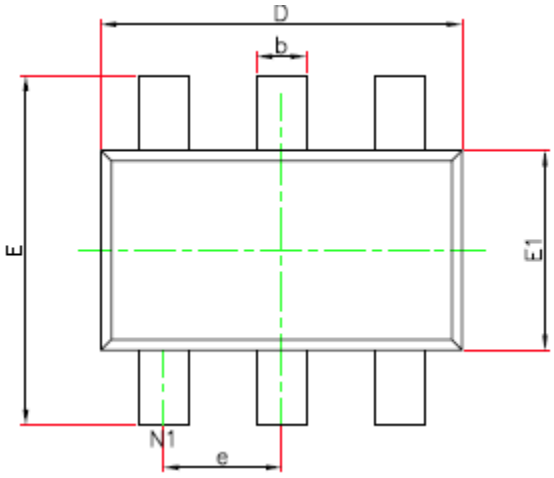
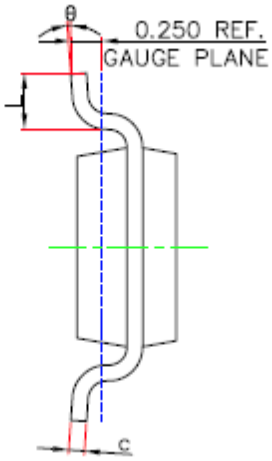
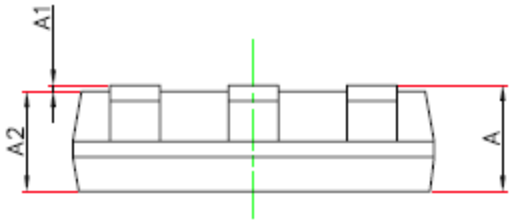
PACKAGE INFORMATION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	-------		1.10
A1	0.000		0.10
A2	0.70		1.00
D	2.85		2.95
E	2.65		2.95
E1	1.55		1.65
b	0.30		0.50
c	0.08		0.20
e	0.95(BSC)		
L	0.30		0.60
θ	0°		8°

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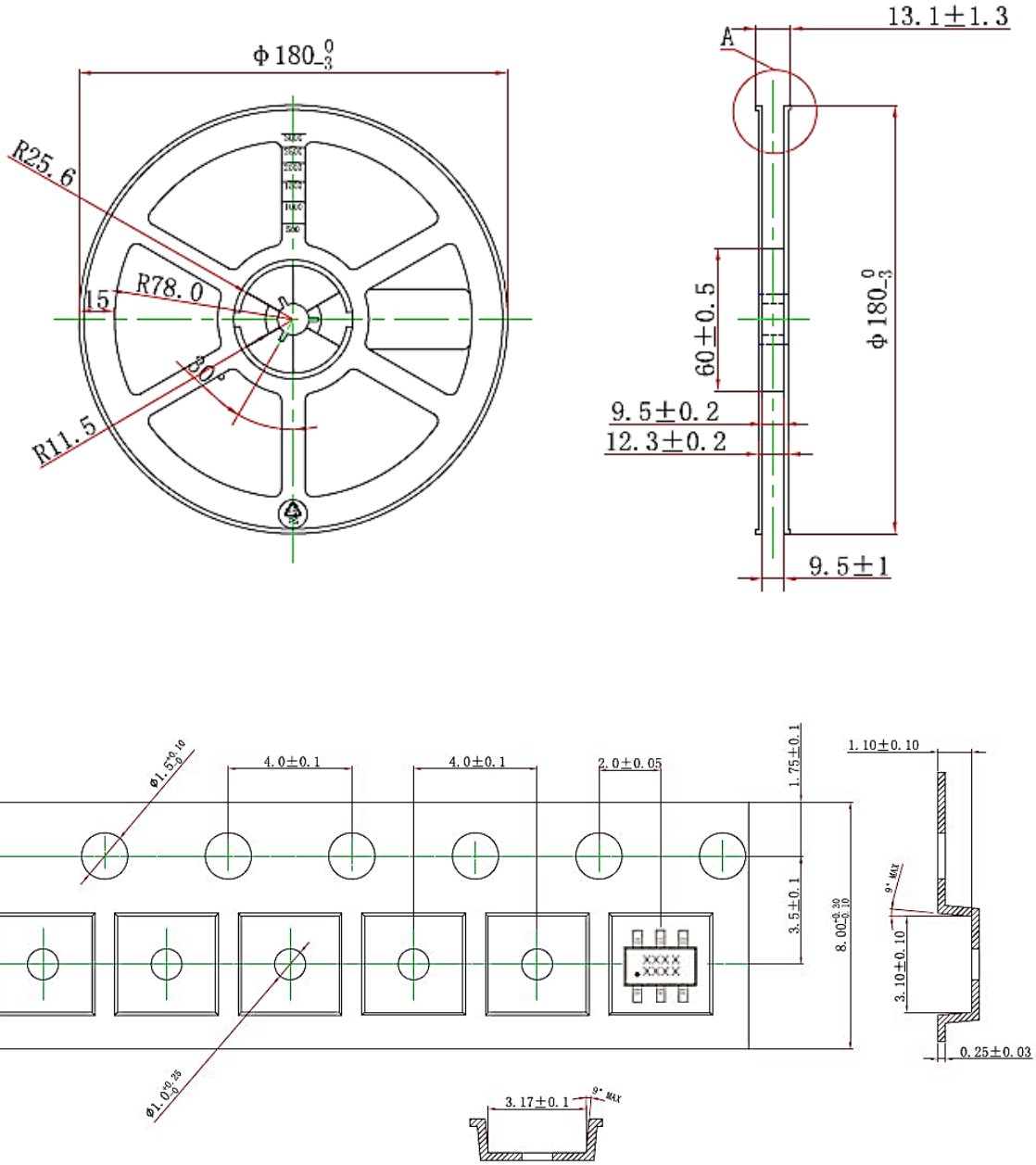
TAPE AND REEL INFORMATION



Feeding Direction