Clockless Link-BD™

Clockless Link-BD™ Deserializer with MIPI CSI-2 Interface for Automotive

BU18RM41-C

General Description

BU18RM41-C supports MIPI CSI-2 data transmission by ROHM's original CDR (Clock Data Recovery) technology. This chip is serial interface receiver IC of the Clockless Link-BD™ series.

BU18RM41-C converts Clockless link stream into a MIPI CSI-2 format, and transmits through four pairs of differential wires.

Features

- AEC-Q100 Qualified *(Note 1)*
  Functional Safety Supportive Automotive Products
- Input Interface: Clockless Link-BD™ 1 Lane
- Output Interface: MIPI D-PHY/CSI-2 4 Lane (☆) *(Note 2)*
  MIPI CSI-2 Ver.1.3 / MIPI D-PHY Ver1.2
  Video Formats: YUV422, RAW8/10/12
- Supported Repeater Mode
  Up to 2M Pixel 30 fps Image Sensor
- Low EMI Transmission by Original DC Balance Protocol and Scrambling
- Supported Functions
  - SSCG (Spread Spectrum Clock Generator)
  - I²C (☆) *(Note 2)*
  - General-Purpose Input/Output (GPIO) 3 pins
- Connect Ability Check
  - CRC
  - Eye Pattern

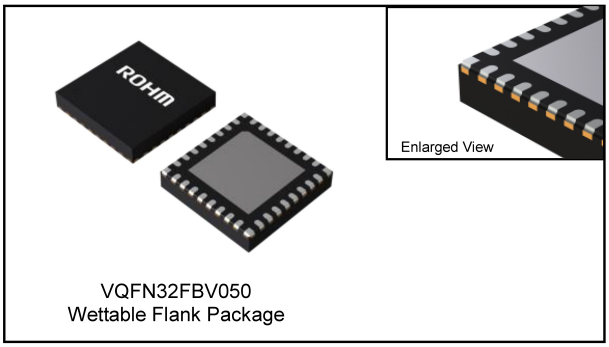
(Note 1) Grade2
(Note 2) (☆): Special Characteristics

Key Specifications

- Supply Voltage Range: VDD18 1.7 V to 3.6 V
- Clockless Link-BD™ Data Rate:
  - Forward Channel 3.6 Gbps/lane (Max)
  - Back Channel 16.875 Mbps/lane (TYP)
- MIPI CSI-2 Data Rate: 1.5 Gbps/lane (Max)
- GPIO Data Rate to BU18TM41: 1 Mbps (Max)
- I²C Clock Frequency: 1 MHz (Max)
- SSCG:
  - Modulation Frequency 30 kHz to 200 kHz
  - Modulation Ratio Up to 2 %
- Operating Temperature Range: -40 °C to +105 °C

Package

Package	W (Typ) x D (Typ) x H (Max)
VQFN32FBV050	5.0 mm x 5.0 mm x 1.0 mm



VQFN32FBV050
Wettable Flank Package

Applications

- Image Sensor Interface

Block Diagram

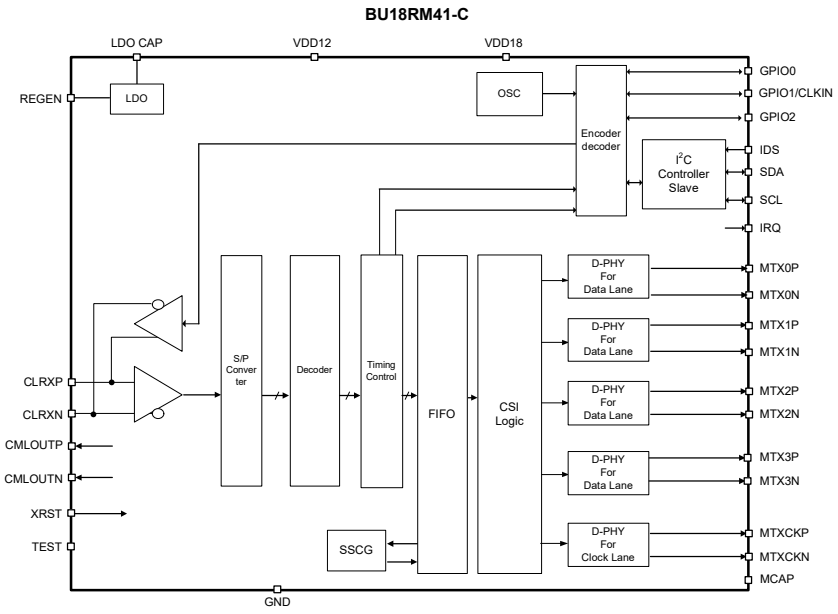


Figure 1. Block Diagram

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.
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Pin Configuration

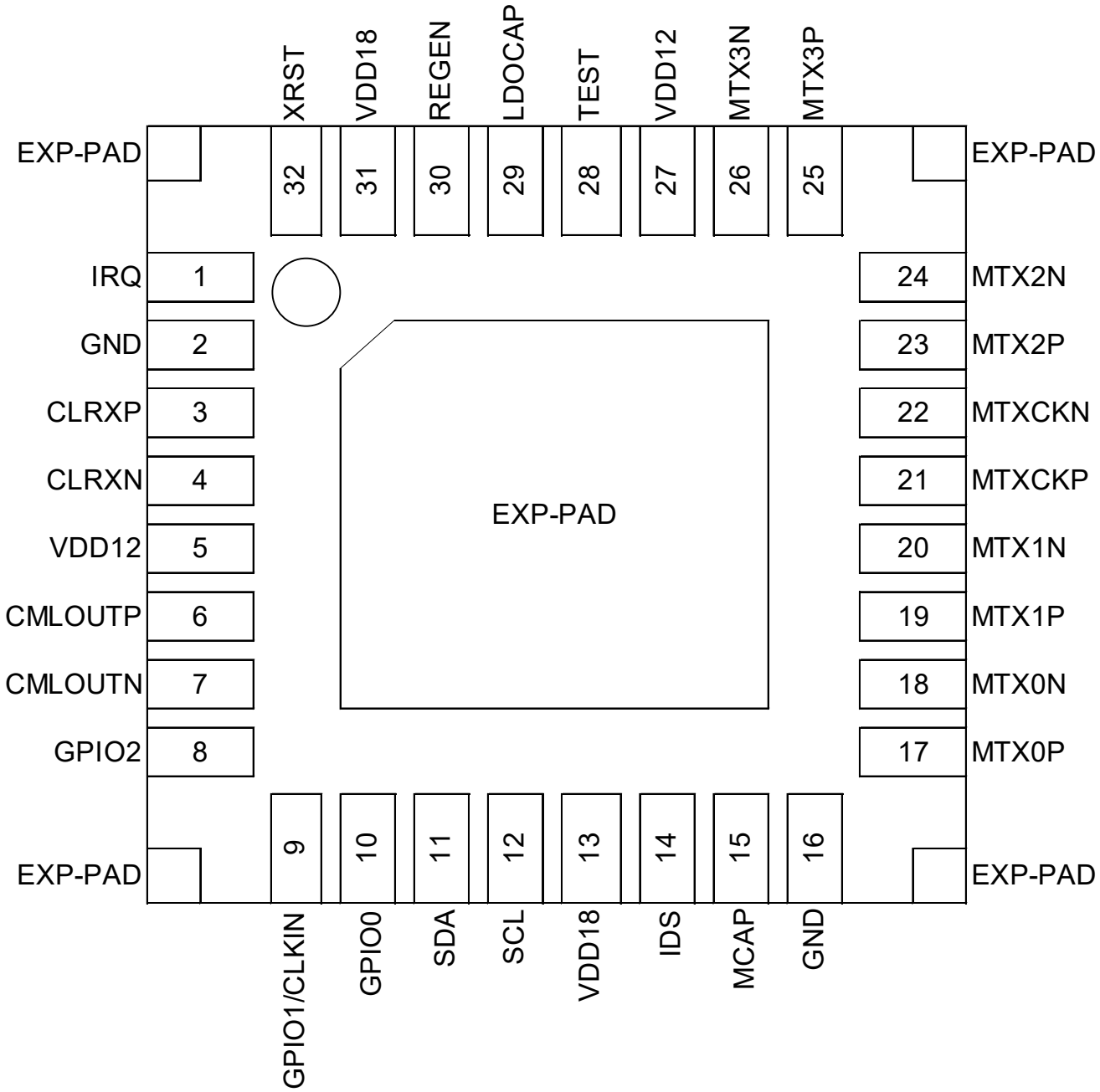


Figure 2. Pin Configuration (Top View)

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Pin Descriptions

Pin No.	Name	Type	Description	Direction	I/O Type
POWER/GND Pin: 7 Pin					
13,31	VDD18	Power	CMOS I/O internal regulator power supply	-	-
5,27	VDD12	Power	Digital power supply Must connect to LDOCAP	-	-
2,16,	GND	Gnd	Ground	-	-
29	LDOCAP	Power	Decoupling capacitor pin This pin should be connected to external decoupling capacitor. Recommended capacitor is 2.2 µF.	-	-
Clockless Link-BD™ Pin: 2 Pin					
3	CLRXP	Analog	Clockless Link-BD™ Receiver input +	In/Out	A
4	CLRXN	Analog	Clockless Link-BD™ Receiver input -	In/Out	A
MIPI Pin: 10 Pin					
17	MTX0P	Analog	MIPI data output 0+	Output	B
18	MTX0N	Analog	MIPI data output 0-	Output	B
19	MTX1P	Analog	MIPI data output 1+	Output	B
20	MTX1N	Analog	MIPI data output 1-	Output	B
21	MTXCKP	Analog	MIPI clock output +	Output	B
22	MTXCKN	Analog	MIPI clock output -	Output	B
23	MTX2P	Analog	MIPI data output 2+	Output	B
24	MTX2N	Analog	MIPI data output 2-	Output	B
25	MTX3P	Analog	MIPI data output 3+	Output	B
26	MTX3N	Analog	MIPI data output 3-	Output	B
GPIO Pin: 3 Pin					
9	GPIO1/ CLKIN	CMOS	General purpose In/Out pin or external clock input	In/Out	D
8,10	GPIO2 GPIO0	CMOS	General purpose In/Out pins	In/Out	D

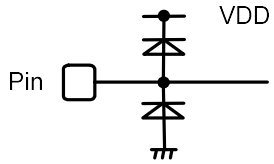
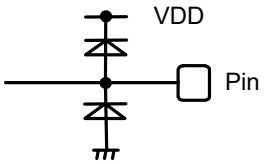
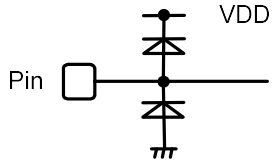
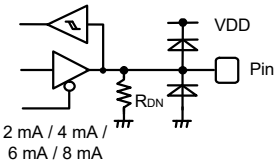
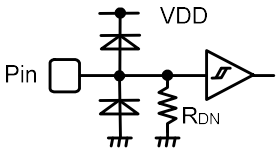
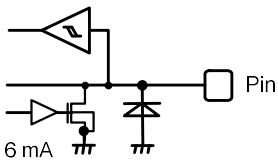
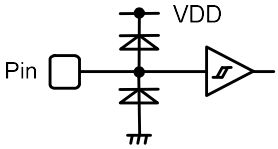
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Pin Descriptions – continued

Pin No.	Name	Type	Description	Direction	I/O Type
Monitor Pin: 2 Pin					
6	CMLOUTP	Analog	CML test output +	Output	B
7	CMLOUTN	Analog	CML test output -	Output	B
Slave Address Pin: 1 Pin					
14	IDS	Analog	Select device address	Input	C
Operation Control Pin: 7 Pin					
1	IRQ	CMOS	Interrupt request pin Active “L”	In/Out	F
15	MCAP	Analog	Decoupling capacitor pin This pin should be connected to external decoupling capacitor. Recommended capacitor is 2.2 µF.	-	-
12	SCL	CMOS	I^2C clock	In/Out	F
11	SDA	CMOS	I^2C data	In/Out	F
30	REGEN	CMOS	LDO enable Must tie to Ground.	Input	C
32	XRST	CMOS	Hardware reset (including all registers) L: Reset active H: Reset non-active	Input	G
28	TEST	CMOS	For test pins ※Must tie to Ground	Input	E
-	EXP-PAD	-	Must tie the center EXP-PAD to Ground. The center EXP-PAD and the corner EXP-PAD are short-circuited inside the package.	-	-

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I/O Equivalent Circuits

Type	Direction	Circuit Type	Applied Pin	Note
A	In/Out		CLRXP, CLRXN	VDD = VDD18
B	Out		MTX0P, MTX0N, MTX1P, MTX1N, MTX2P, MTX2N, MTX3P, MTX3N, MTXCKP, MTXCKN CMLOUTP, CMLOUTN	VDD = VDD12
C	In		IDS, REGEN	VDD = VDD18
D	In/Out		GPIO0, GPIO1/CLKIN, GPIO2	VDD = VDD18
E	In		TEST	VDD = VDD18
F	In/Out		SDA, SCL IRQ	-
G	In		XRST	VDD = VDD18

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	V_{DD18}	-0.3 to +4.5	V	For VDD18
Power Supply Voltage 2	V_{DD12}	-0.30 to +1.68	V	For VDD12 (Internal LDO)
Input Voltage Range 1	V_{IN1}	-0.3 to V_{DD18}+0.3	V	V_{DD18}+0.3 V < 4.5 V
Input Voltage Range 2	V_{IN2}	-0.3 to V_{DD12}+0.3	V	V_{DD12}+0.3 V < 1.68 V
Maximum Junction Temperature	Tjmax	150	°C	-
Storage Temperature Range	Tstg	-55 to +150	°C	-

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 5)*	2s2p*(Note 6)*	
VQFN32FBV050				
Junction to Ambient	θ_{JA}	89.50	31.60	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	12.00	9.00	°C/W

(Note 3) Based on JESD51-2A (Still-Air).
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 5) Using a PCB board based on JESD51-3.
(Note 6) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 7)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 7) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
1.8 V Supply Voltage	V_{DD18}	1.7	1.8	3.6	V	VDD18
1.2 V Supply Voltage	V_{DD12}	1.15	1.25	1.35	V	VDD12 (Internal LDO)
Clockless Link-BD™ Forward Channel Data Rate	f_{CLLF}	1.2	-	3.6	Gbps/ lane	*(Note 8)*
Clockless Link-BD™ Back Channel Data Rate	f_{CLLB}	-	16.875	-	Mbps/ lane	-
MIPI Output Data Rate	f_{MIPI}	0.2	0.8	1.5	Gbps/ lane	*(Note 8)*
GPIO Data Rate to BU18TM41	f_{GPIO}	-	-	1	Mbps	*(Note 9)*
I^2C Operating Frequency	f_{I2C}	-	-	1	MHz	-
CLKIN Input Frequency	f_{CLKIN}	24	27	30	MHz	-
Operating Temperature Range	Topr	-40	+25	+105	°C	-

(Note 8) The input / output data resolution must also meet the following condition.
(Note 9) The GPIO data rate to BU18TM41 is usually 0.25Mbps (max). The rate may slow down due to the I2C command.
Only one pin can be set to 1Mbps (max). In that case, the rate becomes constant without being affected by the I2C command.

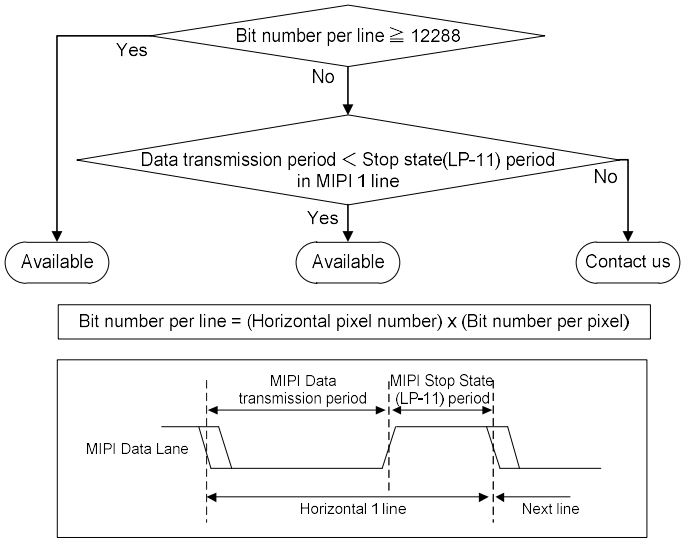


Figure 3. The Data Resolution Condition

Electrical Characteristics - Current Consumption

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Current Consumption	I_{CCW}	-	115	210	mA	Clockless Link-BD™ = 3.6 Gbps MIPI CSI-2 = 600 Mbps MIPI Data Lane = 4 Lane Checker pattern
		-	80	144	mA	Clockless Link-BD™ = 1.4 Gbps MIPI CSI-2 = 466 Mbps MIPI Data Lane = 4 Lane Checker pattern
Power Down Current	I_{CCS}	-	4.0	-	mA	XRST = L

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Electrical Characteristics - DC characteristics

CMOS Pins

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
'L' Input Voltage	V_{IL}	GND	-	0.3 x VDD18	V	GPIO0, GPIO1/CLKIN, GPIO2, SDA, SCL, IRQTEST, XRST
'H' Input Voltage	V_{IH}	0.7 x VDD18	-	VDD18	V	
Hysteresis Voltage	V_H	-	100	-	mV	*(Note 10)*
'L' Input Leak Current	I_{IL}	-10	-	+10	µA	VIN = GND GPIO0, GPIO1/CLKIN, GPIO2, SDA, SCL, IRQ, TEST, XRST
'H' Input Leak Current	I_{IH}	-10	-	+10	µA	VIN = VDD18 SDA, SCL, IRQ, XRST
Pull Down Resistor	R_{DN}	35	50	65	kΩ	GPIO0, GPIO1/CLKIN, GPIO2, TEST
'L' Output Voltage1	V_{OL1}	GND	-	0.6	V	IO = 2/4/6/8 mA GPIO0, GPIO1/CLKIN, GPIO2
'L' Output Voltage2	V_{OL2}	GND	-	0.6	V	IO = 6 mA SDA, SCL, IRQ
'H' Output Voltage	V_{OH}	VDD18 - 0.6	-	VDD18	V	IO = 2/4/6/8 mA GPIO0, GPIO1/CLKIN, GPIO2,

(Note 10) This spec is for schmitt trigger type cell

MIPI pins

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Pin Signal Voltage Range	V_{PIN}	-50	-	+1350	mV	-
Pin Leakage Current	I_{LEAK}	-10	-	+10	µA	-
HS Transmitter						
HS Transmit Static Common-mode Voltage	V_{CMTX}	150	200	250	mV	-
V_{CMTX} Mismatch when Output is Differential-1 or Differential-0	$\lvert\Delta V_{CMTX(1,0)}\rvert$	-	-	5	mV	-
HS Transmit Differential Voltage	$\lvert V_{OD}\rvert$	140	200	270	mV	-
V_{OD} Mismatch when Output is Differential-1 or Differential-0	$\lvert\Delta V_{OD}\rvert$	-	-	14	mV	-
HS Output High Voltage	V_{OHHS}	-	-	360	mV	-
Single-ended Output Impedance	Z_{OS}	40	50	62.5	Ω	-
Single ended Output Impedance Mismatch	ΔZ_{OS}	-	-	10	%	-
LP Transmitter						
Thevenin Output High Level	V_{OH}	1.10	1.20	1.30	V	-
Thevenin Output Low Level	V_{OL}	-50	-	+50	mV	-
Output Impedance of LP Transmitter	Z_{OLP}	110	-	-	Ω	-

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Electrical Characteristics - DC characteristics – continued

Clockless Link-BD™ Pins

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Internal Termination Resistance	R_T	-	100	-	Ω	Differential across CLRXP and CLRXN

IDS Pin

Parameter		Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
Primary Assigned I²C Address	60	V_{IDS}	0	0	0.04 x VDD18	V	−
	61		TYP – (0.04 x VDD18)	0.142 x VDD18	TYP + (0.04 x VDD18)	V	−
	62		TYP – (0.04 x VDD18)	0.285 x VDD18	TYP + (0.04 x VDD18)	V	-
	63		TYP – (0.04 x VDD18)	0.428 x VDD18	TYP + (0.04 x VDD18)	V	-
	64		TYP – (0.04 x VDD18)	0.571 x VDD18	TYP + (0.04 x VDD18)	V	-
	65		TYP – (0.04 x VDD18)	0.714 x VDD18	TYP + (0.04 x VDD18)	V	-
	66		TYP – (0.04 x VDD18)	0.857 x VDD18	TYP + (0.04 x VDD18)	V	-
	67		TYP – (0.04 x VDD18)	VDD18	VDD18	V	-

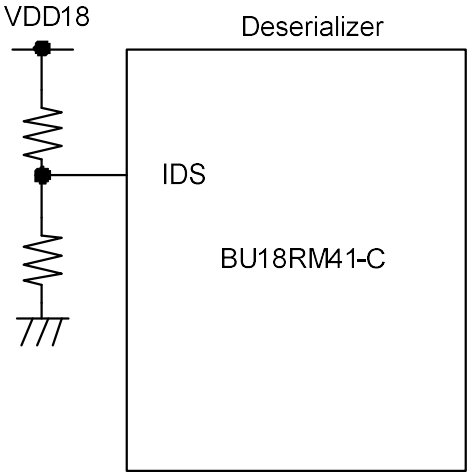


Figure 4. IDS Applications Circuit

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Electrical Characteristics - AC characteristics

Spread Spectrum Clock Generator (SSCG) Pins

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Clock Frequency	f_{IN}	20	-	100	MHz	−
Output Clock Frequency	f_{OUT}	20	-	100	MHz	−
Output Modulation Frequency	f_{OMOD}	30	-	200	kHz	-
Output Modulation Ratio	r_{OMOD}	-2.0	-	+2.0	%	*(Note 11)*

(Note 11) The output modulation ratio of up to 3 % includes input modulation ratio (up to 0.5 %).

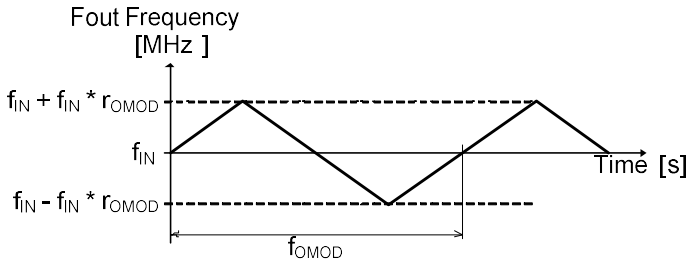


Figure 5. SSCG Profile

I²C Pins

Parameter	Symbol	Limit				Unit	Conditions
		Fast-mode		Fast-mode Plus			
		Min	Max	Min	Max		
SCL Clock Frequency	f_{SCL}	80	400	80	1000	kHz	-
Hold Time (repeated) START Condition	$t_{HD;STA}$	0.6	-	0.26	-	µs	-
Low Period of the SCL Clock	t_{LOW}	1.3	-	0.50	-	µs	-
High Period of the SCL Clock	t_{HIGH}	0.6	-	0.26	-	µs	-
Data Hold Time	$t_{HD;DAT}$	0	-	0	-	µs	-
Data Set-up Time	$t_{SU;DAT}$	0.1	-	0.05	-	µs	-
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	0.6	-	0.26	-	µs	-
Set-up Time for STOP Condition	$t_{SU;STO}$	0.6	-	0.26	-	µs	-
Bus Free Time between STOP and START Condition	t_{BUF}	1.3	-	0.50	-	µs	-

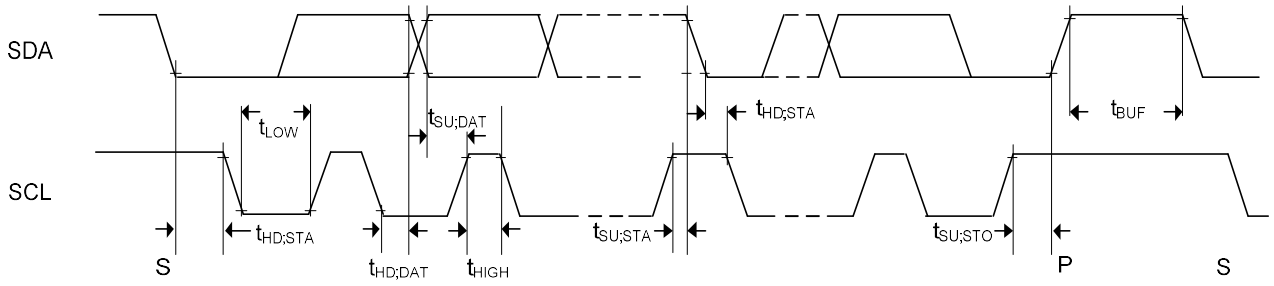


Figure 6. I²C AC Timing

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Electrical Characteristics - AC characteristics – continued

MIPI Pins

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
HS Transmitter						
20 % to 80 % Rise Time and Fall Time	t_R, t_F	-	-	0.35	UI	-
		100	-	-	ps	-
Data-to-Clock Skew	t_{skw}	-0.15	-	+0.15	UI	0.2 Gbps < Data Rate ≤ 1.0 Gbps
		-0.20	-	+0.20	UI	1.0 Gbps < Data Rate ≤ 1.5 Gbps
UI Instantaneous	UI_{INS}	0.667	-	5.0	ns	-
Common-Level Variation Above 450 MHz	ΔVCMTX (HF)			15	mV_{RMS}	-
Common-Level Variation Between 50 MHz to 450 MHz	ΔVCMTX (LF)			25	mV_{RMS}	-
LP Transmitter						
15 % to 85 % Rise Time and Fall Time	t_{RLP}, t_{RLP}	-	-	25	ns	-
30 % to 85 % Rise Time and Fall Time	T_{REOT}	-	-	35	ns	-

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Power On/Off Sequence

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VDD18 Rise Time	t_{V18R}	-	-	10	ms	-
VDD18 Fall Time	t_{V18F}	-	-	10	ms	-
VDD18 Off Time	t_{V18_OFF}	100	-	-	ms	-
Reset Delay Time	t_{RC}	5	10	-	ms	-
XRST L Pulse Width	t_{LRST}	10	-	-	µs	-
XRST on to I²C	t_{RSTI2C}	10	-	-	µs	-



Figure 7. Power Supply Rise and Fall Time

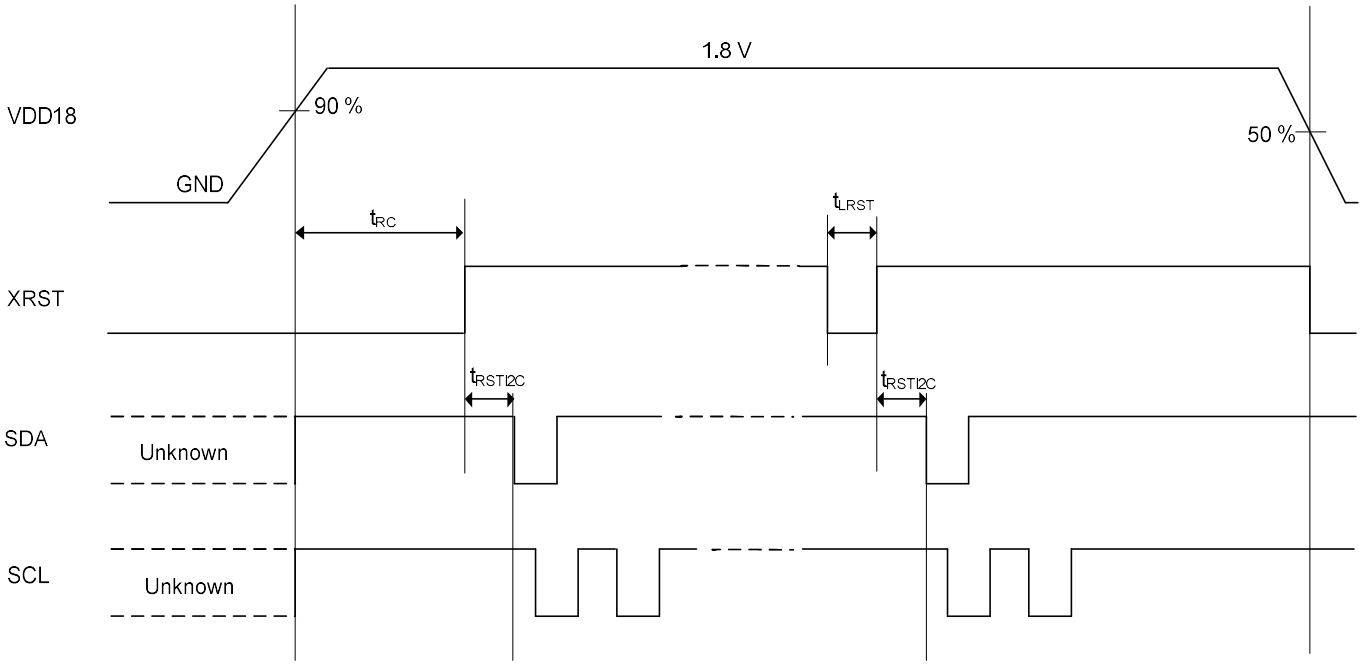


Figure 8. Power Supply Sequence

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Applications Examples

POC (Power Over Coaxial) Cable

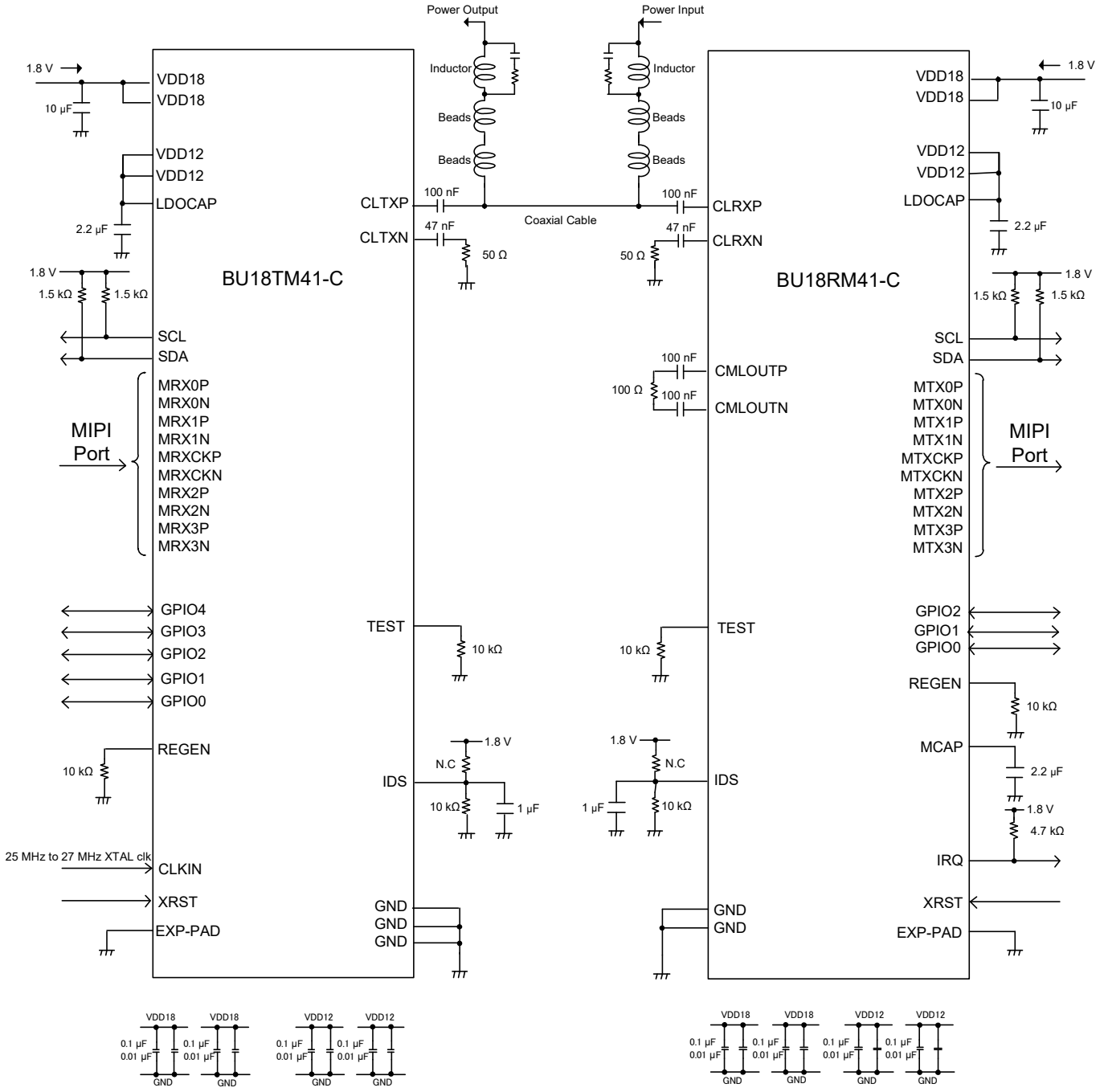


Figure 9. Applications Diagram (POC Cable)

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Applications Examples – continued

STP (Shielded Twisted Pair) Cable

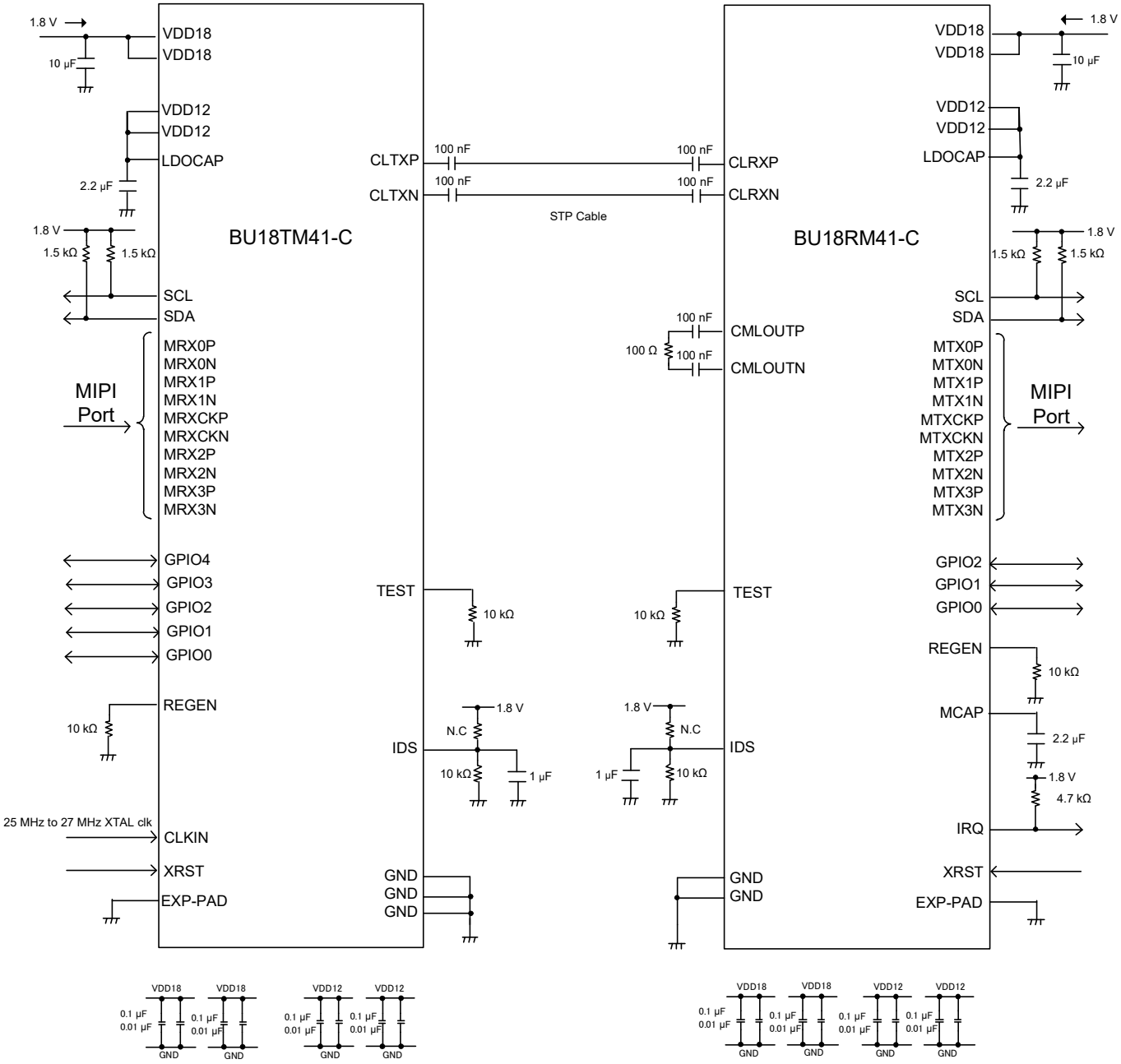


Figure 10. Applications Diagram (STP Cable)

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

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Operational Notes – continued

12. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.
"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.
"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

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Ordering Information

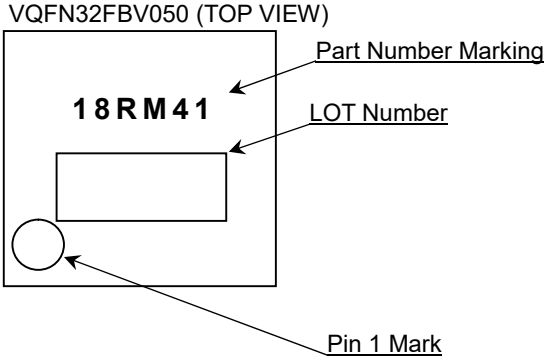
B U 1 8 R M 4 1	-	CE 2

Part Number

Product Rank
C: for Automotive
Packaging Specification
E2: Embossed tape and reel

Marking Diagrams

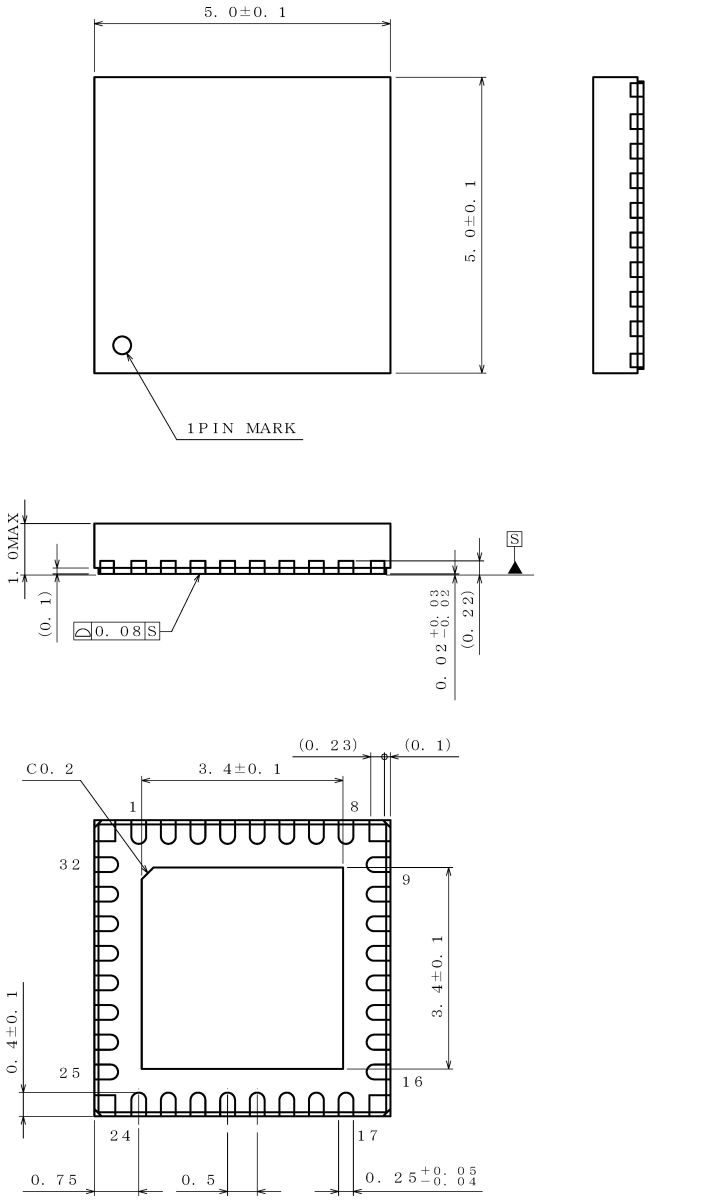
VQFN32FBV050 (TOP VIEW)



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Physical Dimension and Packing Information

Package Name	VQFN32FBV050



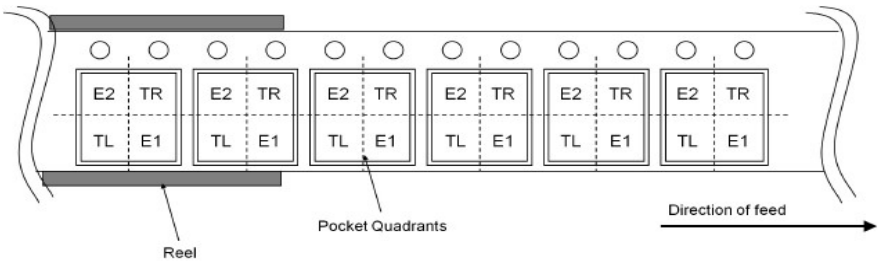
(UNIT : mm)

PKG : VQFN32FBV050
Drawing No. EX416-5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
2020.07.21	Rev.0.08	Changed from Rev.0.07

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